Evaluating the AD4060/AD4062 Compact, Low Power, 12-Bit/16-Bit, 2MSPS Easy Drive SAR ADCs

FEATURES

- Full featured evaluation boards for the AD4060 and AD4062 with a USB power solution
- Single differential channel and common-mode input available through SMA connectors
- Out of the box evaluation experience with the Nucleo-H563ZI
- PC software (ACE plugin) for control and data analysis of the time and frequency domains
- Compatible with other Arduino form factor controller boards

EQUIPMENT NEEDED

- PC with Windows 7 or later operating system
- Nucleo-H563ZI controller board and the accompanying USB cable
- Precision signal generator (see the Evaluation Board Hardware section)

SOFTWARE NEEDED

- ACE evaluation software
- AD4060/AD4062 ACE plugin from the plugin manager (see the Software Installation Procedure section)

EVALUATION BOARD KIT CONTENTS

- EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ evaluation board

USEFUL LINKS AND RESOURCES

- AD4060 product page
- AD4062 product page
- EVAL-AD4060-ARDZ product page
- EVAL-AD4062-ARDZ product page
- ACE Installer

GENERAL DESCRIPTION

The EVAL-AD4060-ARDZ and EVAL-AD4062-ARDZ evaluation boards enable quick and easy evaluation of the performance and features of the AD4060 or the AD4062, respectively. The AD4060 and AD4062 are compact, low power, 12-bit or 16-bit (respectively) Easy Drive successive approximation register (SAR) analog-to-digital converters (ADCs).

The primary controller board for the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ is the Nucleo-H563ZI. The EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ conform to the Arduino® Uno Shield mechanical and electrical standards to interface with the Nucleo-H563ZI, in addition to various software development kits from other manufacturers.

The AD4060/AD4062 evaluation solutions include the AD4060/AD4062 industrial input and output (IIO) firmware application drivers for device configuration and ADC data capture and the AD4060/AD4062 ACE plugin graphical user interface (GUI) for performance evaluation.

EVALUATION BOARD PHOTOGRAPH

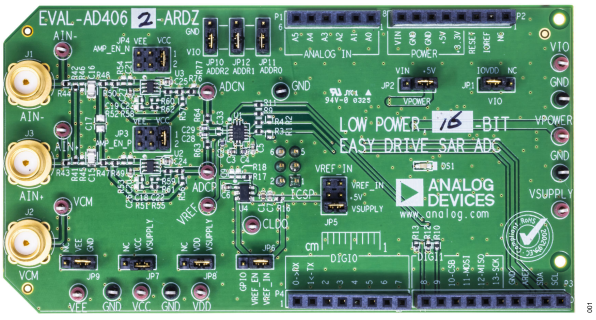

Figure 1. EVAL-AD4062-ARDZ Evaluation Board Photograph

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REVISION HISTORY

7/2025—Revision 0: Initial Version

QUICK START GUIDE

The AD4060/AD4062 ACE plugin is the evaluation GUI that interfaces with the firmware on the Nucleo-H563ZI controller board to communicate with the connected EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ evaluation board. The ACE software must be installed prior to installing and running the AD4060/AD4062 ACE plugin. See the Software Installation Procedure section for instructions on downloading the ACE software and the AD4060/AD4062 ACE plugin.

HARDWARE SETUP

This section details how to set up the AD4060/AD4062 and Nucleo-H563ZI boards for use with the AD4060/AD4062 ACE plugin. Refer to the Evaluation Board Hardware section for detailed descriptions of the on-board circuit blocks and for descriptions of all jumpers referenced in this section.

To set up the hardware, complete the following steps:

- Disconnect both the evaluation board and the Nucleo-H563ZI from all power sources before connecting them together.
- The EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ connect to the Nucleo-H563ZI via the Arduino Uno compatible headers (P1 to P4). Plug the headers on the bottom side of the evaluation board to the corresponding headers on the top side of the Nucleo-H563ZI (see Figure 2).

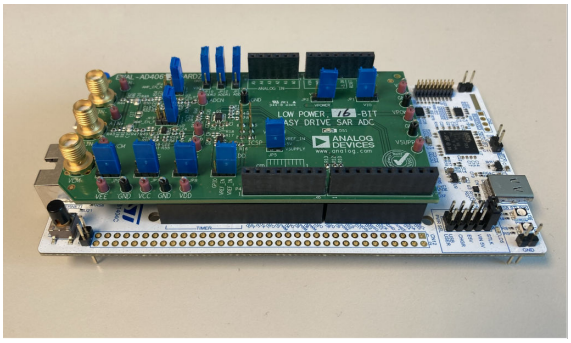

Figure 2. EVAL-AD4062-ARDZ and Nucleo-H563ZI Connections

After the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ are connected to the Nucleo-H563ZI board, power can be applied to the Nucleo-H563ZI. The PWR SEL jumper (JP2) on the Nucleo-H563ZI can be used to select between different input power options for powering up the Nucleo-H563ZI. STLK is the default jumper setting for PWR_SEL and uses the USB STLINK as the power source. The LD5 light-emitting diode (LED) illuminates when Nucleo-H563ZI is receiving power from its PWR_SEL source. On the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ, the DS1 LED illuminates when the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ are receiving power from the Nucleo-H563ZI and are generating the +3.3V rail to the on-board AD4060/AD4062 and its companion circuitry.

When powering from the USB, perform the following steps:

- Ensure the JP2 jumper on the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ is set to the +5V position. This position connects the evaluation board power management circuitry to the +5V pin on the Arduino Uno power header.
- Connect the Nucleo-H563ZI to the PC with a USB cable. After a few seconds, the PWR LED (LD6) on the Nucleo-H563ZI illuminates to indicate the Nucleo-H563ZI is receiving power from the USB.

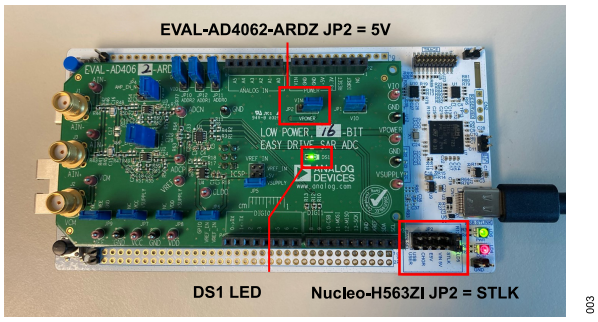

Figure 3. EVAL-AD4062-ARDZ and Nucleo-H563ZI on USB Power

When powering from an external power supply, perform the following steps:

- Ensure the JP2 jumper on the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ is set to the VIN position. This position connects the evaluation board power management circuitry to the VIN pin on the Arduino Uno power header.
- Set the JP2 jumper on the Nucleo-H563ZI to VIN 5V position. This allows a 7V to 12V DC signal to be supplied to the VIN Arduino Uno power header, and the Nucleo-H563ZI's on-board LDO supplies a steady 5V power to the Nucleo-H563ZI circuitry. See the Nucleo-H563ZI user manual for additional ways to use an external power source to power up the Nucleo-H563ZI and set the PWR SEL jumper accordingly.
- After the external power supply is connected, connect the Nucleo-H563ZI to the PC with a USB cable.

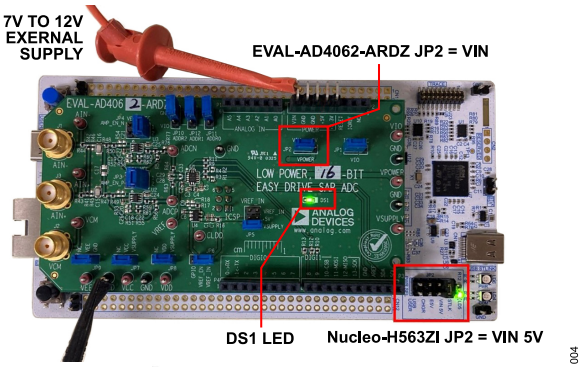

Figure 4. EVAL-AD4062-ARDZ and Nucleo-H563ZI on External DC Power

Before launching the AD4060/AD4062 ACE plugin, it is recommended to connect a precision signal source or signal generator to the analog input Subminiature Version A (SMA) connectors to drive

QUICK START GUIDE

the AD4060/AD4062 inputs into their specified operating ranges. See the Analog Front End (AFE) section for more information.

If no signal generator is available, a jumper cable between the VREF and VCM test points can be used to bias the AD4060/AD4062 analog inputs to VREF. This is preferred over connecting the amplifier inputs to GND, because the amplifier VEE rails are connected to GND by default.

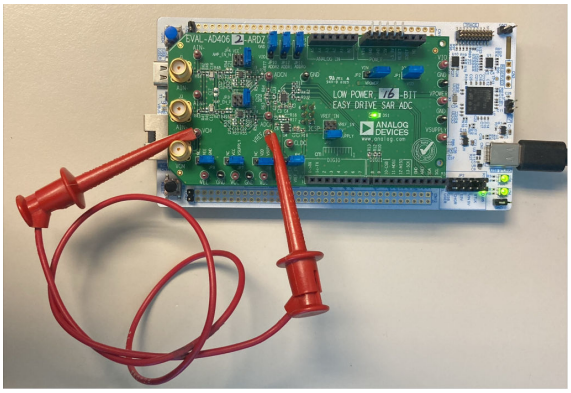

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Figure 5. Biasing the EVAL-AD4062-ARDZ Inputs Without Signal Generator Hardware for Software Validation

EVALUATION BOARD HARDWARE

HARDWARE OVERVIEW

The EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ include the AD4060/AD4062 with companion circuitry for an out of the box evaluation experience. The EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ also include several prototyping options for the analog and digital circuitry on board, as described in the following sections.

Figure 6 shows a simplified block diagram of the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ. Figure 7 and Figure 8 show the location of the primary circuit blocks on the board. The factory-default circuitry includes the following:

- AD4060BCPZ/AD4062BCPZ: the 14-lead LFCSP model of the AD4060/AD4062
- The low-noise, low-power MAX6070 voltage reference provides a 2.5V reference voltage for the AD4060/AD4062
- Two low-power, rail-to-rail input and output MAX44260 operational amplifiers (op amps) buffer the signal generator's output to the AD4060/AD4062 analog inputs
- The AD7118 regulates the Nucleo-H563ZI input power source down to a 3.3V rail to power the AD4060/AD4062 and other analog components

These companion components were selected to simplify evaluation and achieve typical performance characteristics of the AD4060/AD4062 and are not necessarily applicable to all system designs and use cases.

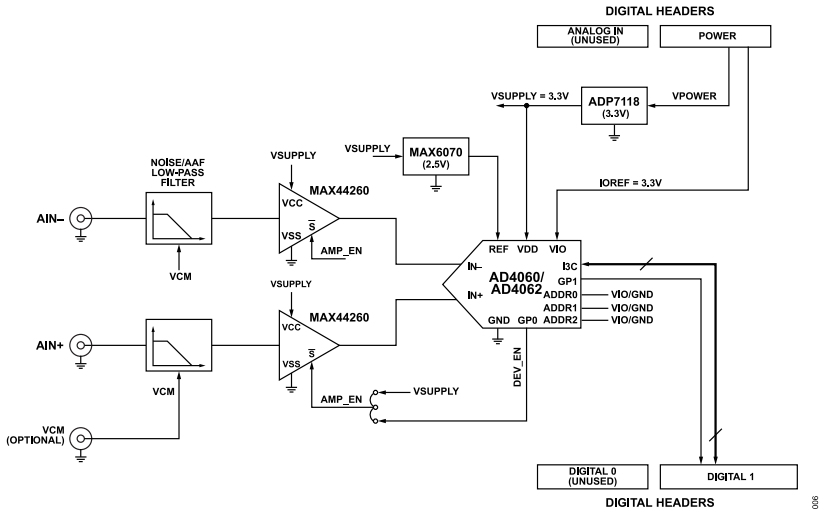

Figure 6. EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ Simplified Block Diagram

EVALUATION BOARD HARDWARE

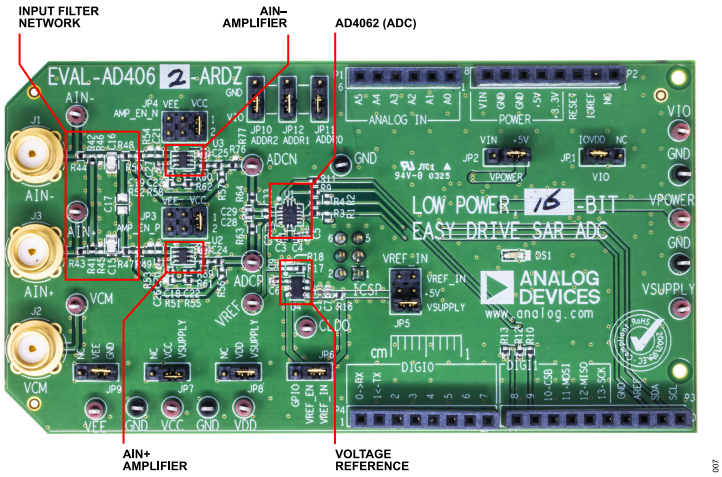

Figure 7. EVAL-AD4062-ARDZ Evaluation Board Circuitry Locations—Top Side

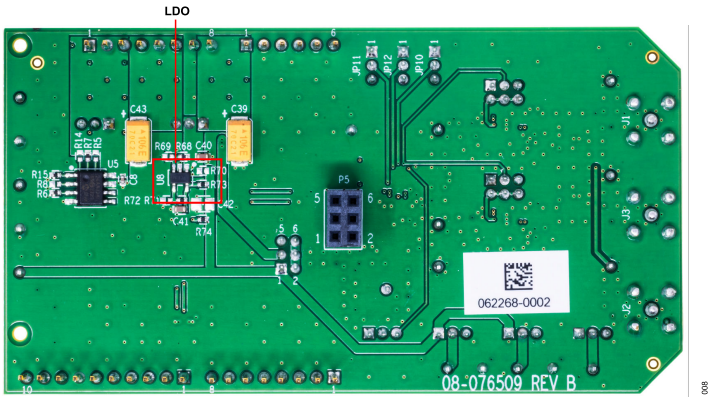

Figure 8. EVAL-AD4062-ARDZ Evaluation Board Circuitry Locations—Bottom Side

EVALUATION BOARD HARDWARE

CONNECTORS AND SOCKETS

The connectors and sockets on the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ are outlined in Table 1.

Table 1. On-Board Connectors

Connector	Function
AIN−	Negative analog input (SMA)
AIN+	Positive analog input (SMA)
VCM	Common-mode input (SMA)
P1 to P4	Arduino Uno headers

DIGITAL INTERFACE CONNECTIONS

The AD4060/AD4062 digital interface includes an I3C interface for reading and writing data, and two GPIOs with multiple functions. The AD4060/AD4062 digital interface signals are transmitted between the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ and the controller board via the Arduino Uno digital headers (P3 and P4). The digital pin function assignment conforms to the Arduino Uno standard, with the I3C interface on the standard I2C header pins. Table 2 details the digital signal names, default and secondary functions, and digital header pin assignments.

The AD4060/AD4062 include three digital input pins ADDR0, ADDR1, and ADDR2. The ADDR[2:0] pins enable the assignment of up to eight unique part instance values to support up to eight AD4060/AD4062s on one I3C bus. The EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ's jumpers JP11, JP 12, and JP10 allow for setting the ADDR0, ADDR1, and ADDR2 respectively to either VIO or GND.

Currently, the default EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ software only supports an ADDR[2:0] value = 3'b000. When evaluating the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ using the default software in ACE, ADDR0, ADDR1, and ADDR2 all must be set to GND.

The EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ include an electrically erasable programmable read-only memory (EEPROM) (U5) used by the AD4060/AD4062 ACE plugin to identify and connect to the board. The controller board communicates with the EEPROM via the inter-integrated circuit (I2C) pins on the Arduino Uno header.

Note the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ include the ICSP header (P5) to conform to the Arduino Uno mechanical specification only. The pins on this header are not routed out as signals to the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ.

Table 2. Digital Header Connections

Signal Name	Function	Header Pin	Arduino Pin Name	Pull-Up/Pull-Down
GP1	ADC GPIO 1. Functions as the data ready (RDYb) signal from the AD4060/AD4062 by default.	P3 Pin 1	D8	100kΩ pull-down (R13)
GP0	ADC GPIO 0. No function by default. Can optionally be configured as the AD4060/AD4062 DEV_EN timer output to power-cycle the front-end amplifiers with custom firmware (see JP3 and JP4).	P3 Pin 2	D9/PWM	100kΩ pull-down (R12)
SDA_ARD	I^3C serial data. Also used to read board ID data from the EEPROM in I2C mode.	P3 Pin 9	SDA	
SCL_ARD	I^3C serial clock. Also used to read board ID data from the EEPROM in I2C mode.	P3 Pin 10	SCL	

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POWER SUPPLIES

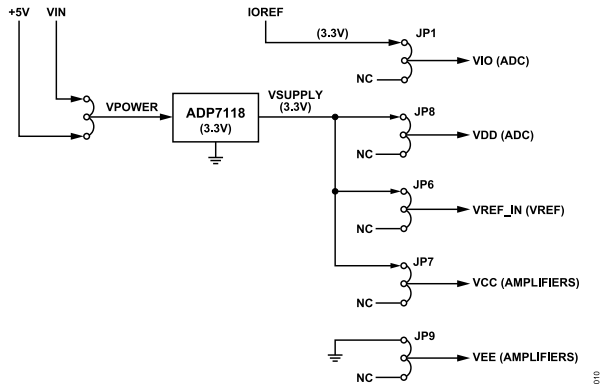

Figure 9. EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ Power Tree

Figure 9 shows the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ power tree. In factory default configuration, the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ analog circuitry is powered by an on-board 3.3V supply and the AD4060/AD4062 I/O logic voltage is supplied directly from the controller board's IOREF voltage. The on-board ADP7118 LDO regulator (U8) regulates the controller board power into a low-noise 3.3V rail to supply the AD4060/AD4062, the voltage reference, and the op amps.

The controller board (Nucleo-H563ZI, for example) provides the input power for the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ through the Arduino Uno power header (P2 on the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ). The JP2 jumper selects between the +5V or VIN as the input source of the ADP7118 that supplies the 3.3V analog rail. By default, +5V is selected, as 5V has enough headroom for the ADP7118 to generate a regulated 3.3V output. The Nucleo-H563ZI can generate the 5V supply from either an external DC supply or from the USB port (see the Nucleo-H563ZI user manual for more detail). The EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ supply current demand in the default configuration is low enough to be powered off the USB port without an additional supply.

The AD4060/AD4062 digital I/O logic supplies (VIO) are sourced directly from the IOREF voltage from the controller board via P2. This ensures the AD4060/AD4062 digital interfaces operate on the same logic levels as the controller board. The AD4060/AD4062 support 3.3V logic. By default, the JP1 jumper connects the VIO supply on the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ to the IOREF supply from the controller board.

Table 3 lists the power domains present on the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ as named in the schematic. Each power rail can be measured or driven with external supplies via the test points labeled in the table. See the Hardware and Link Options section for details on how to configure the jumpers to supply the rails with external supplies. Refer to the data sheets for each relevant product when providing power externally.

Table 3. EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ Power Domains

Power Rail	Function	Test Point Name	Default Nominal Voltage (V)
+5V	5V power source from the P2 header.	N/A	5
VIN	VIN power source from the P2 header.	N/A	7 to 12
IOREF	Controller board I/O logic supply.	N/A	3.3
GND	Power ground.	GND	0
VPOWER	Primary power input from the P2 header. Sourced from either +5V or VIN.	VPOWER	5
VSUPPLY	Primary analog supply generated by on-board ADP7118. Distributed to analog component supply pins.	VSUPPLY	3.3
VCC	Amplifier positive supply rail.	VCC	3.3 (VSUPPLY)
VEE	Amplifier negative supply rail.	VEE	0 (GND)
VREF_IN	Voltage reference supply input.	N/A	3.3 (VSUPPLY)
VDD	AD4060/AD4062 analog input, sourced from VSUPPLY via JP8.	VDD	3.3 (VSUPPLY)
CLDO	AD4060/AD4062 internal LDO regulator output. By default, the AD4060/AD4062 generates this supply with an internal LDO regulator.	CLDO	1.8
VIO	AD4060/AD4062 digital logic supply.	VIO	3.3 (IOREF)

EVALUATION BOARD HARDWARE

VOLTAGE REFERENCE CIRCUIT

In the factory default configuration, the on board MAX6070 (U4) provides a 2.5V reference voltage (VREF) to the AD4060/AD4062 REF input. The VREF sets the input range of the AD4060/AD4062, as described in the AD4060 and AD4062 data sheets. By default, the MAX6070 is powered by the 3.3V analog rail. A 2.2µF VREF decoupling capacitor (C2) is located next to the AD4060/AD4062 REF pin to ensure a stable 2.5V VREF voltage during the conversion time of the SAR ADC core.

ANALOG FRONT END (AFE)

The AFE components provide signal conditioning between the signal generator outputs and the AD4060/AD4062 analog inputs (IN+ and IN− pins). In the factory default configuration, the AFE consists of the following components:

- SMA connectors for the positive and negative inputs (J1 and J2, respectively)
- SMA connector for an optional common-mode voltage (VCM) source (J3)
- Passive filter network for signal generator noise and/or anti-aliasing filtering (see Figure 10)
- MAX44260 operational amplifiers in 6-lead SC70 footprint configured as unity-gain buffers by default (see Figure 11)
- RC kickback filter at the AD4060/AD4062 inputs

The Analog Inputs section provides instructions for interfacing the signal generator and the SMA inputs on the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ.

By default, the amplifiers are configured as unity-gain buffers, but optional passive components are included in the design to support noninverting with gain, single-pole active filter, and Sallen-Key filter configurations.

By default, all amplifiers are powered with a single supply with VEE connected to GND and VCC supplied by VSUPPLY = 3.3V. See the Power Supplies section for more details.

The shutdown pins on the AFE amplifiers can optionally be routed to the GP0 pin on the AD4060/AD4062 via JP3 and JP4 jumpers. This allows performance and power measurements using the DEV_EN control signal from the AD4060/AD4062 to power-cycle the amplifiers in between conversions. See the AD4060 and AD4062 data sheets for more information on the DEV_EN control signal for dynamic power cycling of the AFE.

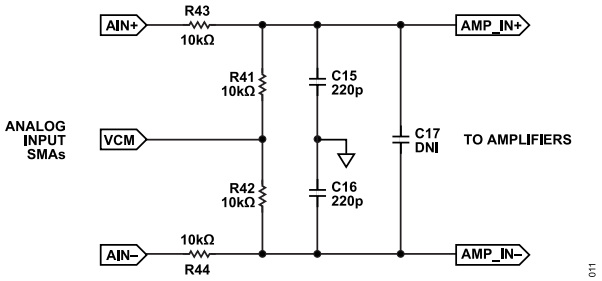

Figure 10. Signal and Common-Mode Inputs and Input Filter

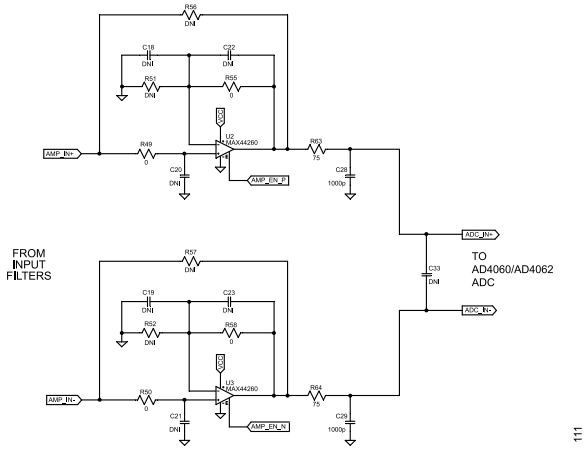

Figure 11. Default Amplifier Circuit Simplified Schematics

Analog Inputs

This section provides guidance for driving the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ with a precision signal generator for ADC performance evaluation.

The AD4060/AD4062 input range is set by the VREF voltage. In the factory default configuration, the on board MAX6070 generates a 2.5V VREF (see Voltage Reference Circuit section). Therefore, the AD4060/AD4062 input is 0V to 2.5V on either input (IN+ and IN−) for a resulting maximum differential input swing of 2.5V peak and 5V p-p.

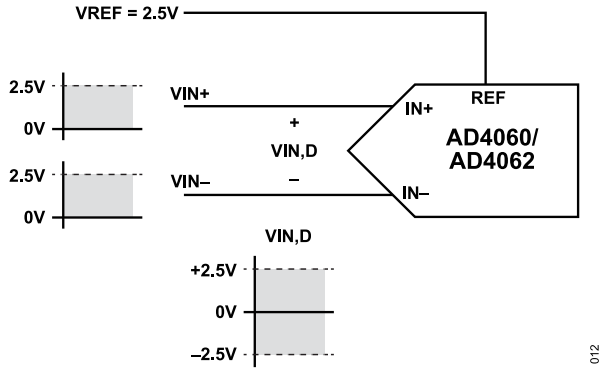

Figure 12. AD4060/AD4062 Input Range

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By default, the MAX44260 amplifiers driving the AD4060/AD4062 analog inputs are configured as unity-gain buffers, so the signal on their noninverting inputs must also be limited to 0V to 2.5V. When populating optional feedback networks for larger gain, the input signal must be limited such that the output swings of the amplifier stay within the AD4060/AD4062 input range.

The following provides some examples for hooking up different types of signal generators to the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ. All of the following examples ignore the output impedance of the signal generator:

- For signal generators with bipolar, differential output swings (signals that go below GND), the VCM input provides a means to apply the necessary DC offset to satisfy the input range specification of the MAX44260 amplifiers. Figure 13 gives an example with a 2.5V VREF and amplifiers in unity-gain configuration. The signal source (VS) is 5V peak or 10V p-p and VCM is 2.5V DC.
- For signal generators with floating, differential outputs, the VCM input provides a means to apply the necessary DC offset to satisfy the input range specification of the MAX44260 amplifiers. Figure 14 gives an example with a 2.5V VREF and amplifiers in unity-gain configuration. The differential input swing (VIN,diff) is 5V peak or 10V p-p and VCM is 1.25V DC.
- For signal generators with differential outputs that provide their own DC offset, the VCM input can be left disconnected. In the factory default configuration, the R41 and R42 resistors that are used with the VCM input will attenuate the differential input signal by half. It is recommended to disconnect R41 and R42 when using these types of signal generators, as shown in Figure 15. VIN,diff is 2.5V peak or 5V p-p, and VCM is 1.25V DC.

Note that any noise generated by the signal generator will propagate through the AFE circuit and appear at the AD4060/AD4062 analog inputs. If the noise of the signal generator is large enough, performance metrics like SNR, RMS noise, and others will be affected. If the noise signal is common to both the positive and negative inputs, then the AD4060/AD4062 will reject some portion of it depending on the bandwidth of the device. If the noise signal is differential (or when operating the board with a single-ended signal generator), the noise will couple directly into the ADC samples.

By default, the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ are populated with a single-pole RC low-pass filter set to a bandwidth of ~140kHz to assist with anti-aliasing and noise filtering. The RC filter components can be modified based on the input signal bandwidth and noise targets for the evaluation or prototyping system.

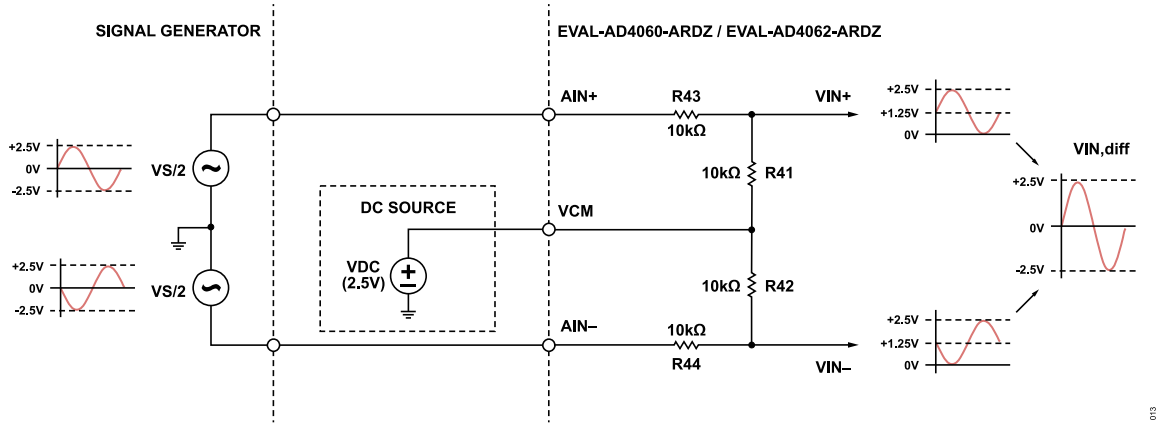

Figure 13. Bipolar Differential Signal Generator Example

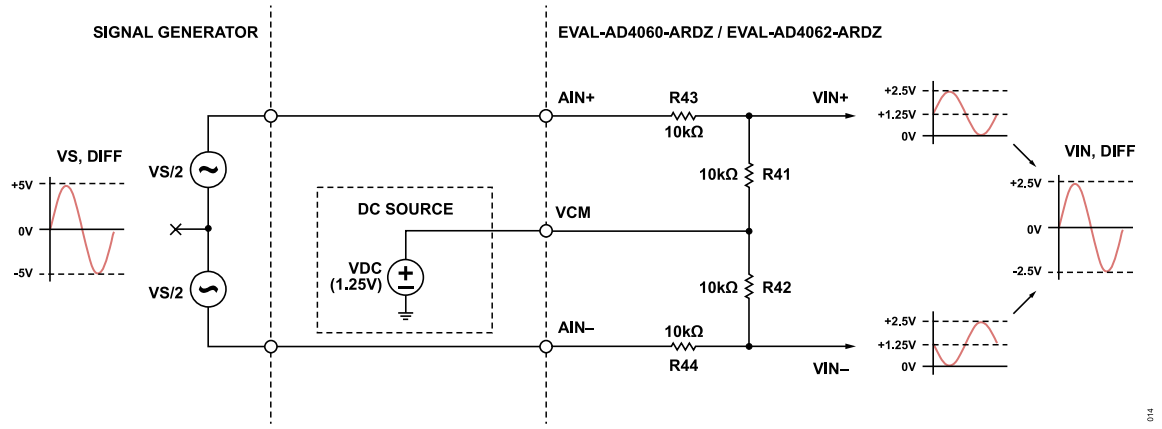

Figure 14. Floating Differential Signal Generator Example

EVALUATION BOARD HARDWARE

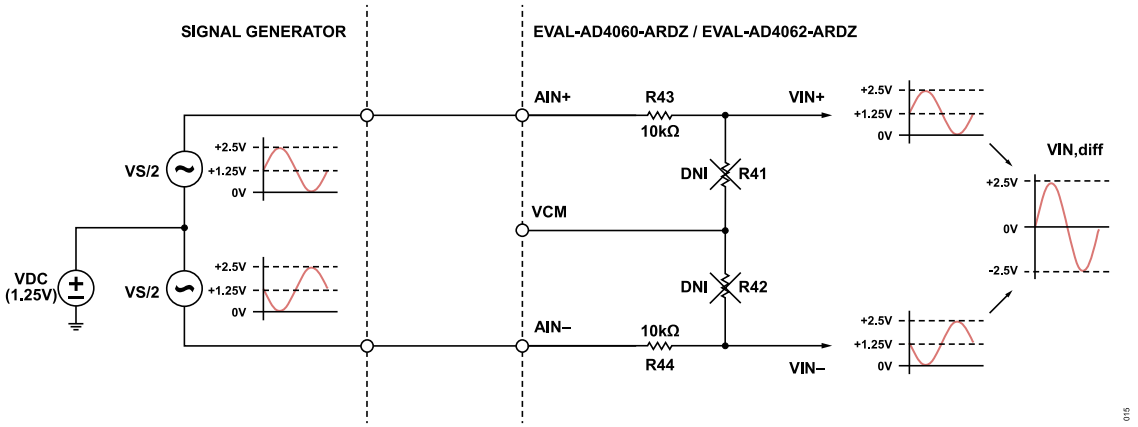

Figure 15. Biased Differential Signal Generator Example

EVALUATION BOARD HARDWARE

HARDWARE AND LINK OPTIONS

Table 4 details each of the optional jumper and link options present on the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ with a brief description of the default and secondary positions and functions.

Table 4. Jumper and Link Options and Descriptions

Jumper Reference Designator	Description	Default Position/Function	Secondary Position/Function(s)
JP1	VIO Source Selection	1: VIO supplied by the IOREF supply of the controller board.	3: No connect. Place the jumper in this position if supplying VIO by an external supply.
JP2	VPOWER Source Selection	3: VPOWER supplied by the +5V supply of the controller board.	1: VPOWER supplied by the VIN supply of the controller board.
JP3	AIN+ Amplifier Shutdown Selection	1 to 2: Shutdown pin tied high to enable amplifier.	3 to 4: Shutdown pin driven by AD4060/AD4062 DEV_EN signal on GP0. Allows prototyping with dynamic power scaling. 5 to 6: Shutdown pin tied low to disable amplifier.
JP4	AIN− Amplifier Shutdown Selection	1 to 2: Shutdown pin tied high to enable amplifier.	3 to 4: Shutdown pin driven by AD4060/AD4062 DEV_EN signal on GP0. Allows prototyping with dynamic power scaling. 5 to 6: Shutdown pin tied low to disable amplifier.
JP5	VREF_IN Source Selection	1 to 2: VREF_IN supplied by VSUPPLY.	3 to 4: VREF_IN supplied by +5V. Allows prototyping with different voltage references up to 3.3V. 5 to 6: No connect. Place the jumper in this position if powering VREF_IN from an external supply.
JP6	VREF Shutdown Selection	1: Shutdown pin tied high to enable voltage reference.	3: Shutdown pin connected to GPIO signal. Allows prototyping of dynamic power scaling of voltage reference during long periods without ADC activity.
JP7	VCC Source Selection	1: VCC supplied by VSUPPLY.	3: No connect. Place the jumper in this position if powering VCC from an external supply.
JP8	VDD Source Selection	1: VDD supplied by VSUPPLY.	3: No connect. Place the jumper in this position if powering VDD from an external supply.
JP9	VEE Source Selection	1: VEE tied to GND.	3: No connect. Place the jumper in this position if powering VEE from an external supply.
JP10	ADDR2 Source Selection	1: ADDR2 tied to GND.	3: ADDR2 set to VIO.
JP11	ADDR0 Source Selection	1: ADDR1 tied to GND.	3: ADDR1 set to VIO.
JP12	ADDR1 Source Selection	1: ADDR0 tied to GND.	3: ADDR0 set to VIO.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURE

Download the ACE evaluation software from the EVAL-AD4060-ARDZ or the EVAL-AD4062-ARDZ evaluation kit page. Install the software on a PC before using the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ kit. Download the AD4060/AD4062 ACE plugin from the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ product page or from the ACE plugin manager.

Perform the following steps to complete the installation process:

1. Install the ACE evaluation software.
2. Install the AD4060/AD4062 plugin. The ACE Quickstart page shows the plugin installation guide.

INSTALLING THE ACE EVALUATION SOFTWARE

To install the ACE evaluation software, take the following steps:

1. Download the ACE software to a Windows-based PC.
2. Double click the **ACEInstall.exe** file to begin the installation. By default, the ACE software is saved to the following location: **C:\Program Files (x86)\Analog Devices\ACE**.
3. A dialog box opens asking for permission to allow the program to make changes to the PC. Click **Yes** to start the installation process.
4. In the **ACE Setup** window, click **Next >** to continue the installation.

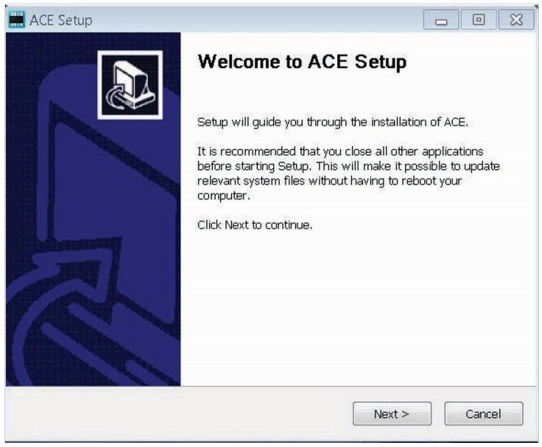

Figure 16. Evaluation Software Installation Confirmation

5. Read the software license agreement and click **I Agree**.
6. Click **Browse...** to choose the installation location and then click **Next >**.

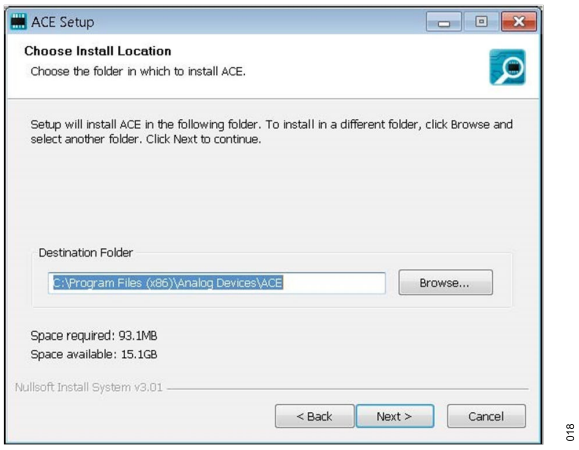

Figure 17. Choose Installation Location Window

7. The ACE software components to install are preselected. Click **Install** and wait for installation to complete.

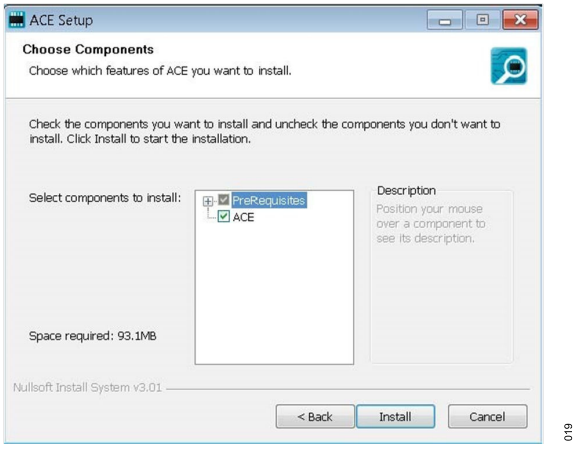

Figure 18. Choose ACE Installation Components Window

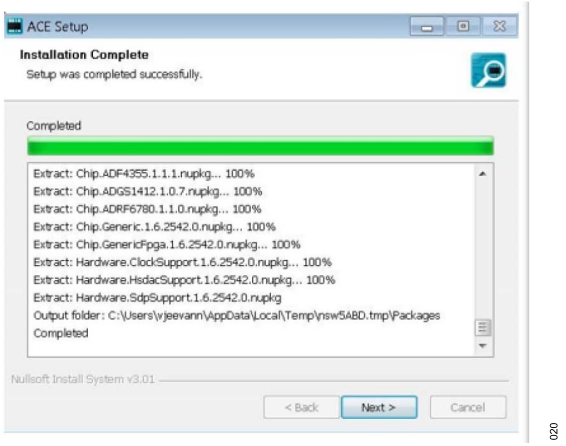

Figure 19. ACE Installation Progress Window

EVALUATION BOARD SOFTWARE

INSTALLING THE AD4060/AD4062 ACE PLUGIN

1. Download and install the ACE software tool from the ACE download page, as per the Installing the ACE Evaluation Software section. If ACE is already installed, make sure you have the latest version by using **Check For Updates** option in the ACE sidebar, as shown in Figure 20.

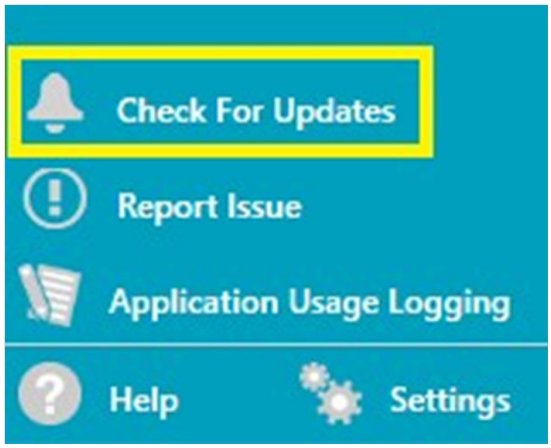

Figure 20. Check for Updates in the ACE Sidebar

2. Run the **ACE** software. Select **Plugin Manager** from the ACE sidebar to install the board plugin that supports the product evaluation board and select **Available Packages**, as shown in Figure 21. You can use the search field to help filter the list of boards to find the relevant one. An ACE quick start guide is available at ACE Quickstart - Using ACE and Installing Plugins.

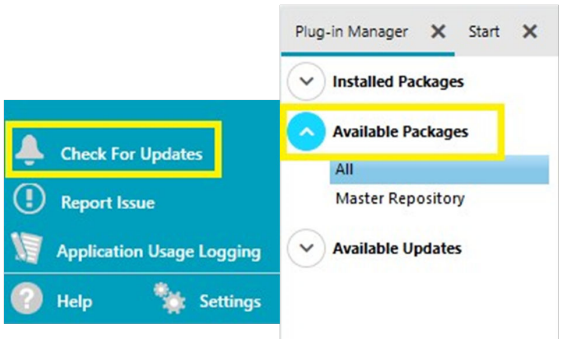

Figure 21. Plugin Manager Option in the ACE Sidebar

LAUNCHING THE SOFTWARE

To start the ACE evaluation software, open the Windows **Start** menu and click **Analog Devices > ACE**. The software window continues loading until the software recognizes the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ. When the software recognized the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ, the connected device will be displayed in the **Attached Hardware** menu as shown in Figure 22.

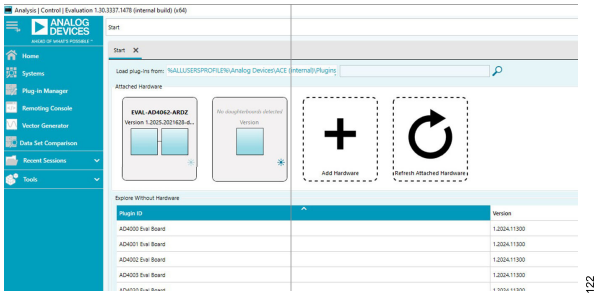

Figure 22. EVAL-AD4062-ARDZ in Attached Hardware

Double clicking on the EVAL-AD4062-ARDZ block in the attached hardware menu brings up the board view. The **Proceed to Documentation** button (as shown in Figure 23) navigates to the Embedded ACE plugin documentation which serves as a guide on using the EVAL-AD4060-ARDZ/EVAL-AD4062-ARDZ ACE plugin and collecting ADC data and analysis.

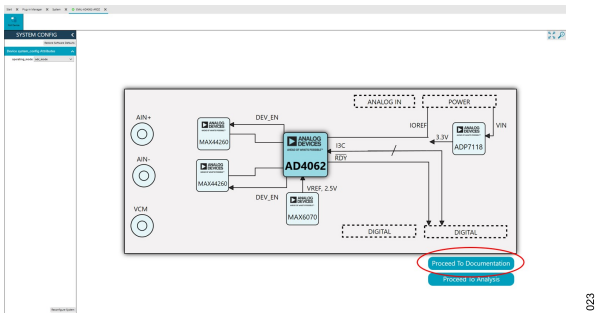

Figure 23. EVAL-AD4062-ARDZ Board View

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.