

Evaluating the AD3542R, 16-Bit, 16 MUPS, Dual Channel, Voltage Output DAC

FEATURES

- ▶ Full featured evaluation board for the [AD3542R](#)
- ▶ Selectable transimpedance gain with rotary switch
- ▶ Selectable transimpedance amplifier supplies
- ▶ On-board or external power supply
- ▶ On-board or external voltage reference
- ▶ Impedance matching options for different instruments
- ▶ Used with [SDP-H1](#) controller board

EVALUATION KIT CONTENTS

- ▶ EVAL-AD3542RFMCZ

HARDWARE REQUIRED

- ▶ SDP-H1 board, must be purchased separately

SOFTWARE REQUIRED

- ▶ [ACE](#) software
- ▶ **Board.AD35X2R** ACE plugin (automatically downloaded within ACE)

GENERAL DESCRIPTION

The EVAL-AD3542RFMCZ is an evaluation board for the AD3542R, a dual-channel, 16-bit fast precision digital-to-analog converter (DAC). The board allows testing all the output ranges of the DAC, waveform generation, power supply, and reference options.

The EVAL-AD3542RFMCZ interfaces to the USB port of a PC via a system demonstration platform (SDP-H1 board). The EVAL-AD3542RFMCZ can also be connected to a different controller board using the pin header connector at position P5.

This user guide covers the details of the configuration and operation of the EVAL-AD3542RFMCZ board and the associated ACE plugin. For additional information on the DAC operation, refer to the AD3542R data sheet.

ONLINE RESOURCES

- ▶ [Bill of materials and layout files](#)

EVALUATION BOARD PHOTOGRAPH

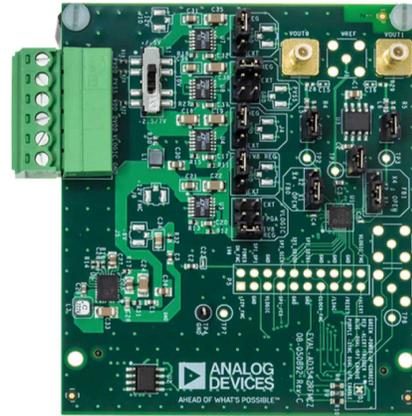


Figure 1. EVAL-AD3542RFMCZ, Top View



Figure 2. EVAL-AD3542RFMCZ, Bottom View

001

002

TABLE OF CONTENTS

Features.....	1	On-Board Connectors.....	6
Evaluation Kit Contents.....	1	LED Indicators.....	8
Hardware Required.....	1	DAC Output Range Selection.....	8
Software Required.....	1	Output Impedance Matching.....	8
General Description.....	1	ACE Plugin Description and Features.....	9
Online Resources.....	1	ACE Plugin Hierarchy.....	9
Evaluation Board Photograph.....	1	Board View.....	10
Evaluation Board Quick Start Procedure.....	3	Chip View.....	11
Installing the Software.....	3	Memory Map View.....	12
Connecting the Board.....	4	Waveform Generator View.....	13
Evaluation Board Hardware.....	5	Vector Generator View.....	15
Power Supplies.....	5	Generating a Waveform.....	16
Power Supply Configuration for		Unsupported Features in the Plugin.....	16
Transimpedance Amplifier.....	5	Evaluation Board Schematics.....	17
Link and Switch Options.....	5		

REVISION HISTORY

8/2024—Revision A: Initial Version

.....

EVALUATION BOARD QUICK START PROCEDURE

INSTALLING THE SOFTWARE

The EVAL-AD3542RFMCZ uses the analysis, control, evaluation (ACE) software with the **Board.AD35X2R** plugin for evaluation.

To install the software, take the following steps:

1. Download and run the latest version of the ACE installer. It installs the application and the necessary drivers for the **SDP-H1** controller board.
2. Click **Plug-in Manager** on the left-hand menu as shown in [Figure 3](#).

3. Go to **Available Packages**, select **Board.AD35X2R**, and click the **Install Selected** button at the bottom of the list. Once the plugin is installed, it moves to the **Installed Packages** section.
4. Click **Home** on the left-hand menu. If the EVAL-AD3542RFMCZ board is connected, it shows up in the **Attached Hardware** section as shown in [Figure 4](#). If you do not have an EVAL-AD3542RFMCZ board, you can still explore the functionality of the plugin by double clicking the desired board in the **Explore Without Hardware** list.

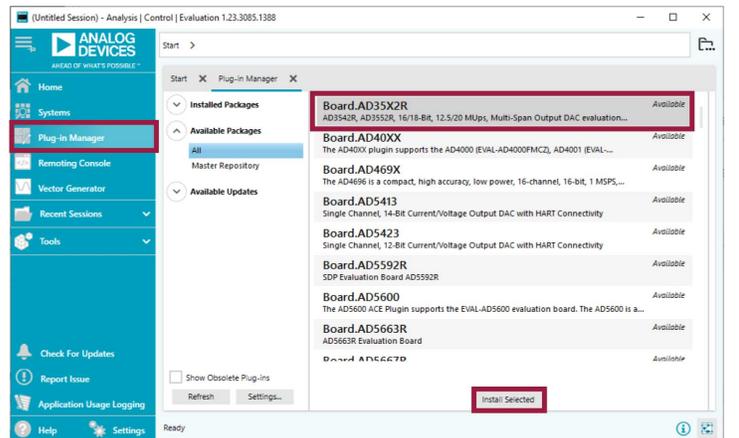


Figure 3. Plug-in Manager

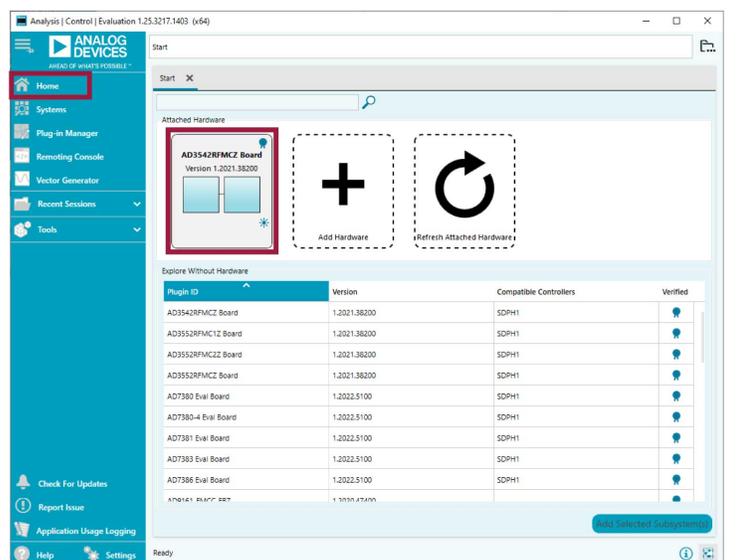


Figure 4. Start Tab

EVALUATION BOARD QUICK START PROCEDURE

CONNECTING THE BOARD

To set up the evaluation board, take the following steps:

1. Make sure that all the links and switches are set in the default positions listed in [Table 3](#).
2. Plug the EVAL-AD3542RFMCZ evaluation board on the [SDP-H1](#) controller board.
3. Connect the wall-plug brick power supply to the SDP-H1 DC jack and power from the AC network. The power LED on the SDP-H1 turns on green.
4. Connect the USB cable between the SDP-H1 board and the PC.
5. ACE must now be able to detect the board and show it in the **Attached Hardware** section, as shown in [Figure 4](#). Double click the **AD3542RFMCZ Board** icon to open the **Board View**, as seen in [Figure 8](#). The green LED DS3 turns on at this moment. The **Board View** shows the relevant parts included in the evaluation board, where the [AD3542R](#) chip is highlighted in darker blue.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-AD3542RFMCZ includes a complete power conversion solution to allow powering the evaluation board from the SDP-H1. The board includes a DC/DC converter LTC7149 to generate -7 V from the +12 V power provided by the SDP-H1. Low-dropout regulators (LDOs) LT3045 and LT3094 are used to generate the positive and negative supplies for the internal transimpedance amplifiers, which are selectable using the S1 switch. Additional LT3045 LDOs are used to generate 1.8 V and 5 V for the logic and the DAC core of the AD3542R, respectively. This power solution is configured with the default link settings shown in Table 3.

Alternatively, the board can be powered from a collection of external power supplies via the P3 connector. The assignment of the pins in the P3 connector is listed in Table 1.

Table 1. Pin Assignment on P3 Power Supply Connector

Pin Number	Signal	Description
1	EXT_PVDD	External positive supply for transconductance amplifiers. 4.7 V to 10.6 V.
2	EXT_PVSS	External negative supply for transconductance amplifiers. 0 V down to PVDD - 10.6 V.
3	EXT_VDD	External analog supply for AD3542R. 5 V ± 5%.
4	EXT_DVDD	External digital supply for AD3542R. 1.8 V ± 5%.
5	EXT_VLOGIC	External digital I/O supply for AD3542R. 1.1 V to 1.9 V.
6	GND	Ground.

The EVAL-AD3542RFMCZ also integrates an on-board 2.5 V, 2 ppm/°C analog reference ADR4525.

POWER SUPPLY CONFIGURATION FOR TRANSIMPEDANCE AMPLIFIER

The supply for the transimpedance amplifier integrated in the AD3542R must be adjusted depending on the selected output span using the S1 switch. Table 2 presents the three possible supply configurations. The correspondence with the output range is shown in the DAC Output Range Selection section.

Table 2. Transimpedance Amplifier Supply Options

S1 Position	Label	PVDD Voltage	PVSS Voltage
Left	+/-5 V	+5.2 V	-5.2 V
Middle	10 V	+10.2 V	-0.2 V
Right	-2.5 V/+7 V	+7.7 V	-2.7 V

Note: do not change the position of S1 while the board is powered up.

LINK AND SWITCH OPTIONS

The EVAL-AD3542RFMCZ board is delivered with the links and switches placed in the default positions listed in Table 3. This configuration is suitable for operating the board right out of the box. However, the S1, S2, and S3 switches, and the J_REF link may need to be adjusted depending on the configuration set in the registers of the AD3542R. Refer to Figure 5 to locate the position of links and connectors.

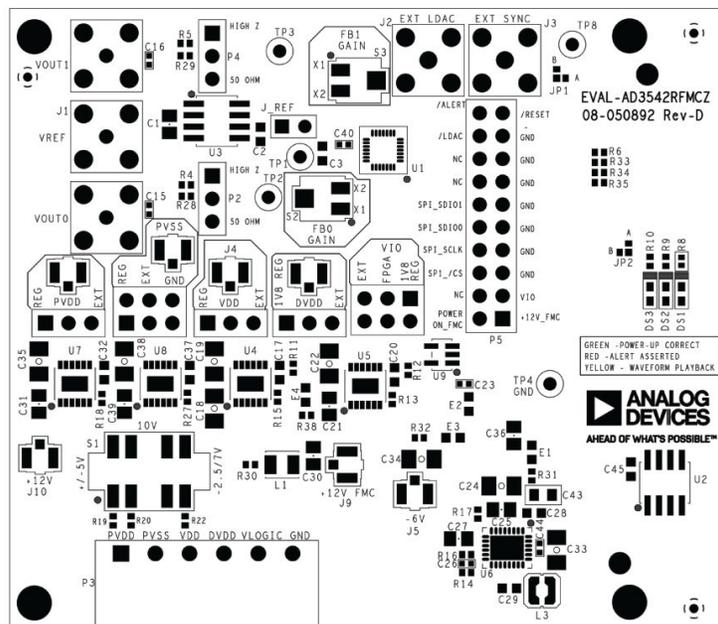


Figure 5. Board Layout

EVALUATION BOARD HARDWARE

Table 3. Link and Switch Options

Link/Switch	Silkscreen	Description	Default Position
S2	FB0 GAIN	This switch selects the gain of the transimpedance amplifier for Channel 0. The gains are labeled X1 and X2 which correspond to the multiplicative factor between them. The gain must be set in accordance to the desired output range listed in the DAC Output Range Selection section. The switch has two positions for X1 or X2 gains.	X1
S3	FB1 GAIN	This switch selects the gain of the transimpedance amplifier for Channel 1. The gains are labeled X1 and X2 which correspond to the multiplicative factor between them. The gain must be set in accordance to the desired output range listed in the DAC Output Range Selection section. The switch has two positions for X1 or X2 gains.	X1
P2	P2	This link configures the on-board matching pad to adapt to the impedance of the instrument connected on VOUT0. Set the link to HIGH Z if VOUT0 is connected to an instrument with high input impedance using a coaxial cable. Set the link to 50 OHM if VOUT0 is connected to an instrument with 50 Ω input impedance.	HIGH Z
P4	P4	This link configures the on-board matching pad to adapt to the impedance of the instrument connected on VOUT1. Set the link to HIGH Z if VOUT1 is connected to an instrument with high input impedance using a coaxial cable. Set the link to 50 OHM if VOUT1 is connected to an instrument with 50 Ω input impedance.	HIGH Z
J_REF	J_REF	This link allows connecting the on-board reference to the AD3542R . This link must be removed if an external reference is provided via the J1 connector (VREF) or if the internal reference is output to the VREF pin.	Inserted
J_PVDD	PVDD	This link selects the positive voltage supply for the transimpedance amplifier. REG selects the supply from the on-board LDO. EXT selects the supply provided externally on the P3 connector.	REG
J_PVSS	PVSS	This link selects the negative voltage supply for the transimpedance amplifier. REG selects the supply from the on-board LDO. EXT selects the supply provided externally on the P3 connector. GND sets the supply rail to ground.	REG
J_VDD	VDD	This link selects the voltage supply for the analog section of the AD3542R . REG selects the 5 V supply from the on-board LDO regulator. EXT selects the supply provided externally on the P3 connector.	REG
J_DVDD	DVDD	This link selects the voltage supply for the digital section of the AD3542R . 1V8 REG selects the supply from the on-board LDO regulator. FPGA selects the supply provided from the SDP-H1 board, the same as used in the FPGA IO pins. EXT selects the supply provided externally on the P3 connector.	1V8 REG
J_VIO	VIO	This link selects the voltage supply for the AD3542R IO pins. 1V8 REG selects the supply for the on-board LDO regulator. FPGA selects the supply provided from the SDP-H1 board, the same as used in the FPGA IO pins. EXT selects the supply provided externally on the P3 connector.	1V8 REG
S1	S1	This switch selects one of the following combinations for PVDD and PVSS: Left: PVDD = +5.2 V, PVSS = -5.2 V Middle: PVDD = +10.2 V, PVSS = -0.2 V Right: PVDD = +7.7 V, PVSS = -2.7 V	Left +/- 5 V

ON-BOARD CONNECTORS

Table 4 shows the list of connectors available on the EVAL-AD3542RFMCZ and their corresponding use.

Table 4. List of Connectors

Connector	Silkscreen	Signal Name	Function
J1	VREF	VREF	Reference voltage input/output. This connector can be used to provide an external reference voltage to the AD3542R or to monitor the reference generated by the ADR4525 or the AD3542R .
J2	EXT LDAC	EXT_LDAC	Input for an external LDAC signal. This connector is terminated to 50 Ω . The voltage of the signal must not exceed V_{LOGIC} voltage by more than 0.3 V.
J3	EXT SYNC	EXT_SYNC	Input for an external synchronization signal provided to the field-programmable gate array (FPGA). This connector is terminated to 50 Ω . The voltage of the signal must not exceed the FPGA I/O voltage by more than 0.3 V.
VOUT0	VOUT0	C_VOUT0	Voltage output of DAC Channel 0.
VOUT1	VOUT1	C_VOUT1	Voltage output of DAC Channel 1.
P1	P1	Multiple ¹	FPGA mezzanine card (FMC) connector carrying the digital signals between the evaluation board and the controller board.
P3	P3	Multiple ²	External supply connector. Pin assignment given in Table 1 .
P5	P5	Multiple ³	Custom controller interface. This connector is used to control the AD3542R with a controller different from the SDP-H1 . The pin assignment is listed in Table 5 . The pin header is not assembled by default so that the holes can be used as test points for the digital signals.

¹ See the [Evaluation Board Schematics](#) section.

EVALUATION BOARD HARDWARE

² See Table 1.

³ See Table 5.

The P5 connector is used to connect an external controller when the SDP-H1 is not present. This connector grants access to all the digital signals of the AD3542R and some board supplies and control lines.

Table 5. Pin Assignment on P5 Connector

Pin Number	Connector Label	Function
1	+12V_FMC	External 12 V power supply. Use this pin to supply the EVAL-AD3542RFMCZ board when using a controller different from the SDP-H1.
2	POWER_ON_FMC	Enable signal for the on-board regulators. This pin is used to turn on the LDOs and DC/DC converters. Set a voltage higher than 1.24 V to turn on. If the controller is not driving this signal, it must be set manually to use the board.
3	VIO	Voltage supply used for the AD3542R I/O pins. If this pin is used to supply V_{LOGIC} , remove the VIO link or set it to EXT.
4	NC	Not connected.
5	GND	Ground.
6	SPI_CS ¹	Serial peripheral interface (SPI) chip select signal.
7	GND	Ground.
8	SPI_SCLK ¹	SPI clock signal.
9	GND	Ground.
10	SPI_SDIO0 ¹	Serial data input (SDI)/main out/subordinate in signal in classic SPI mode or SDIO0 signal in dual SPI mode.
11	GND	Ground.
12	SPI_SDIO1 ¹	Serial data output (SDO)/main in/subordinate out signal in classic SPI mode or SDIO1 signal in dual SPI mode.
13	GND	Ground.
14	NC	Not connected.
15	GND	Ground.
16	NC	Not connected.
17	GND	Ground.
18	$\overline{\text{LDAC}}$ ¹	$\overline{\text{LDAC}}$ signal.
19	$\overline{\text{RESET}}$ ¹	$\overline{\text{RESET}}$ signal.
20	$\overline{\text{ALERT}}$ ¹	$\overline{\text{ALERT}}$ signal.

¹ The voltage on this pin must not exceed V_{LOGIC} voltage by more than 0.3 V.

The board includes several test points to access relevant signals. Only TP4 has the test ring assembled. The list is given in Table 6.

Table 6. List of Test Points

Test Point	Signal	Description
TP1	VREF	Reference voltage for the AD3542R (internal, on-board, or external)
TP2	VOUT0	Voltage output of DAC Channel 0
TP3	VOUT1	Voltage output of DAC Channel 1
TP4	GND	Ground
TP8	EXT_SYNC	External synchronization signal.

EVALUATION BOARD HARDWARE

LED INDICATORS

The EVAL-AD3542RFMCZ has three LED indicators as follows:

- ▶ DS1: this yellow LED turns on when the controller starts a waveform playback in streaming mode. This LED is controlled from a general-purpose input/output (GPIO) on connector P1, Pin H13. Therefore, this functionality depends on the software and the controller used with the evaluation board.
- ▶ DS2: this red LED turns on when the ALERT pin is asserted in the AD3542R. This LED can also be controlled from a GPIO if the link JP2 is changed to position B.
- ▶ DS3: this green LED turns on when both AV_{DD} and DV_{DD} are powered up at 5 V and 1.8 V, respectively.

DAC OUTPUT RANGE SELECTION

The selection of the output range requires a combination of register configurations and a given transimpedance gain. The supply of the transimpedance amplifier must be adjusted accordingly. The gains and supplies corresponding to each output range are listed in Table 7. See the AD3542R data sheet for more details on output range configuration.

Table 7. Transimpedance Gain Setting

CHx_OUTPUT_RANGE_S EL Field Value	Output Range	Transimpedance Gain Setting	S1 setting
000	0 V to 2.5 V	X1	Any
001	0 V to 5 V	X1	Any
010	0 V to 10 V	X2	10 V
011	-5 V to +5 V	X2	+/- 5V
100	-2.5 V to 7.5 V	X2	-2.5/7 V

OUTPUT IMPEDANCE MATCHING

The AD3542R is a fast precision DAC that settles much faster than traditional precision DACs. At this speed, transmission line effects on the cable cannot be neglected. The board implements an impedance matching network with two configurations selectable using the P2 and P4 links for Channel 0 and Channel 1, respectively. The diagram of this network is shown in Figure 6.

- ▶ HIGH Z option provides impedance matching on the source side. This configuration sets a 52.3 Ω resistor in series with the output of the amplifier. This resistor provides some return loss to attenuate reflected waveforms originated on the high-impedance end of the coaxial cable. It also provides isolation from the capacitance of the cable to prevent the oscillation of the high-speed amplifier. This series resistor introduces a DC error of 50 ppm if the load is an oscilloscope, and 5 ppm if the load is a multimeter.
- ▶ 50 OHM option provides impedance matching when the load at the other end of the cable is 50 Ω . This configuration offers optimal signal transmission over a wide frequency band, but it is not for free. The matching network introduces an attenuation factor of 39.18 corresponding to 31.86 dB.

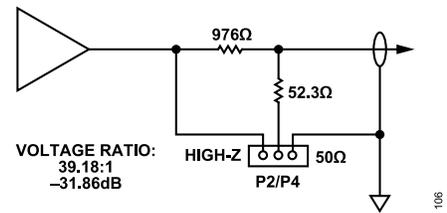


Figure 6. Impedance Matching Network

Some recommendations are given for the following different types of measurements:

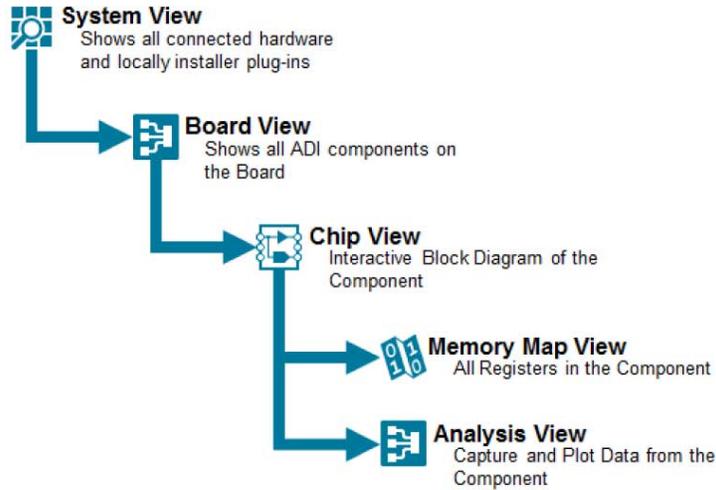
- ▶ DC measurements: it is recommended to connect the multimeter using a coaxial cable to minimize noise and interference. The matching network must be set to HIGH Z mode to obtain the highest SNR. For long-term measurements, it is recommended to cover the evaluation board with a cardboard box to prevent air flow. Do not cover the SDP-H1 controller because its power dissipation is high.
- ▶ Step response measurements: it is recommended to connect the oscilloscope using a coaxial cable with 50 Ω impedance. The matching network must be set to 50 OHM and the oscilloscope input configured to 50 Ω . Use \overline{LDAC} or \overline{CS} to trigger the oscilloscope and set the acquisition mode to averaging to reduce noise and be able to measure settling time accurately. Passive probes are not recommended for settling time because their compensation circuits alter the step response.
- ▶ Noise measurements: noise is so low that it is only visible in the HIGH Z configuration. An instrument with 50 Ω input impedance may be connected as long as it is AC-coupled. Note that the noise spectral density depends on the load impedance. Therefore, using a 50 Ω instrument results in a lower voltage than using a high impedance instrument.
- ▶ Glitch amplitude: the glitch is so small that it is only visible in the HIGH Z configuration. It is recommended to use an oscilloscope or a digitizer with 12- to 16-bit resolution, AC coupling, and the maximum vertical resolution. Use \overline{LDAC} or \overline{CS} to trigger the oscilloscope and set the acquisition mode to averaging to distinguish the glitch from the noise.
- ▶ THD and SFDR: THD at low frequency can be measured using a digitizer or an audio analyzer. In this case, the matching network must be set to HIGH Z because these instruments are high impedance. For higher frequencies, a spectrum analyzer is needed. In this case, the matching network must be set to 50 OHM. Most spectrum analyzers do not have enough linearity to measure the harmonics of the AD3542R reliably. Therefore, it is recommended to use high-pass filters to attenuate the fundamental tone. Alternatively, the 20-bit fast precision ADC AD4080 can be used to measure THD at high frequency and high impedance.

ACE PLUGIN DESCRIPTION AND FEATURES

ACE PLUGIN HIERARCHY

ACE has several views to control different aspects of the DAC. When a view is first opened, it creates a new tab at the top of the main window. The AD3542R plugin has a **Board View**, a **Chip View**, a **Memory Map View**, a **Waveform Generator View**, and a

Vector Generator View. Figure 7 shows the hierarchical relation between these views. For additional information, refer to the user manual that is accessible from the help panel displayed when clicking the **Help** button on the lower left angle of the application. There is also an [ACE Wiki](#) with additional information.



005

Figure 7. ACE Plugin Hierarchy

ACE PLUGIN DESCRIPTION AND FEATURES

BOARD VIEW

The **Board View** displays a simplified diagram of the evaluation board including some relevant connectors and the interconnection between chips, as seen in [Figure 8](#). Analog Devices, Inc., chips are shown with their part number and the **AD3542R** is highlighted in darker blue.

The actions that can be performed at this level are displayed as buttons at the top of the main window, as seen in [Figure 9](#).

- ▶ **Poll Device:** this action is performed automatically every second to verify that the evaluation board is connected to the system. The button allows turning on or off this feature.
- ▶ **Reset Board:** this action performs a power cycle on the evaluation board, bringing everything back to default.

To open the **Chip View**, double click the AD3542R block.

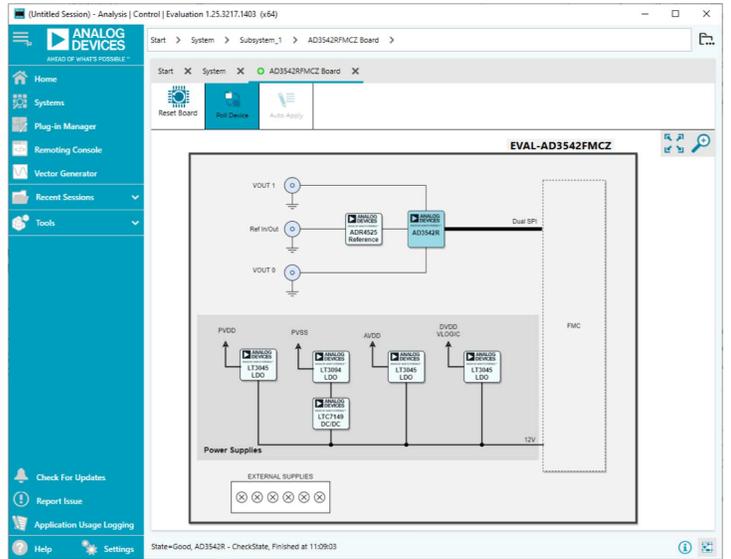


Figure 8. AD3542R Board View

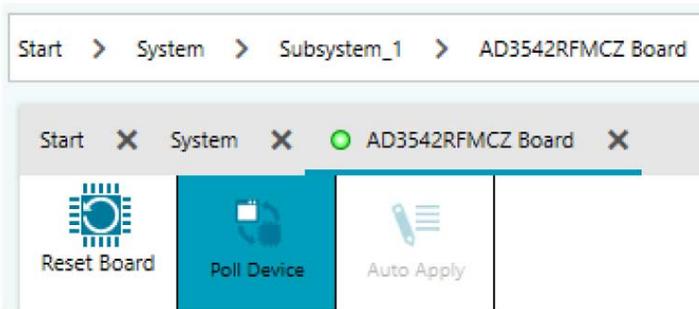


Figure 9. AD3542R Board View Buttons

ACE PLUGIN DESCRIPTION AND FEATURES

CHIP VIEW

The **Chip View** displays a simplified internal diagram of the chip showing the interface logic, the DAC cores, the precision feedback resistors, and the relevant pins for those blocks. This view contains the following three interactive areas, as depicted in [Figure 10](#):

- ▶ Button list (Label 1): these buttons perform the following actions on the chip:
 - ▶ **Apply Changes**: changes in the values of the registers are recorded in a cached copy kept on the PC memory. When the **Apply Changes** button is pressed, only the registers that were changed are updated in the [AD3542R](#).
 - ▶ **Read All**: this button reads all the registers from the AD3542R and updates the cached copy in the PC memory, displaying the values in the corresponding fields.
 - ▶ **Reset Chip**: this button resets the AD3542R but not the board. All registers are cleared to default values and ACE reads them back to keep the cached copy synchronized.
 - ▶ **Diff**: this button reads the registers of the AD3542R and compares their value to the cached copy, highlighting in bold those that are different.

- ▶ **Software Defaults**: this button loads the software default values in the cached copy without copying the values to the AD3542R.
- ▶ **Memory Map Side-By-Side**: this button opens a new window besides the chip view containing the list of the AD3542R registers.
- ▶ DAC registers (Label 2): each DAC symbol contains an editable field where the hexadecimal code can be written to the DAC output register. This allows performing a static update of the DAC. After writing the value, the **Apply Changes** button must be pressed to update the DAC output.
- ▶ Shortcuts to other views (Label 3): there are two buttons on the lower right corner to access the **Register Map View** and the **Waveform Generator View**. The use of these panels is explained in the [Memory Map View](#) section and the [Generating a Waveform](#) section.

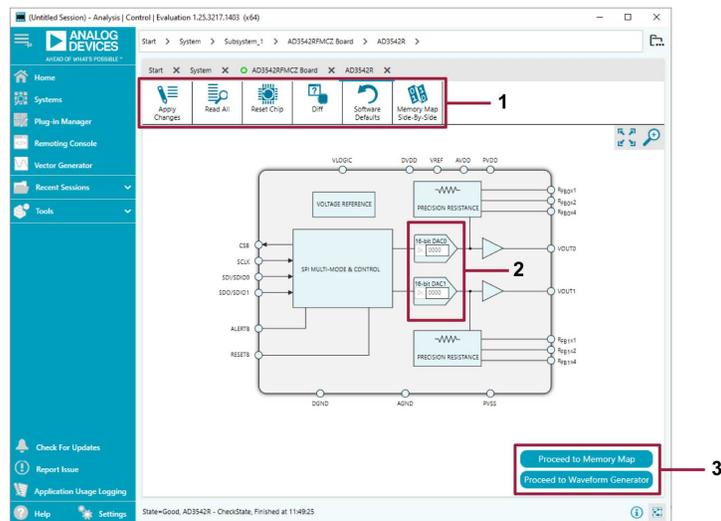


Figure 10. Chip View

ACE PLUGIN DESCRIPTION AND FEATURES

MEMORY MAP VIEW

The **Memory Map View** displays the entire configuration space of the AD3542R. The configuration space can be displayed as a list of registers or as a list of bit fields. The application allows sorting by any of the column categories or searching by register name or field name. Registers can be displayed collapsed or expanded into its bit fields, as shown in [Figure 11](#).

This view has the following interactive elements:

- ▶ Button list (Label 1): these buttons perform the following actions:
 - ▶ **Apply Changes**: this button writes all the registers that have been changed since the last update.
 - ▶ **Apply Selected**: this button writes only the register or bit field that is selected in the list.
 - ▶ **Read All**: this button forces the reading of all the AD3542R registers and the update of the cached copy.
 - ▶ **Read Selected**: this button reads only the register or bit field that is selected and updates its value in the cached copy.
 - ▶ **Reset Chip**: this button resets the AD3542R and forces the reading of all registers to update the cached copy.
 - ▶ **Diff**: this button reads the registers of the AD3542R and compares them with the cached copy, highlighting in bold those that have any difference.
- ▶ **Software Defaults**: this button loads the software default values in the cached copy without copying the values to the AD3542R.
- ▶ **Export**: this button exports the list of registers and their values to a CSV file. This feature is useful to generate the configuration file for a given application avoiding human error.
- ▶ **Import**: this button allows reading a CSV file containing the register values.
- ▶ **Chip View Side-by-Side**: this button displays the chip view by the side of the register map.
- ▶ **Show Bitfields/Show Registers**: this button toggles presentation mode as register list or bit field list.
- ▶ Register value (Label 2): this field allows editing the entire register value in hexadecimal (left side) or toggling the bits one by one (right side). Modified registers are highlighted in bold.
- ▶ Bit field values (Label 3): registers can be expanded into their bit fields and each bit can be edited individually by clicking on it to toggle its value. Modified registers are highlighted in bold.

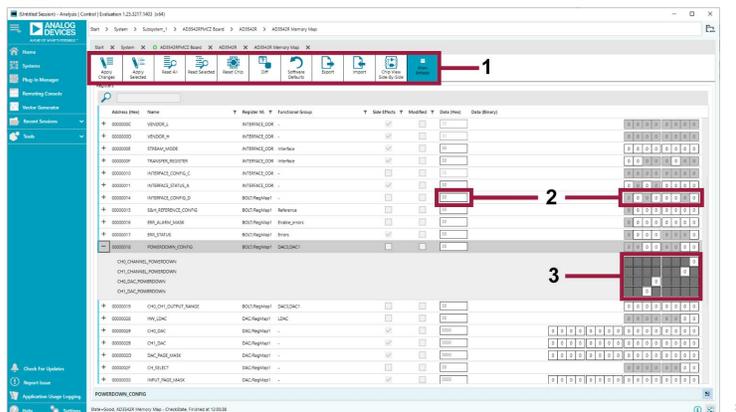


Figure 11. AD3542R Memory Map View

ACE PLUGIN DESCRIPTION AND FEATURES

WAVEFORM GENERATOR VIEW

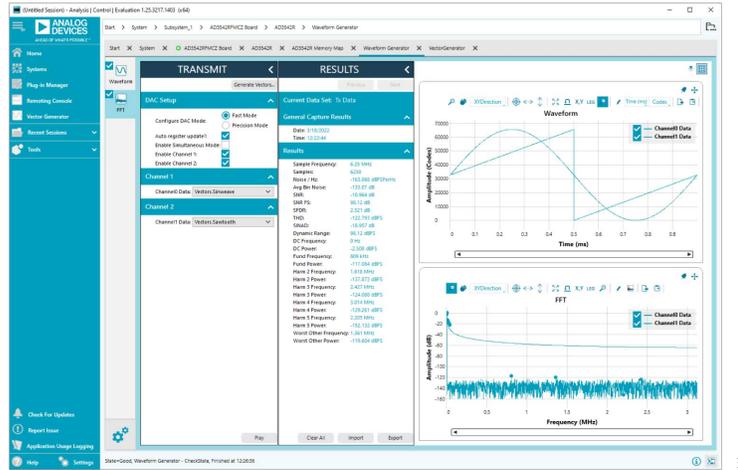


Figure 12. Waveform Generator View

The **Waveform Generator** view allows assigning vectors to the channels and starting or stopping waveform generation. A screenshot of this view is given in [Figure 12](#).

The operation mode of the **AD3542R** and the assignment of the waveforms is controlled from the **Transmit** pane that contains the following controls:

- ▶ **Generate Vectors...**: this button opens the **Vector Generator View** where waveforms can be defined, scaled, loaded, or exported. The use of this generator is covered in the [Vector Generator View](#) section.
- ▶ **Configure DAC Mode**: radio buttons allow selecting **Fast Mode** that uses 16-bit data word or **Precision Mode** that uses 24-bit word data. The same mode is used for both DAC channels when operated simultaneously.
- ▶ **Auto register update?**: this feature automatically configures the interface registers to operate in streaming mode with the highest possible update rate. If this box is not checked, configuration must be made manually on the **AD3542R Memory Map**. The settings are described at the end of this section.
- ▶ **Enable Simultaneous Mode**: this checkbox allows playing the same samples on both channels. Data is written to the DAC page register. Therefore, it maintains the same update rate as for a single channel. When this box is checked, the waveform is selected in the **Simultaneous Update** menu as seen in [Figure 14](#).
- ▶ **Enable Channel 1/Enable Channel 2**: these checkboxes allow enabling channels individually. When both channels are enabled, each one can play a different waveform, as seen in [Figure 13](#). The update rate depends on the DAC mode and the update mode. All the combinations are shown in [Table 8](#).
- ▶ **Play Button**: this button starts and stops the waveform playback. The status of the playback is displayed on the EVAL-AD3542RFMCZ by turning the yellow DS2 LED on.

Table 8. Update Rate Combinations

Mode	Fast Mode (16-bit)	Precision Mode (24-bit)
Dual Channel Mode	6.25 MUPS	4.16 MUPS
Single Channel/ Simultaneous Mode	12.5 MUPS	8.33 MUPS

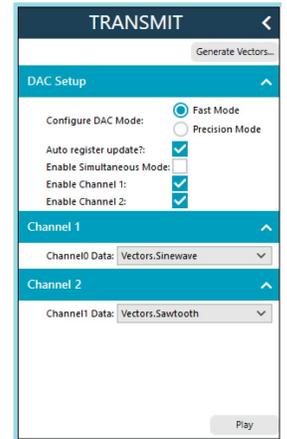


Figure 13. Waveform Generation in Dual Mode

ACE PLUGIN DESCRIPTION AND FEATURES

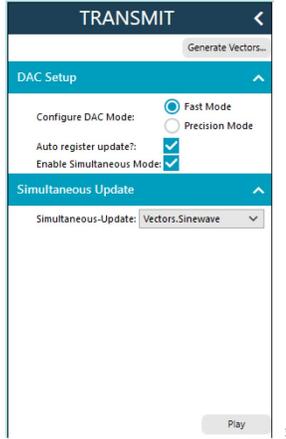


Figure 14. Waveform Generation in Simultaneous Mode

Manual Register Configuration for Streaming Mode

If the **Auto register update?** (Figure 12) checkbox is not checked, the streaming mode parameters must be configured manually in the Memory Map View (Figure 11) before pressing the **Play** button. The following registers must be set:

- ▶ **STREAM_MODE** (0x0E): length value must be set according to Table 9.
- ▶ **TRANSFER_REGISTER** (0x0F): set **STREAM_LENGTH_KEEP_VALUE** bit to 1.
- ▶ **INTERFACE_CONFIG_D** (0x14): set **SPI_CONFIG_DDR** bit to 1.

Table 9. Stream Mode Length Values

Mode	Fast Mode (16-bit)	Precision Mode (24-bit)
Single Channel/ Simultaneous Mode	2	3
Dual Channel Mode	4	6

ACE PLUGIN DESCRIPTION AND FEATURES

VECTOR GENERATOR VIEW

The **Vector Generator View** allows defining or loading waveforms that can later be assigned to the DAC channels. Waveforms are identified by name. The generator automatically adapts the sample rate based on the operating mode and the number of DAC channels enabled. A snapshot of this view is presented in [Figure 15](#).

The **Vector Generator** tool is composed of the following sections:

- ▶ **Predefined waveforms (Label 1):** the generator has several predefined waveforms: DC, single tone, square, triangle, sawtooth, chirp, noise, and multi-tone. Clicking the + button adds this waveform to the **Generate** panel where it can be customized.
- ▶ **Waveforms from File (Label 2):** the generator can load waveforms from **File** in three different file formats: text file vector, hexadecimal file vector, or ACE file vector. Refer to the ACE user manual for further details on the file formats. When loading a waveform all the samples are played irrespective of the update rate. Therefore, the waveform files must be generated for a specific update rate.
- ▶ **First waveform parameters (Label 3):** every waveform has a set of parameters that can be customized as follows:
 - ▶ **Vector Name:** specify a name in this field to identify the waveforms in the **Waveform Generator View**.
 - ▶ **Desired Frequency:** specify the repetition frequency of the waveform. The value is assumed to be in Hz if no unit

is specified. If the unit is specified, it must adhere to the standard capitalization (for example, kHz, not khz).

- ▶ **Attenuation:** all waveforms are generated at full scale by default. Attenuation can be used to reduce the signal amplitude keeping the offset constant at midscale. Amplitude is scaled by $10^{-Att/20}$.
 - ▶ **Relative Phase:** specify the phase offset relative to the start of the waveform record.
 - ▶ **Preview:** pressing this button displays the waveform in the time-domain and its fast Fourier transform (FFT) in the frequency-domain window, if present.
 - ▶ **Copy:** pressing this button duplicates the waveform entry in the **Generate** pane.
 - ▶ **Export:** pressing this button allows exporting the waveform as a text file containing decimal numbers.
- ▶ **Second waveform parameters (Label 4):** if a second waveform is added, it shows up stacked in the **Generate** pane under the first waveform. The same parameters are applicable.
 - ▶ **Time-domain waveform preview (Label 5):** a preview of the selected waveform is displayed in this window. Only one waveform is displayed at a time. The plot window allows zooming, panning, and measuring on the waveform.
 - ▶ **Waveform FFT (Label 6):** the frequency-domain analysis of the selected waveform is displayed in this window. The plot window allows zooming, panning, and measuring on the spectrum.

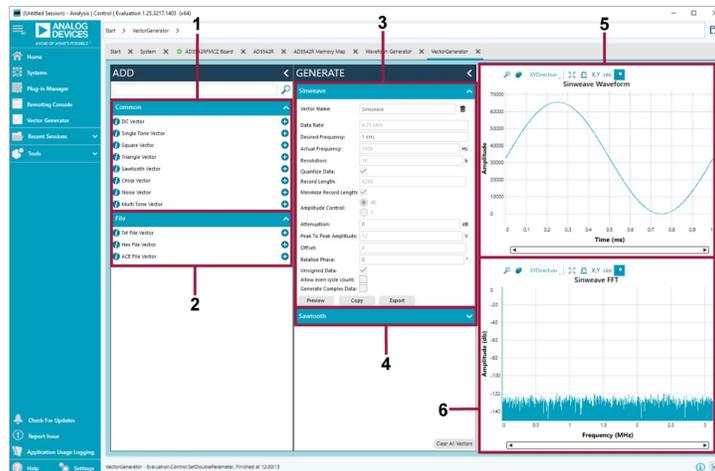


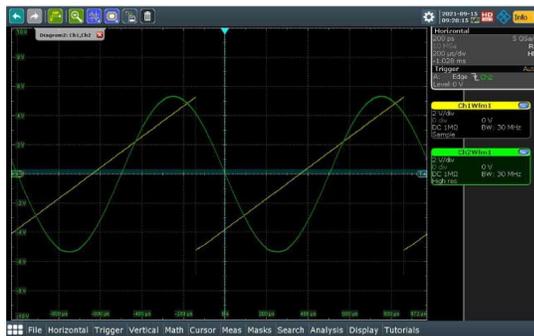
Figure 15. Vector Generator View

ACE PLUGIN DESCRIPTION AND FEATURES

GENERATING A WAVEFORM

Follow these steps to produce a dual waveform playback on the EVAL-AD3542RFMCZ evaluation board:

1. From the start page, double click on the board icon to open the **Board View**.
2. Double click on the AD3542R block to open the **Chip View**.
3. Click the **Proceed to Memory Map** button to open the **Memory Map View**.
4. Go to **CH0_CH1_OUTPUT_RANGE** register and set the desired output range (0x33 in this example). Refer to [Table 7](#) for the possible values of this register. Then, click **Apply All** to force the register update.
5. Click **Vector Generator** on the left-hand panel to open the **Vector Generator View**.
6. Follow the instructions given in the [Vector Generator View](#) section to create a 1 kHz sinewave and a 1 kHz sawtooth.
7. Follow the shortcuts in the gray bar at the top of the window to go back to the **Chip View**. Then, click the **Proceed to Waveform Generator** button to open the **Waveform Generator View**.
8. Select **Fast Mode**, **Enable Channel 1**, and **Enable Channel 2**. Then, unfold the Channel 1 and Channel 2 sections to select each of the waveforms you created. Finally, click the **Play** button.
9. The DS2 LED on the EVAL-AD3542RFMCZ turns on yellow and the playback starts. The waveforms must look like the ones shown in [Figure 16](#) in the oscilloscope.



014

Figure 16. Simultaneous Waveform Output

UNSUPPORTED FEATURES IN THE PLUGIN

The ACE plugin does not support all the features of the [AD3542R](#) and the EVAL-AD3542RFMCZ. The following are the nonsupported features:

- ▶ DAC output range selection and customization: there is no visual control to change this. The configuration must be entered manually in the **Memory Map View**.
- ▶ CRC checking.
- ▶ Amplitude and offset control in waveform generation: waveform scaling is only possible using the **Attenuation** field in dB. Offset is fixed to midscale.
- ▶ Using the $\overline{\text{LDAC}}$ line to update the DAC output: the FPGA writes the DAC register directly. In streaming mode, DAC Channel 1 is delayed from DAC Channel 0 by four clock cycles.
- ▶ $\overline{\text{ALERT}}$ pin monitoring, error status readback, and on-screen reporting: the alert condition is displayed visually using an LED, but the application does not report it.
- ▶ External triggering of waveform playback.

EVALUATION BOARD SCHEMATICS

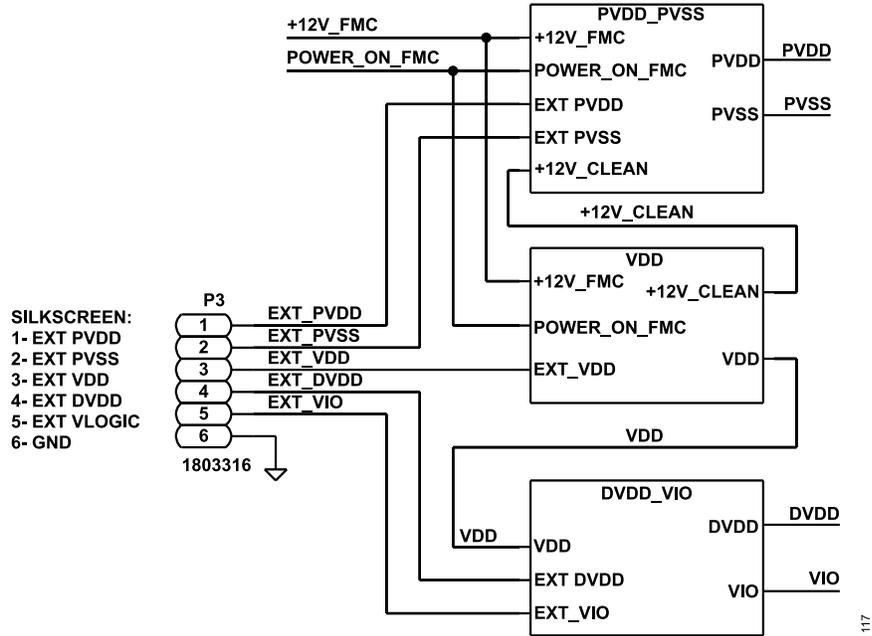


Figure 17. Power Supply Tree

EVALUATION BOARD SCHEMATICS

510

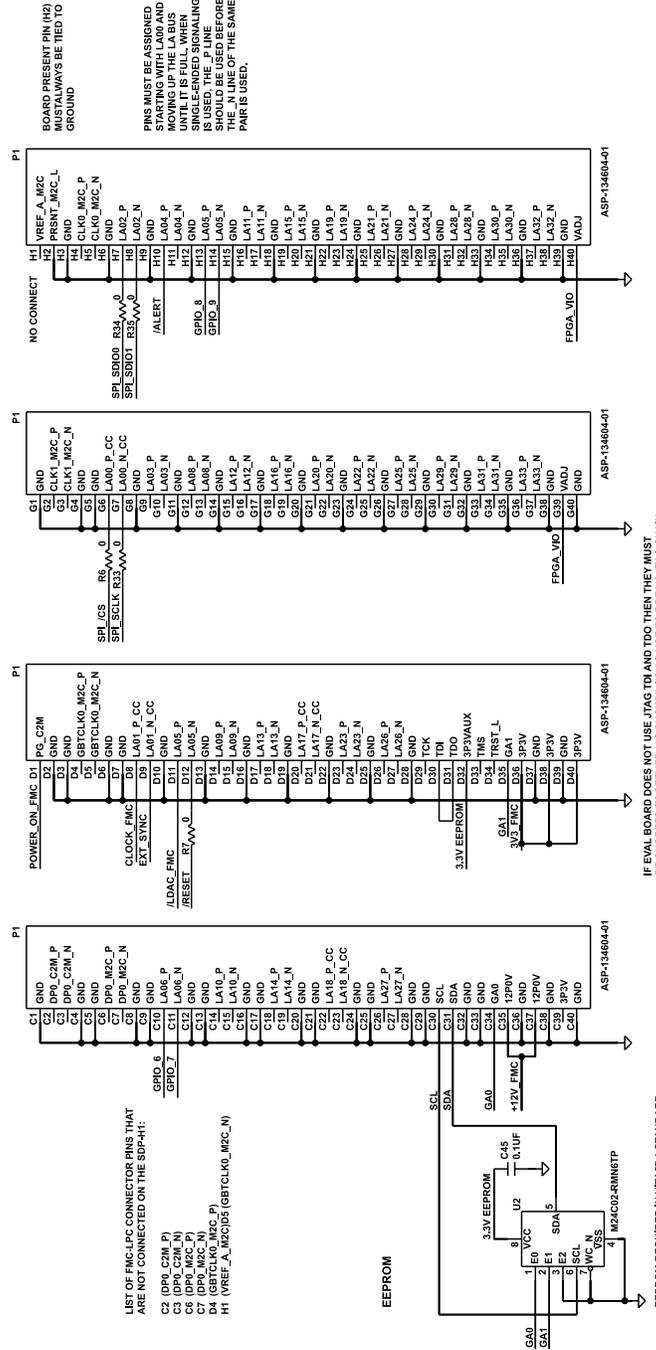


Figure 18. FMC Connector and EEPROM

EVALUATION BOARD SCHEMATICS

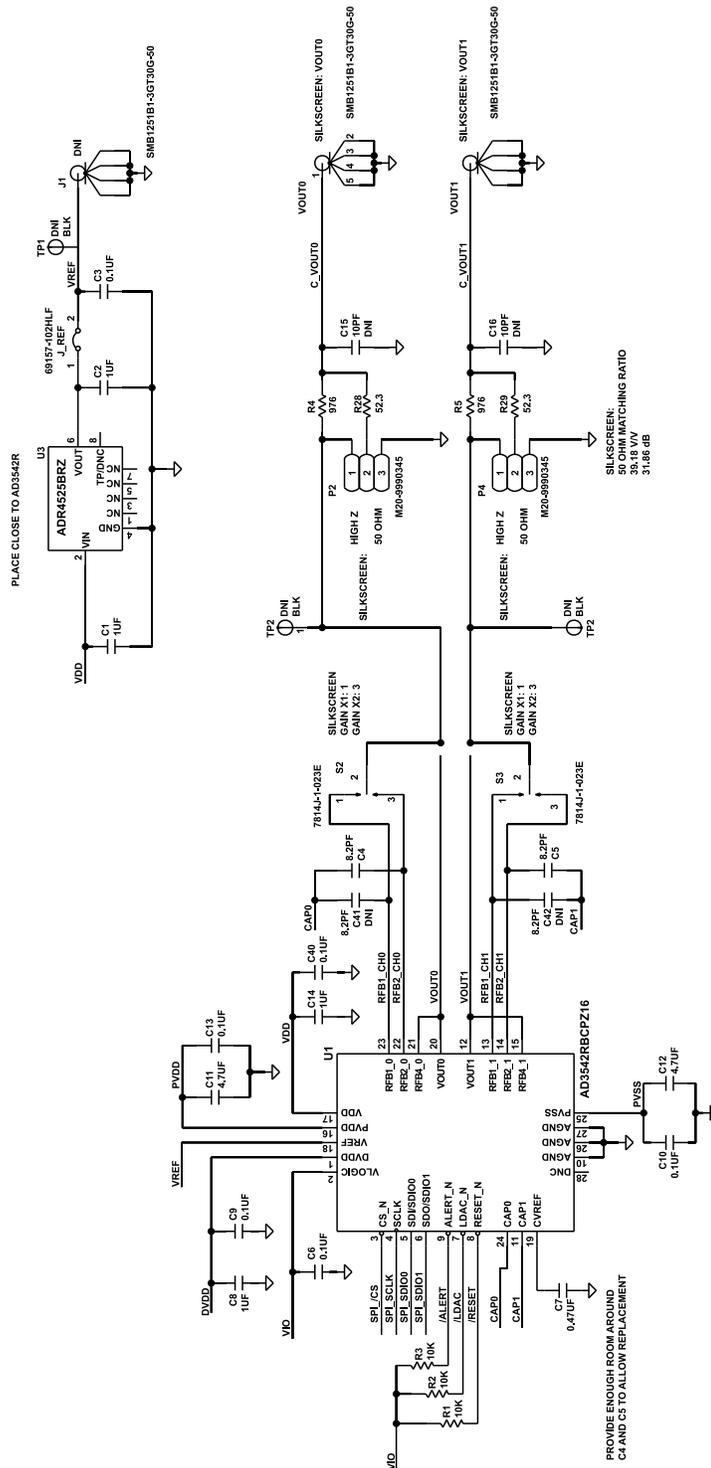


Figure 19. AD3542R and Reference

EVALUATION BOARD SCHEMATICS

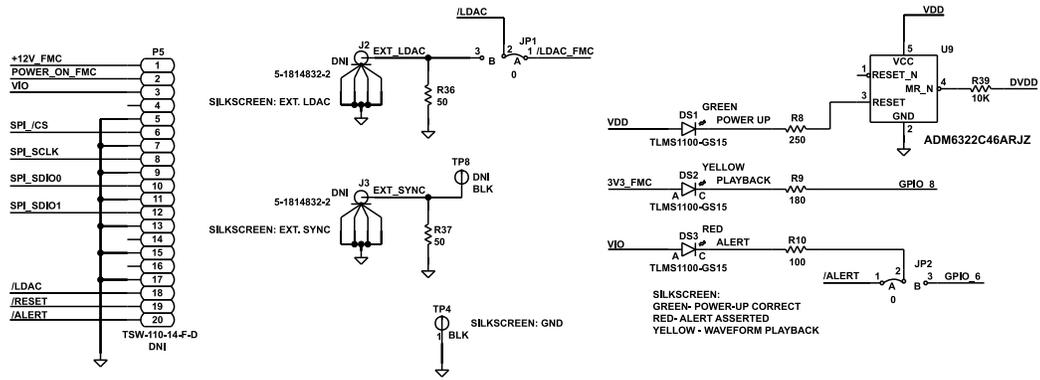


Figure 20. Digital Connectors and LEDs

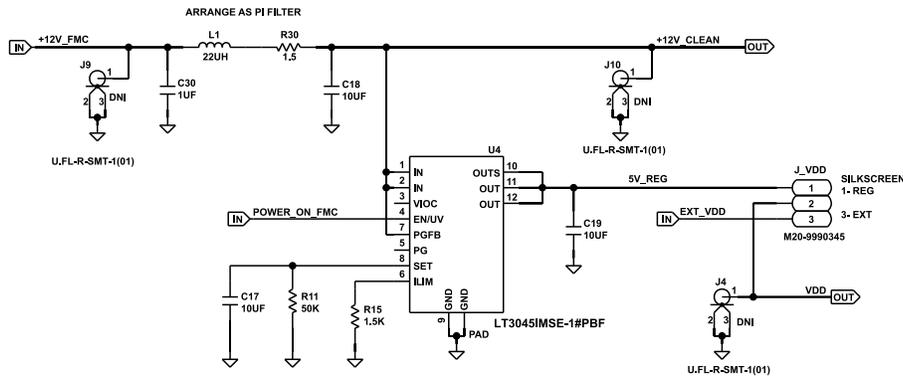


Figure 21. AVDD LDO

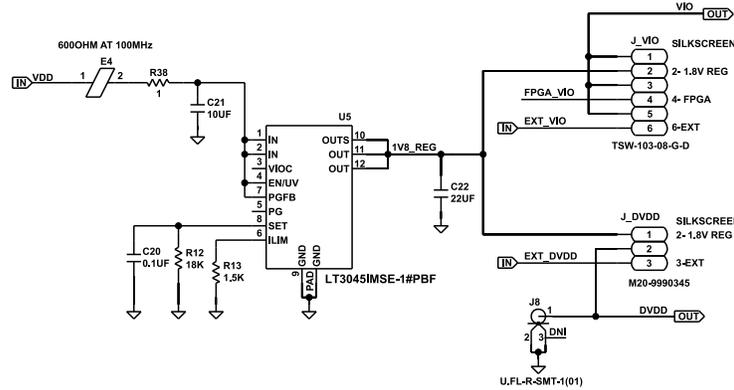


Figure 22. DVDD and VIO LDO

EVALUATION BOARD SCHEMATICS

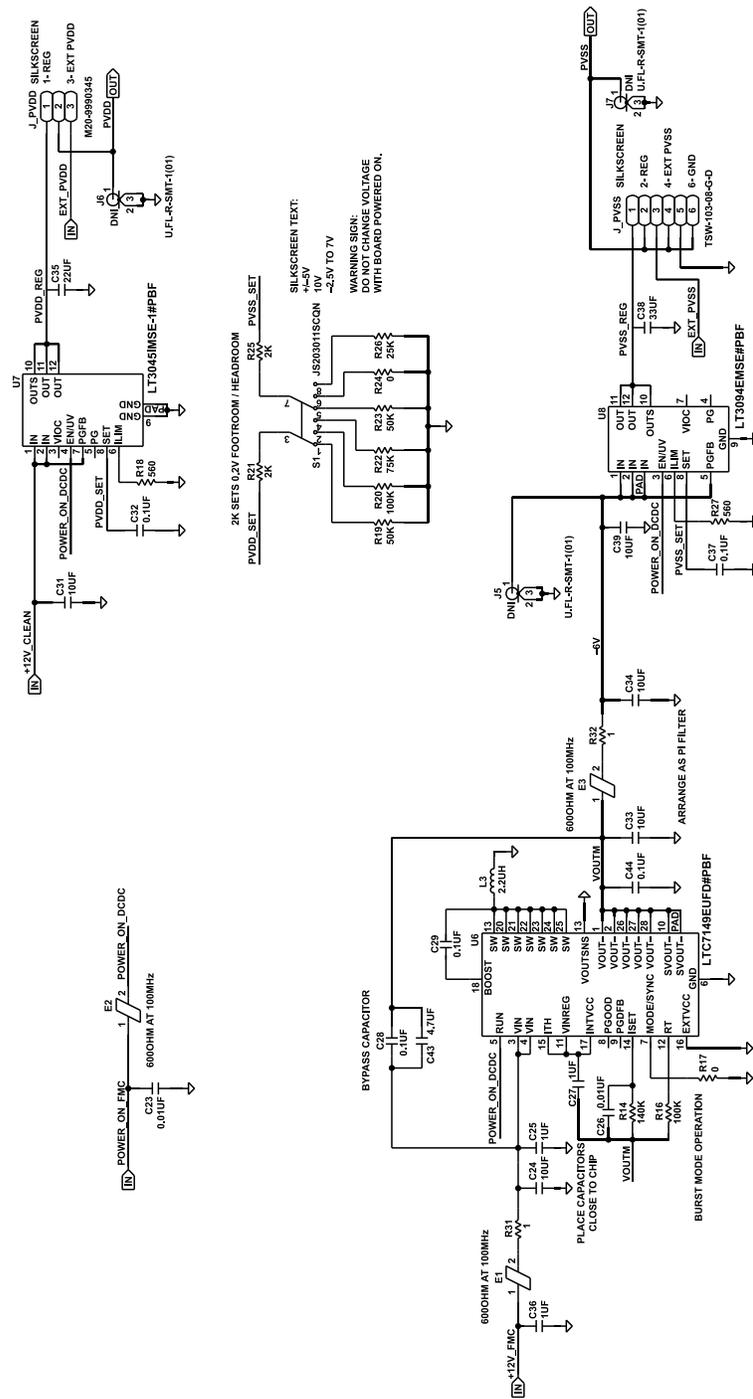


Figure 23. PVDD and PVSS LDOs and DC/DC Converter

EVALUATION BOARD SCHEMATICS

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

