DEMO MANUAL DC202

LOW INPUT VOLTAGE SWITCHER

LTC1649 Constant-Frequency Synchronous 15A DC/DC Converter

DESCRIPTION

Demonstration Circuit 202 is a constant-frequency, high efficiency regulator using the LTC®1649 switching regulator. This controller is optimized for use with very low supply voltages. Typical applications are power for DSPs, ASICs and low voltage logic termination (SSTL, GTL and the like). The input voltage can range from 2.7V to 5V. The output voltage is programmable from 1.5V to 2.5V by means of a jumper. The LTC1649 uses a 200kHz switching frequency and voltage mode control to switch a pair of N-channel power MOSFETs. Operating efficiencies exceeding 90% are obtained for load currents from 1A to 10A. Additionally, the supply current in shutdown is less than 10µA. **Gerber files for this circuit board are available. Call the LTC factory.**

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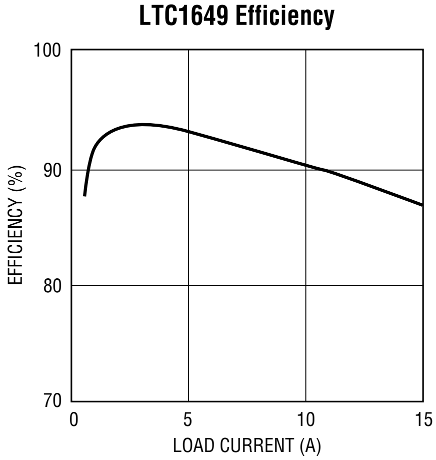
PERFORMANCE SUMMARY ($T_A = 25°C$)

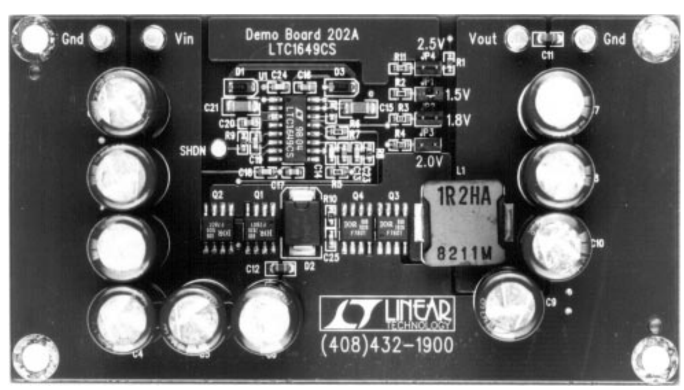
SYMBOL	CONDITION	VALUE
V_{IN}	Input Voltage Range	2.7V to 5V
V_{OUT}	Output Voltage (Jumper Selectable)	1.5V, 1.8V, 2V, 2.5V
I_{OUT}	Maximum Output Load Current	15A
	Typical Output Ripple (I_O = 15A)	$40mV_{P-P}$
	Nominal Operating Frequency	200kHz
I_Q	Supply Current in Shutdown	10µA

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

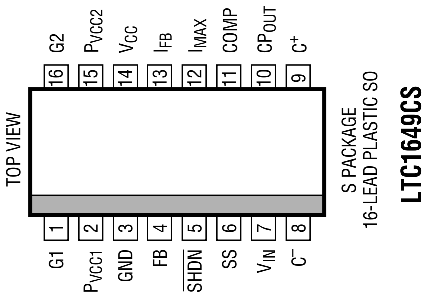
LTC1649 Efficiency



Demo Board



PACKAGE AND SCHEMATIC DIAGRAMS



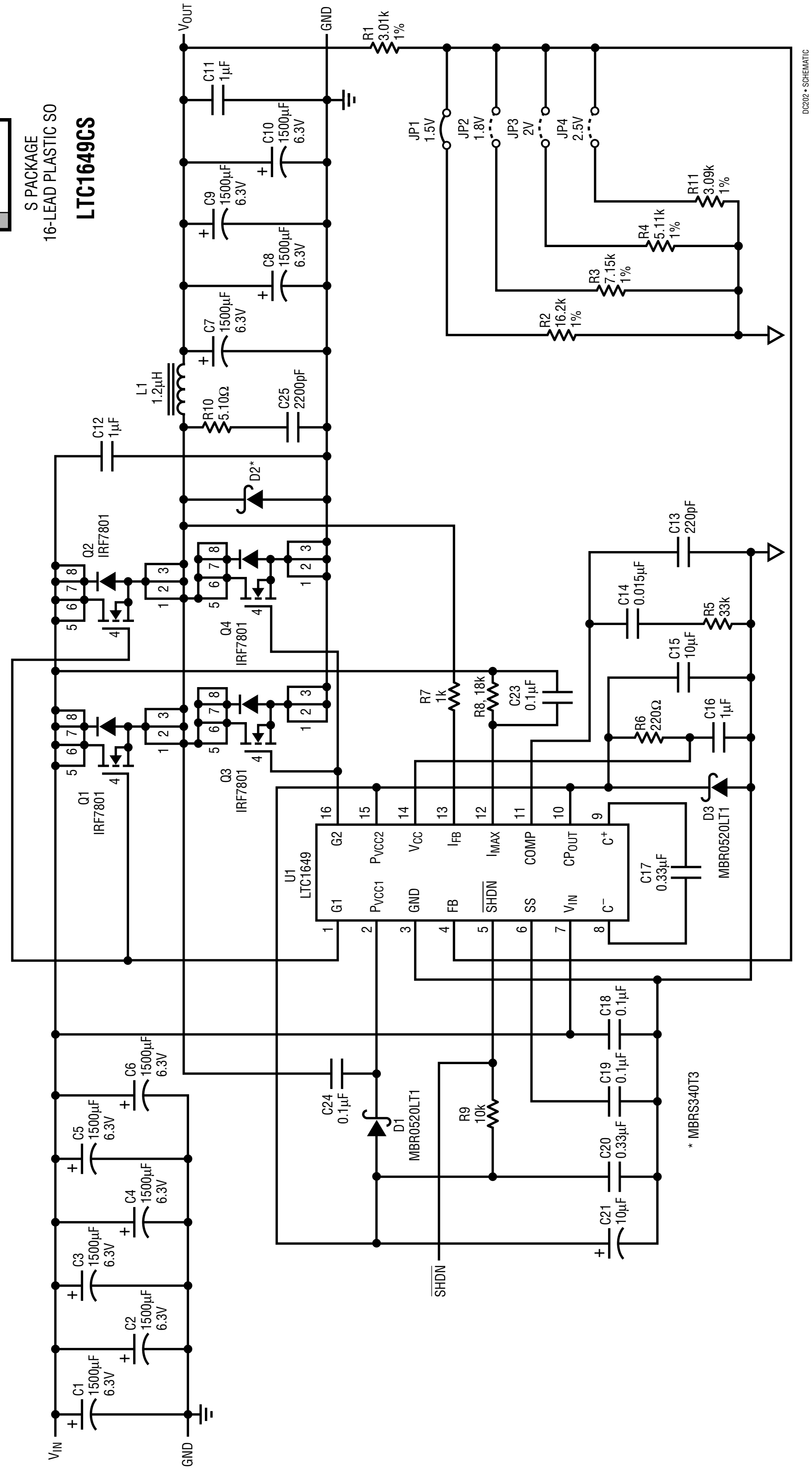


Figure 1. LTC1649 Constant-Frequency Synchronous DC/DC Converter Schematic

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1 to C10	10	6MV1500GX	1500µF 6.3V 20% Aluminum Capacitor	Sanyo	(619) 661-6835
C11, C12	2	0805YG105ZAT1A	1µF 16V 80% Y5V Capacitor	AVX	(803) 946-0362
C13	1	06035A221KAT1A	220pF 50V NPO Capacitor	AVX	(803) 946-0362
C14	1	06033C153KAT1A	0.015µF 25V X7R Capacitor	AVX	(803) 946-0362
C15, C21	2	1206ZG106ZAT2A	10µF 10V 80% Y5V Capacitor	AVX	(803) 946-0362
C16	1	0603ZG105KAT1A	1µF 10V 80% Y5V Capacitor	AVX	(803) 946-0362
C17, C20	2	0603YC334KAT1A	0.33µF 16V 10% X7R Capacitor	AVX	(803) 946-0362
C18, C19, C23, C24	4	0603YC104KAT1A	0.1µF 16V 10% X7R Capacitor	AVX	(803) 946-0362
C25	1	06035C222KAT1A	2200pF 50V X7R Capacitor	AVX	(803) 946-0362
D1, D3	2	MBR0520LT1	Diode	Motorola	(800) 441-2447
D2	1	MBRS340T3	Schottky Diode	Motorola	(800) 441-2447
JP1 to JP4	4	2802S-02G2	Jumper	COMM-CONN	(626) 301-4200
L1	1	ETQP6F1R2HFA	1.2µH Inductor	Panasonic	(201) 348-7522
Q1 to Q4	4	IRF7801	N-Channel MOSFET	Int'l Rectifier	(310) 322-3331
R1	1	WCR0603-3011-F-P-LT	3.01k 1/16W 1% CR Resistor	IRC	(512) 992-7900
R2	1	WRC0603-1622-F-P-LT	16.2k 1/16W 1% CR Resistor	IRC	(512) 992-7900
R3	1	CR16-7151FM	7.15k 1/16W 1% Chip Resistor	TAD	(800) 508-1521
R4	1	WCR0603-5111-F-P-LT	5.11k 1/16W 1% CR Resistor	IRC	(512) 992-7900
R5	1	CR16-333JM	33k 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R6	1	CR16-221JM	220Ω 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R7	1	CR16-102JM	1k 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R8	1	CR16-183JM	18k 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R9	1	CR16-103JM	10k 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R10	1	CR16-5R1JM	5.10Ω 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R11	1	CR16-3091FM	3.09k 1/16W 1% Chip Resistor	TAD	(800) 508-1521
TP1, TP2, TP4, TP5	4	2502-2	Turret Test Point	Mill-Max	(516) 922-6000
TP3	1	2308	Test Point	Mill-Max	(516) 922-6000
U1	1	LTC1649CS	I.C.	LTC	(408) 432-1900

QUICK START GUIDE

Refer to Figure 2 for proper measurement equipment set up and follow the procedure outlined below:

1. Connect the input power supply to the V_{IN} and GND terminals on the board using 16-gauge or heavier wire, soldered to the terminals. The input voltage is limited to between 2.7V and 5V.
2. Connect an ammeter in series with the input supply to measure input current.
3. Since this demo board operates with low input voltage and high output current, it is essential that the input voltage source be well regulated. If the input power supply is equipped with sense lines, connect $SENSE^+$ to V_{IN} and $SENSE^-$ to the GND terminal on the board.
4. Connect either power resistors or an electronic load to the V_{OUT} and GND terminals using 14-gauge or heavier wire, soldered to the terminals.
5. Connect an ammeter in series with output load to measure output current.
6. The $\overline{SHDN}$ pin should be left floating for normal operation and tied to GND for shutdown.
7. Set the desired output voltage with jumpers JP1 to JP4, as shown in Table 1.
8. Connect a voltmeter across the V_{IN} and GND terminals to measure input voltage.
9. Connect a voltmeter across the V_{OUT} and GND terminals to measure output voltage.
10. After all connections are made, turn on input power and verify that the output voltage is correct.

Table 1

POSITION	OUTPUT VOLTAGE
JP1	1.5V
JP2	1.8V
JP3	2.0V
JP4	2.5V

OPERATION

The circuit in Figure 1 highlights the capabilities of the LTC1649. The application circuit can provide a variety of output voltages (1.5V to 2.5V) by selecting the appropriate jumper JP1 to JP4. The LTC1649 is a voltage mode control, PWM, synchronous switching regulator, designed to drive external N-channel power MOSFETs using a fixed 200kHz switching frequency. The LTC1649 shares the bulk of its circuitry with the LTC1430. The significant difference is that the LTC1649 features an internal charge pump that provides a regulated 5V output at the CP_{OUT} pin with V_{IN} as low as 2.7V. This output is used to power the LTC1649's control circuitry and output drivers to provide 5V drive to the external MOSFETs.

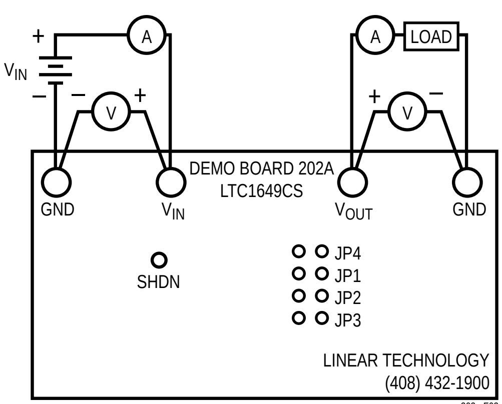


Figure 2. Proper Measurement Setup

Theory of Operation

The divided output is compared to the 1.265V reference. The difference voltage is multiplied by the error amplifier's (FB) gain. The resulting error signal is then compared to an internally generated, fixed frequency sawtooth waveform by the PWM comparator, which generates a pulse-width modulated signal. This PWM signal drives the external MOSFETs through G1 and G2. The output of this chopper circuit is then filtered by L1 and C7 to C11 to produce the desired DC output voltage. Loop compensation is achieved with external compensation at the COMP pin, the output node of the FB transconductance amplifier.

OPERATION

Soft Start Function

The LTC1649 includes a soft-start circuit to control the rate of rise of the output voltage at turn-on. An internal 12µA current source charges an external capacitor, C19 (see Figure 1), connected to the SS pin. When the voltage at the SS pin rises to 3V, the LTC1649 begins operating at a low duty cycle. As the voltage at the SS pin continues to rise, the duty cycle will increase until the error amplifier takes over and begins to regulate the output.

Current-Limit Loop

The I_{LIM} amplifier (see the LTC1649 or LTC1430 data sheet) monitors the voltage drop across the external high-side MOSFETs (Q1 and Q2) with the I_{FB} pin during the time when G1 is high. It compares this voltage to the voltage at the I_{MAX} pin. As the peak current increases, the drop across Q1 and Q2 increases. When the voltage at I_{FB} drops below the voltage at I_{MAX}, indicating that the MOSFET's drain current has exceeded the maximum level, the I_{LIM} amplifier starts to pull current out of the external soft-start capacitor, cutting the duty cycle and controlling the output current level.

Charge Pump

The LTC1649's internal charge pump generates a regulated 5V at the CP_{OUT} pin with an input voltage of 2.7V to 5V. The charge pump achieves regulation by sensing the output voltage at the CP_{OUT} pin through an internal resistor divider and enabling the charge pump when the divided output drops below the comparator's lower trip point. When the charge pump is enabled, a 2-phase nonoverlapping clock (typical operating frequency = 800kHz) controls the internal charge pump switches. On phase one of the clock, flying capacitor C1 is charged to V_{IN}. On phase two of the clock, C1 is stacked in series with V_{IN} and connected to CP_{OUT} through an internal switch. This charging and discharging of the flying capacitor continues until the divided output reaches the trip point of the comparator and the charge pump is disabled. At this point, the voltage on the CP_{OUT} pin is 5V.

COMPONENT SELECTION

Capacitor Considerations

Input and output capacitors are Sanyo 6.3MV1500GX. The input capacitors must be rated for the RMS input ripple. A good rule of thumb is that the input ripple current will be 50% of the output current. It isn't necessary to design for the worst-case peak output current. The capacitors can easily handle short excursions to higher loads. Only the sustained average load current need be considered. For a continuous output current of 15A, the ripple current rating of the input capacitors should be 7.5A. The capacitors chosen are rated at 1.25A each, so six capacitors are adequate.

Output capacitors need to have a ripple current rating greater than the RMS value of the inductor ripple current. This is a function of the operating frequency and inductor value, as well as input and output voltages. Because the ripple current is relatively small, the controlling parameter is generally the capacitor's ESR (equivalent series resistance). The maximum allowable ESR is equal to the maximum allowable peak-to-peak output ripple voltage divided by the peak-to-peak inductor ripple. In general, if the ESR is low enough for the ripple voltage and transient requirements, the capacitors will have more than adequate ripple-current capability.

Inductor Selection

Inductor selection is not extremely critical. The inductor used here was chosen for fairly low cost and ready availability. The main concerns in choosing an appropriate inductor are the inductance value required, the saturation current rating and the temperature rise. Most manufacturers specify a DC current rating that produces a temperature rise of 40°C. If a design will not see high ambient temperatures, a larger temperature rise can usually be tolerated. Another maximum current specification is related to core saturation. A manufacturer may specify that maximum rated current is the point at which inductance is down by 10% (some specify 25%). Since most core materials and structures will result in a gentle, controlled roll off of inductance with DC bias, there is no magical point where the inductor is no longer useful. Look

OPERATION

at what the inductance will be at the maximum load current expected and determine if the output ripple will remain within specified limits. If it will, the inductor will most likely work correctly. Ripple current is generally designed for between 10% and 40% of output current.

MOSFET Selection

The main concern with FET selection in very low voltage applications is thermal management. At high current levels, power devices will get hot. The trick is to keep the temperature rise within acceptable limits. Most of the FET's power dissipation will be due to conduction losses. Therefore, by choosing a FET with a sufficiently low $R_{DS(ON)}$, the power dissipation, and therefore the temperature rise, can be made arbitrarily low. The price paid for very low temperature rise is more expensive FETs. Switching losses are a concern only for the high-side FET. The low-side FET turns on and off into a forward-biased diode, so its transition losses are very small. The high-side FET, in contrast, must provide all of the reverse recovery charge that the low-side FET's body diode will demand. This can result in a significant amount of switching loss in this device.

Although it may seem that a lower on-resistance FET is always desirable from an efficiency perspective, this is not necessarily true. A smaller device will have a lower gate-charge power requirement and will also exhibit faster switching transition times. The resulting reduction in AC losses may more than offset the increase in conduction losses. A smaller, higher on-resistance FET may prove the more efficient, as well as the lower cost solution. As the load current increases, gate drive losses become less of a concern. At output currents on the order of 15A, lower resistance FETs will probably be better in terms of overall efficiency, but not necessarily the most cost-effective choice. Each application will place a different value on a few points of efficiency.

How to Measure Voltage Regulation and Efficiency

When trying to measure load regulation or efficiency, voltage measurements should be made directly across the V_{OUT} and GND terminal and should not be taken at the end of test leads at the load. Similarly, input voltage should be measured directly on the V_{IN} and GND terminals of the LTC1649 demo board. Input and output current should be measured by placing an ammeter in series with the input supply and load. Refer to Figure 2 for the proper test equipment setup. Refer to page one for a typical efficiency curve for V_{IN} = 3.3V, V_{OUT} = 2.5V and I_{LOAD} = 0.5A to 15A.

How to Measure Output Voltage Ripple

In order to measure output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Therefore, a sturdy wire should be soldered on the output side of the GND terminal. The other end of the wire is looped around the ground side of the probe and should be kept as short as possible. The tip of the probe is touched directly to V_{OUT} (see Figure 3). Bandwidth is generally limited to 20MHz for ripple measurements. Also, if multiple pieces of line-powered test equipment are used, be sure to use isolation transformers on their power lines to prevent ground loops, which can cause erroneous results. Figure 4 shows the output voltage ripple with a steady-state load of 15A.

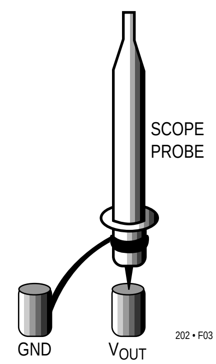


Figure 3. Measuring Output Voltage Ripple

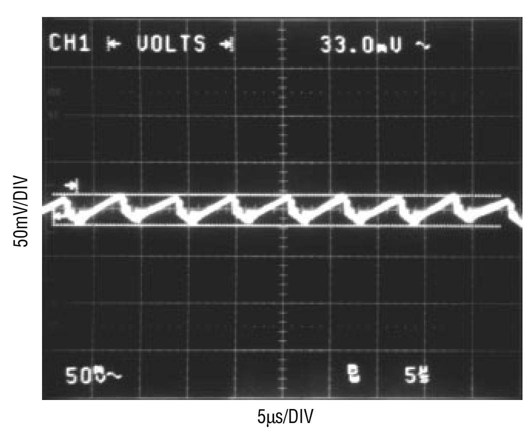


Figure 4. Output Voltage Ripple at I_0 = 15A, V_{IN} = 3.3V and V_{OUT} = 2.5V

OPERATION

Heat Dissipation Issues

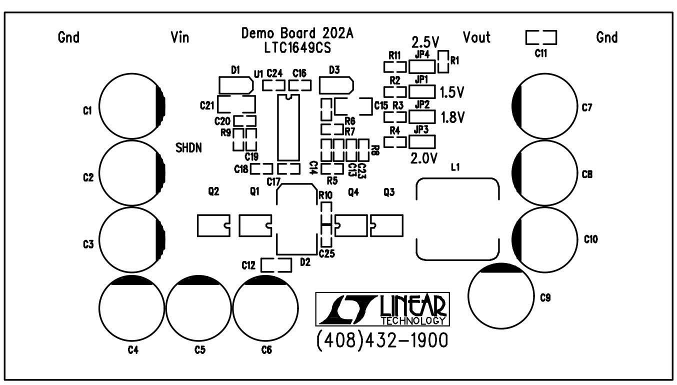
Since the LTC1649 demo board can supply up to 15A of continuous load current, care must be taken so as not to exceed the maximum junction temperature for the power MOSFETs. A few possibilities for dissipating the power are to use heat sinks and/or have airflow. Another possibility is to use the PC board as a heat sink. On the LTC1649 demo board, power MOSFETs Q1 to Q4 are surrounded by ground and power planes on both sides of the PC board, which are connected through vias to handle the power dissipation. If the LTC1649 is laid out on a multilayer motherboard, it is recommended to have metal on the inner layers directly underneath the power MOSFETs. This helps in spreading the heat and improves the power dissipation capability of the PCB.

Layout Guidelines

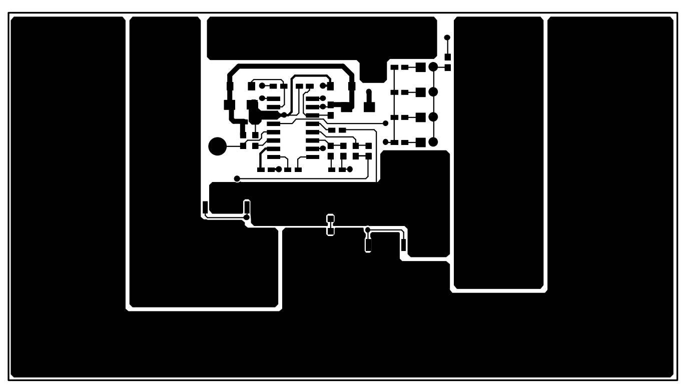
Be sure to follow the layout guidelines below:

1. The inductor, L1, MOSFETs Q1 to Q4 and the Schottky diode (D2) should be placed as close as possible to each other.
2. The I_{FB} pin should be connected directly to the sources of the MOSFETs Q1 and Q2 through R7.
3. The I_{MAX} pin should be connected directly to the drains of the MOSFETs Q1 and Q2 through R8 in parallel with C23.
4. Keep the trace from the FB pin to the junction of R1 and R2 short and use a long trace from the top of resistor R1 to the output terminal, rather than vice versa.
5. The source of the bottom MOSFETs Q3 and Q4 should be tied back to the ground of input capacitors C1 to C6 by means of a wide trace, not by the ground plane.
6. The ground of output capacitors C7 to C10 should be tied directly to the input capacitors' ground by means of a wide trace or by the ground plane.
7. The ground of the feedback resistors, COMP, SS and CP_{OUT} should be referenced to the chip ground pin, which is directly tied to the input bulk capacitors' ground.

PCB LAYOUT AND FILM



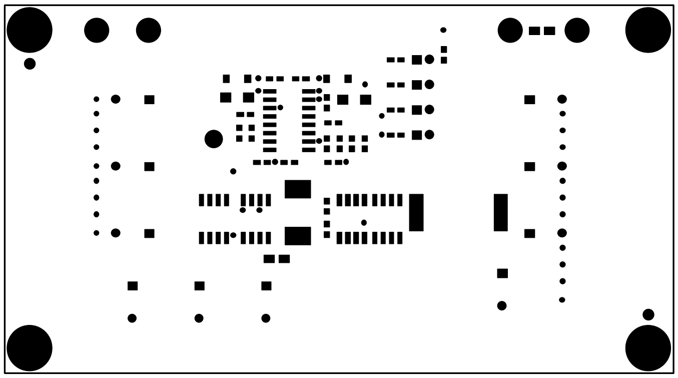
Component Side Silkscreen



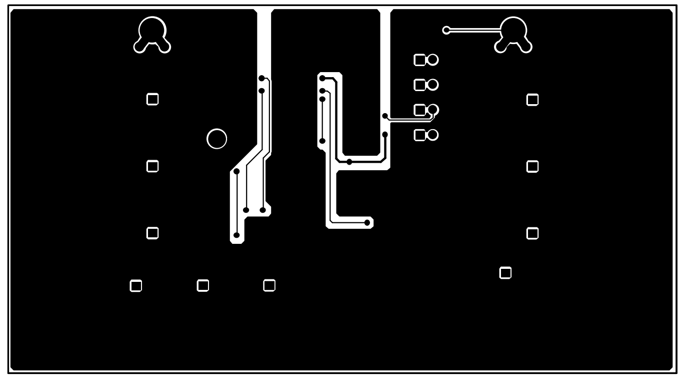
Component Side

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

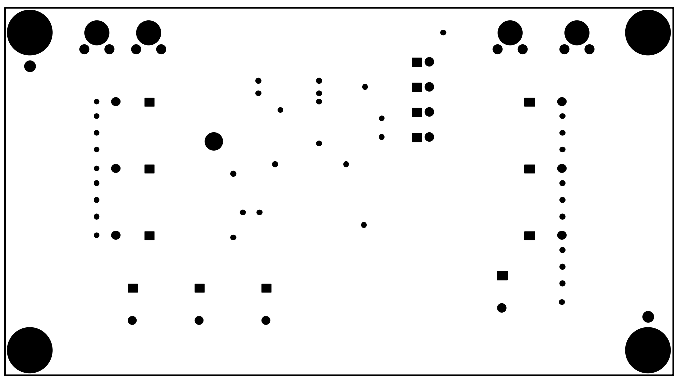
PCB LAYOUT AND FILM



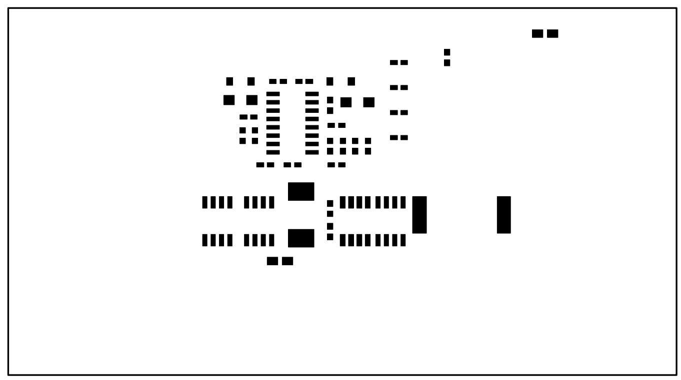
Component Side Solder Mask



Solder Side

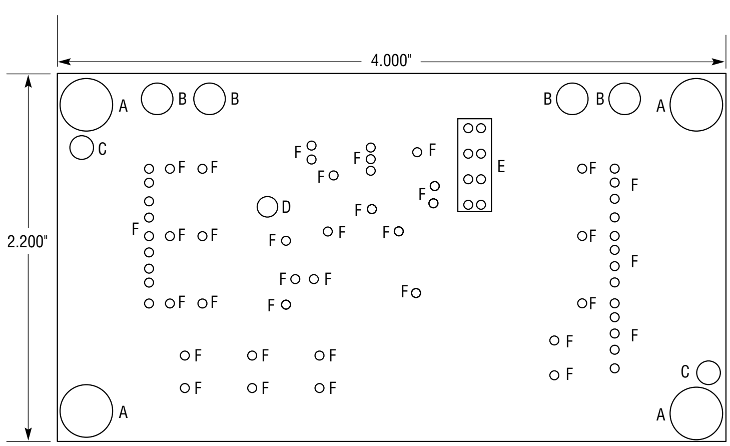


Solder Side Solder Mask



Component Side Pastemask

PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED
1. MATERIALS: 2 LAYERS, 0.062" THICK,
   FR-4 GLASS EPOXY 2 OZ COPPER CLAD
2. ALL HOLES SHALL BE PLATED THRU
3. PLATE THRU HOLES WITH COPPER 0.014 MIN
   THICKNESS (ALL VIAS SHOULD BE FILLED)
   ALL HOLE SIZES IN HOLE TABLE ARE AFTER PLATING
4. SILKSCREEN: USING WHITE NONCONDUCTIVE EPOXY INK
5. PROCESS: SOLDER MASK OVER BARE COPPER (SMOBC)
6. SOLDER MASK : LPI GREEN

SYMBOL	DIAMETER	NUMBER OF HOLES
A	0.156	4
B	0.094	4
C	0.070	2
D	0.061	1
E	0.026	8
F	0.025	20
UNMARKED	0.015	37
	TOTAL HOLES	76

DC202 • FAB DWG

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