ADV212 Release Notes

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ADV212 Release Notes

This document presents the release notes for the ADV212. The ADV212 has the same footprint and pin-configuration as the ADV202 and is also software compatible with the ADV202.
This document applies to parts that are branded as follows :

ADV212XBCZ Surf®
-115 or -150
xxxxxx.x [Revision Code]

1) Revision register and Chip ID

   The bit allocation for the Hardware Revision Register at 0x FFFF14F4h is defined as :

   0xFFFF14F4h [15:8] = Hardware Revision
   0xFFFF14F4h [7:1] = Software Revision
   0xFFFF14F4h [0] = Marker [always 0x1]

   The Chip ID is a 32-bit value where bits [31:16] contain the part number and bits [15:0] the value from the Hardware Revision Register:

   Chip ID [31:16] = part number = 0x27DB
   Chip ID [15:0] = revision register

   Chip ID bits [15:0] can be accessed at address 0xFFFF14F4 or 0xFFFF0250.
   Chip ID bits [31:16] can be accessed at address 0xFFFF0254 or otherwise the Chip ID can be read by accessing the JTAG scan chain #5. It is a 32-bit, LSB first scan chain.

2) ARM JTAG IDCODE

   For ADV212 parts the ARM JTAG IDCODE is 0x307000CB.

3) Normal Host Mode operation

   Issue: Normal Host Mode reads require: ADDR, CS/, WE/, ACK/ HDATA,
   Normal Host Mode writes require: ADDR, CS/, RD/ ACK/, HDATA.
   Timing specifications for Normal Host Mode reads and writes remain the same for the ADV202 and the ADV212.

   On the ADV202 and ADV212, the address set-up time [tSA] is 2ns for Normal Host Mode Read/Write accesses.

However, on the ADV202, ADDR [3:0] could change after the falling edge of WE/ or RD/ and still be recognized as a valid address. On the ADV212, ADDR[3:0] must be set up as specified for correct operation.

4) Raw Video Mode and JDATA mode

Issues: On the ADV202, is was not possible to use JDATA mode and Raw Video Mode simultaneously. This capability has been added in the ADV212.

In order to use Raw Video mode/JDATA mode on the ADV212 the following must be observed:

- Uncompressed video data is interfaced over VDATA[15:0] with VDATA[15] being MSB.
- Compressed video data is interfaced over HDATA[31:24] with HDATA[31] being MSB.
- BUSMODE [6:4] must be set to 0x0003h for Raw Video Mode/JDATA mode.
- EDMOD0 [5:3] must be set to 0x0003h.

5) PLL Control Register

Issues: PLL_HI [7] at address 0xE is reserved. Writes to this bit have no effect. Default value of this bit is undefined.

6) Raw Video mode

Issues: The ADV212 can recover from an empty FIFO condition without causing the part to stall or flushing data present in the CODE FIFO.
Dimension register settings recommended for Video Raw mode:

PIXEL_START = 1
PIXEL_END = XTOT
V0_START = 1
V0_END = YTOT
V1_START = not used
V1_END = not used

7) HSYNC to VDATA delay

Issues: The decode slave ‘ HSYNC input to VDATA output delay ‘ specification has changed from the ADV202 specifications.
Refer to the datasheet: VDATA Mode timing - Sync Delay for Decode Slave for ADV212 specifications.

8) EAV/SAV Field bit in Decode Slave mode

Issues: This work around is only required when replacing the ADV202 with ADV212 in Decode Slave mode for interlaced modes [NTSC, PAL, 1080i] when EAV/SAV mode is used.

On the ADV212 the Field bit in the timing codes is updated differently than on the ADV202:
The ADV212 updates on the EAV first, then the SAV for a particular line, whereas the ADV202 only updates the SAV for that particular line.

The data sequence for EAV/SAV video data is :

1. FF 00 00 EAV
2. Digital Line Blanking
3. FF 00 00 SAV
4. Digital Active Line data

When using the ADV212 it requires a change to the F0_START and F1_START register settings as follows:

Subtract 1 from the value of the previous [ADV202] register settings for F0_START and F1_START.

Example:

For NTSC:

ADV202 F0_START = 4
ADV202 F1_START = 266

change to :

ADV212 F0_START = 3
ADV212 F1_START = 265

For PAL:

ADV202 F0_START = 4
ADV202 F1_START = 266

change to :

ADV212 F0_START = 3

ADV212 F1_START = 265

For 1080i :

ADV202 F0_START = 4
ADV202 F1_START = 266

change to :

ADV212 F0_START = 3
ADV212 F1_START = 265

9) Decode Slave frame drop

Issues: Video data input with external sync signals. On previous releases, vertical synchronization was obtained only once - on the first inactive edge of VSYNC. Subsequent Vsyncs were ignored.

The ADV212 is now sensitive to every end of frame VSYNC transition. Therefore, to avoid any frame drops, the VSYNC inactive edge should not be asserted during the active portion of a line. Rather, it should be asserted during the horizontal blanking of the last active line in a field.

Example:
HSYNC polarity = 0 = negative edge.
VSYNC polarity = 0 = negative edge.

The polarity is set with the PICFG decode parameter for non-custom specific modes or in the PMODE2 register for Custom Specific mode.

For these polarity settings, VSYNC rising edge should be applied when HSYNC = 1 during horizontal blanking.

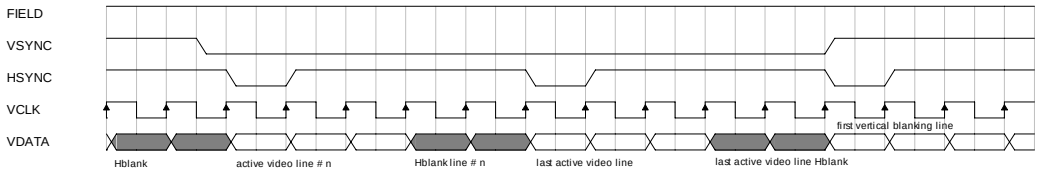

Figure 1. ADV212 incorrect H, V, F sync input in decode slave mode

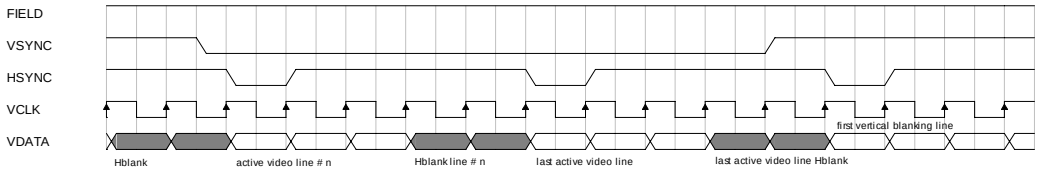

Figure 2. ADV212 correct H,V, F sync input in decode slave mode