Evaluation Board User Guide

ADPL42092 Evaluation Boards

Evaluating the ADPL42092: -20V, -200mA, Low-Noise Linear Regulator

General Description

The ADPL42092 evaluation boards evaluate the ADPL42092, a -20V, -200mA, low-noise, low-dropout linear regulator, in two packages: 6-Lead Lead Frame Chip Scale Package (LFCSP) and 5-Lead Thin Small Outline Transistor (TSOT). The circuits designed with the ADPL42092 are used primarily in noise-sensitive applications, communications and infrastructure, medical and healthcare, and industrial and instrumentation.

Features and Benefits

- Input Voltage Range: -2.7V to -20V
- Resistor Programmed -15V Output Voltage
- Maximum Output Current: -200mA
- The configuration jumper selects between connecting the EN pin to the V_{IN} pin to turn the regulator ON, or using an external EN signal to turn the regulator ON
- Jumper connects the SENSE/ADJ Pin to the Output through a resistor divider or directly
- VIN, VOUT, and GND test points for Regulation and Dropout Voltage Monitoring
- 6-Lead (2mm x 2mm) LFCSP Package or 5-Lead TSOT Package

Ordering Information ***appears at end of data sheet.***

Quick Start

Required Equipment

- DC power supply
- Multimeters for voltage and current measurements
- Electronic or resistive loads

Procedure

The ADPL42092 evaluation boards are easy to set up for evaluating the ADPL42092's performance. See *Figure 1* and *Figure 2* for the evaluation board connections, and use the following steps:

1. Connect the load between the VOUT and GND terminals.
2. With the input power supply off and turned down, connect the input supply to the VIN and GND terminals. Remember that this is a negative LDO, so ensure that V_{IN} is correct. Ensure that the JP1 shunt connects EN to V_{IN}, as specified in the jumper connection guide. Ensure that the JP2 shunt allows the resistor divider to set the output to -15V, as shown in the jumper connection guide (see *Table 1*).
3. With the load turned down, turn the input power supply on and adjust the voltage to -15.5V or higher.
4. Vary V_{IN} from -15.5V to -20V and the load current from 0A to -200mA. Observe conservative power dissipation limits and note the following when setting V_{IN} and the load current.
   - An input voltage too close to the programmed output voltage that is too low can cause dropout operation and a loss of output-voltage regulation.
   - The amount of output current combined with an input voltage that is too high above the output can increase power dissipation to an unacceptable level.
5. Monitor regulation and dropout voltage at the VIN, VOUT, and GND test points.
6. To apply an EN signal externally, reposition jumper JP1 and apply the EN signal to the EN connector.
7. If an output voltage other than -15V is desired, change resistors R1 and R2.
8. A resistor-capacitor (RC) network can be installed in the component placeholder locations in parallel with the top feedback divider resistor R1 to improve noise performance. Refer to the *ADPL42092* data sheet for details.

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ADPL42092 Evaluation Board Photos

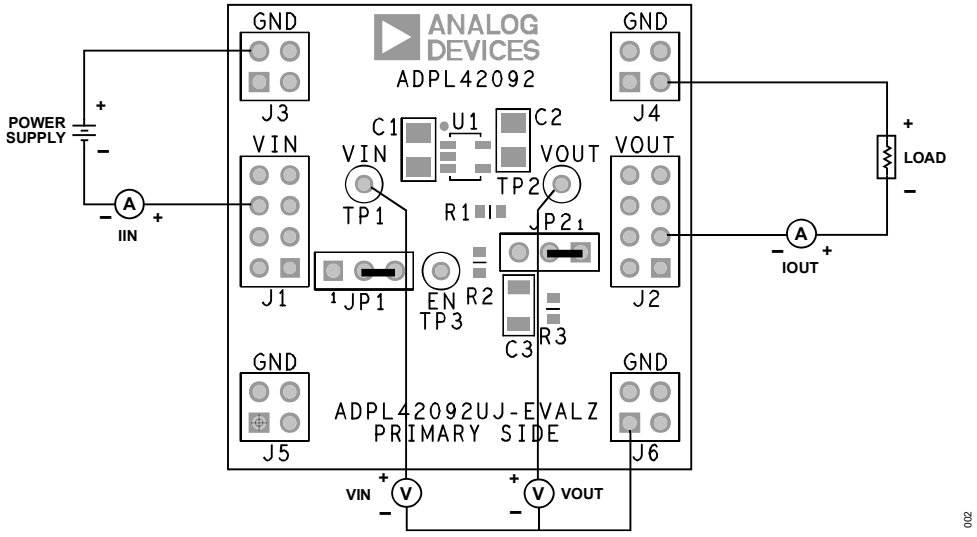

Figure 1. ADPL42092 TSOT Evaluation Board

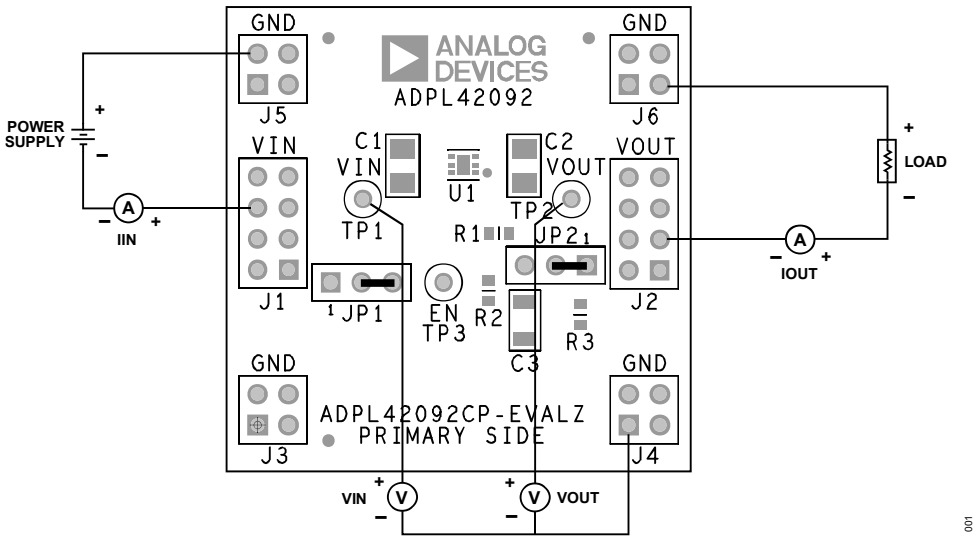

Figure 2. ADPL42092 LFCSP Evaluation Board

Table 1. Jumper Connection Guide

JUMPER	DEFAULT CONNECTION	FEATURE
JP1	Pin 2 to Pin 3	Turns the regulator on.
JP2	Pin 1 to Pin 2	Connects the ADJ pin to the output through a resistor divider.

Detailed Description of Hardware

Full specifications for the ADPL42092 are provided in the *ADPL42092* data sheet from Analog Devices, Inc. This user guide is intended to be used in conjunction with the ADPL42092 data sheet when operating the ADPL42092 evaluation boards. See the Ordering Information section for more details on the two available evaluation boards: one configured for the 6-lead, 2mm × 2mm LFCSP package, and the other for the 5-lead TSOT package.

The evaluation boards have a default output voltage of -15V. The maximum output current is -200mA, but the output current is also limited by the thermal dissipation of the ADPL42092. The evaluation boards use the adjustable version of the ADPL42092. A resistor divider programs the output of the adjustable ADPL42092 to -15V. Noise performance of the adjustable ADPL42092 can be made comparable to that of a fixed output ADPL42092 by installing optional RC network components in the placeholders provided by the evaluation board's printed circuit board (PCB) designs. The evaluation boards can easily be configured with a jumper for fixed output voltage operation to achieve -1.22V, using the adjustable output version of the ADPL42092, which connects the ADJ pin directly to the device's output.

In addition to connectors for the input voltage, output voltage, EN control signal, and GND, the evaluation boards provide test points for the input and output pin voltages. A jumper normally connects the EN pin to the V_{IN} input, but it can be repositioned to drive EN externally at its connector instead.

Table 2. Performance Summary of the Evaluation Boards

Specifications are at T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	I_{OUT} = -10mA, V_{OUT} = -15V	-15.5		-20	V
Input Voltage Range (LFCSP Package Evaluation Board)	V_{IN}	I_{OUT} = -200mA, V_{OUT} = -15V	-15.5		-20*	V
Input Voltage Range (TSOT Package Evaluation Board)	V_{IN}	I_{OUT} = -200mA, V_{OUT} = -15V	-15.5		-18.5*	V
Output Voltage	V_{OUT}	V_{IN} = -15.5V, I_{OUT} = -200mA, R1 = 137kΩ, R2 = 12.1kΩ	-14.57	-15	-15.33	V
Shutdown Input Current	I_{GND_SD}	JP1 = Pin 1 to Pin 2, V_{IN} = -15.5V, EN = GND			-8	µA

**The maximum power dissipation and, consequently, the maximum input voltage for an output that is programmed to -15V with a -200mA load is determined by the 60°C temperature rise of the ADPL42092 on the evaluation board. In addition, ensure that both the ambient temperature and the maximum device junction temperature are considered. Refer to the ADPL42092 data sheet for more information.*

Printed Circuit Board (PCB) Layout

The printed circuit boards (PCBs) for these evaluation boards are 0.062” thick and 1.5” square. There are four copper layers, and the finished copper thickness of the top and bottom layers is 1 ounce. The input and output capacitors are placed near the ADPL42092 with their ground terminals connected to the lower half of the board. The bottom side of the ADPL42092 TSOT package PCB connects to the ground on the top PCB layer by thermal vias under or near the ADPL42092 and at other points, while the ADPL42092 LFCSP PCB bottom side does the same, but this board has the input shape aside from just the bottom layer being a whole ground plane. The layout significantly affects the circuit's electrical performance and reliability.

Ordering Information

MODEL[1,2]	PACKAGE DESCRIPTION
ADPL42092CP-EVALZ	6-Lead LFCSP Package Evaluation Board
ADPL42092UJ-EVALZ	5-Lead TSOT Package Evaluation Board

[1]*Z = RoHS Compliant Part.*

[2]*The evaluation boards are preconfigured with an adjustable ADPL42092.*

ADPL42092 LFCSP Package Evaluation Board Bill of Materials

ITEM	QTY	REF_DES	DESCRIPTION	MANUFACTURER, PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	2	C1, C2	Capacitor, 2.2µF, 50V, 10%, X7R, 1206	Kyocera AVX, 12065C225KAT2A
2	1	R1	Resistor, 137kΩ, 1%, 1/10W, 0603	Panasonic, ERJ-3EKF1373V
3	1	R2	Resistor, 12.1kΩ, 1%, 1/8W, 0603, AEC-Q200	Vishay, CRCW060312K1FKEA
4	1	U1	-20V, -200mA, low-noise, low-dropout (LDO) regulator, LFCSP package	Analog Devices Inc., ADPL42092ACPZN-R7
OPTIONAL EVALUATION BOARD COMPONENTS				
1	1	R3	Resistor, 0603, optional	
2	1	C3	Capacitor, 1206, optional	
HARDWARE				
1	2	J1, J2	Connector, header, male, through hole, 8 position, 2.54mm	Sullins, PEC04DAAN
2	4	J3, J4, J5, J6	Connector, header, male, through hole, 4 position, 2.45mm	Sullins, PEC02DAAN
3	2	JP1, JP2	Connector, header, male, through hole, 3 position, 2.54mm	Sullins, PEC03SAAN
4	3	TP1, TP2, TP3	Test Point, White	Components Corporation, TP-105-01-09
5	2	XJP1, XJP2	Shunt connector, 2 (1 x 2) position, closed top, 2.54mm	Sullins, STC02SYAN

ADPL42092 TSOT Package Evaluation Board Bill of Materials

ITEM	QTY	REF_DES	DESCRIPTION	MANUFACTURER, PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	2	C1, C2	Capacitor, 2.2µF, 50V, 10%, X7R, 1206	Kyocera AVX, 12065C225KAT2A
2	1	R1	Resistor, 137kΩ, 1%, 1/10W, 0603	Panasonic, ERJ-3EKF1373V
3	1	R2	Resistor, 12.1kΩ, 1%, 1/8W, 0603, AEC-Q200	Vishay, CRCW060312K1FKEA
4	1	U1	-20V, -200mA, Low Noise, LDO regulator, TSOT package	Analog Devices, Inc., ADPL42092AUJZ-R7
OPTIONAL EVALUATION BOARD COMPONENTS				
1	1	R3	Resistor, 0603, optional	
2	1	C3	Capacitor, 1206, optional	
HARDWARE				
1	2	J1, J2	Connector, header, male, through hole, 8 position, 2.54mm	Sullins, PEC04DAAN
2	4	J3, J4, J5, J6	Connector, header, male, through hole, 4 position, 2.54mm	Sullins, PEC02DAAN
3	2	JP1, JP2	Connector, header, male, through hole, 3 position, 2.54mm	Sullins, PEC03SAAN
4	3	TP1, TP2, TP3	Test Point, White	Components Corporation, TP-105-01-09
5	2	XJP1, XJP2	Shunt connector, 2 (1 x 2) position, closed top, 2.54mm	Sullins, STC02SYAN

ADPL42092 LFCSP Package Evaluation Board Schematic Diagram

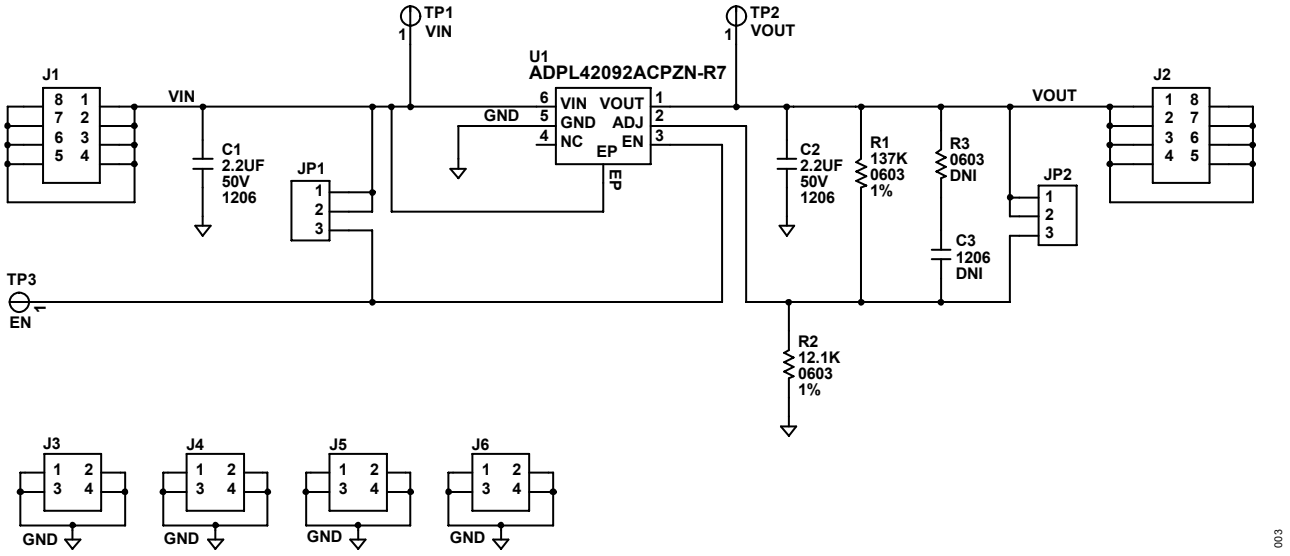

Figure 3. ADPL42092 LFCSP Package Evaluation Board Schematic Diagram

ADPL42092 TSOT Package Evaluation Board Schematic

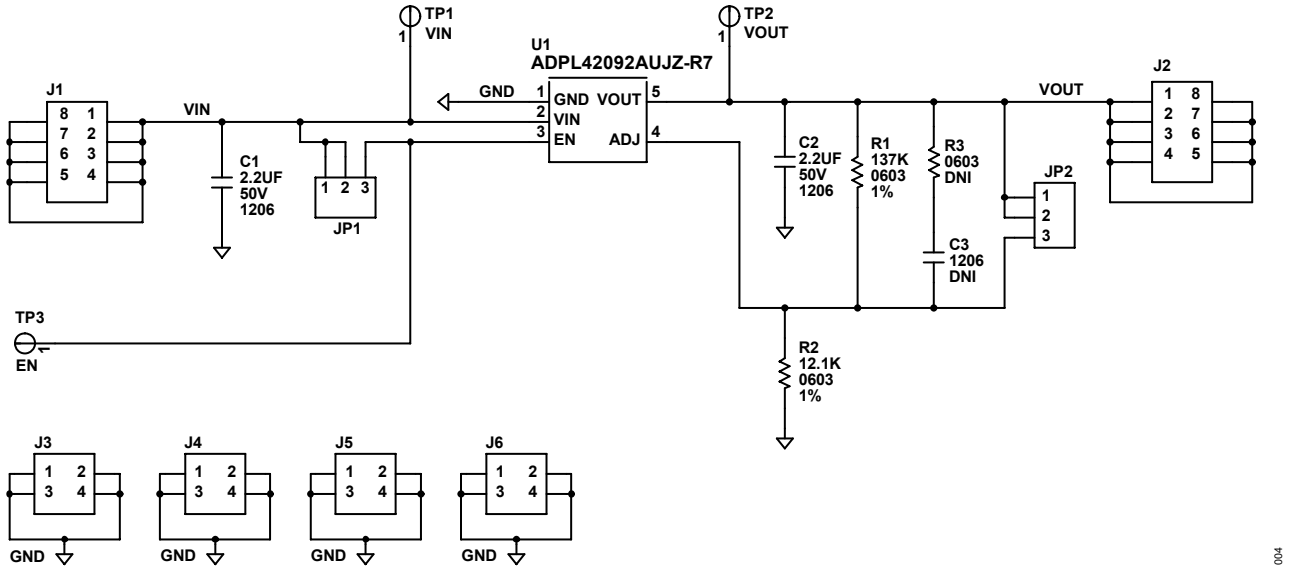

Figure 4. ADPL42092 TSOT Package Evaluation Board Schematic Diagram

ADPL420292 LFCSP Package Evaluation Board PCB Layout

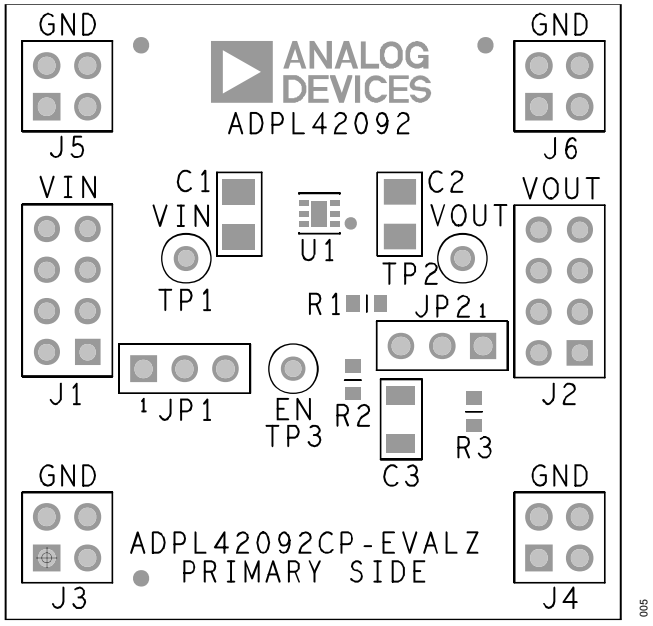

Figure 5. ADPL42092CP-EVALZ Component Placement Guide—Top Silkscreen

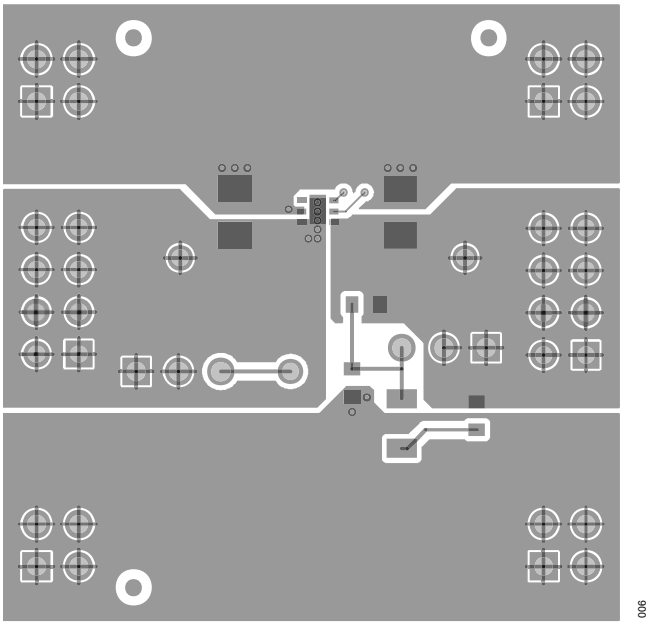

Figure 6. ADPL42092CP-EVALZ PCB Layout—Top View

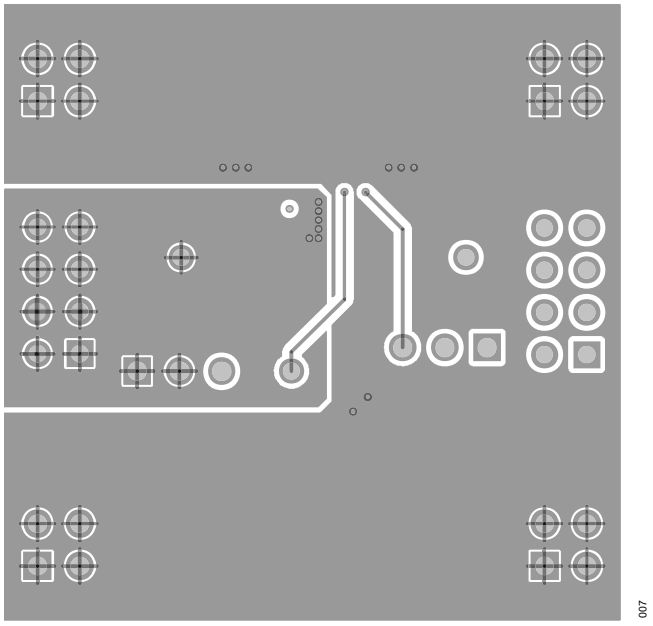

Figure 7. ADPL42092CP-EVALZ PCB Layout—Bottom View

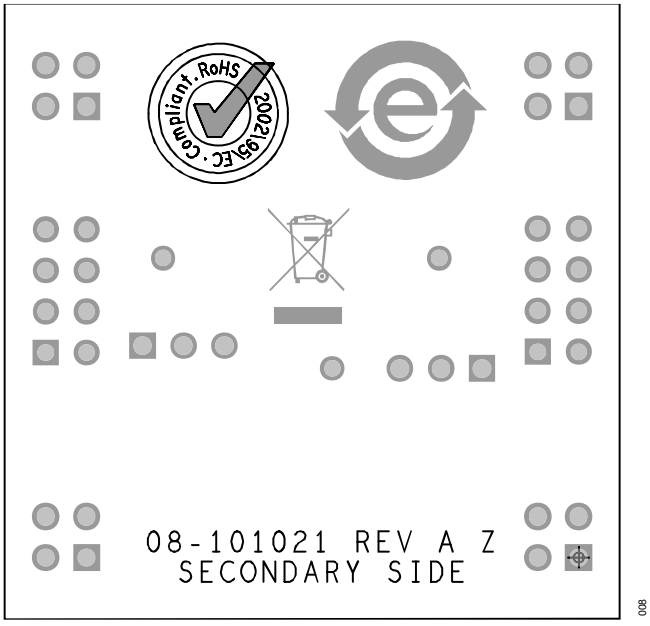

Figure 8. ADPL42092CP-EVALZ PCB Layout—Bottom Silkscreen

ADPL42092 TSOT Package Evaluation Board PCB Layout

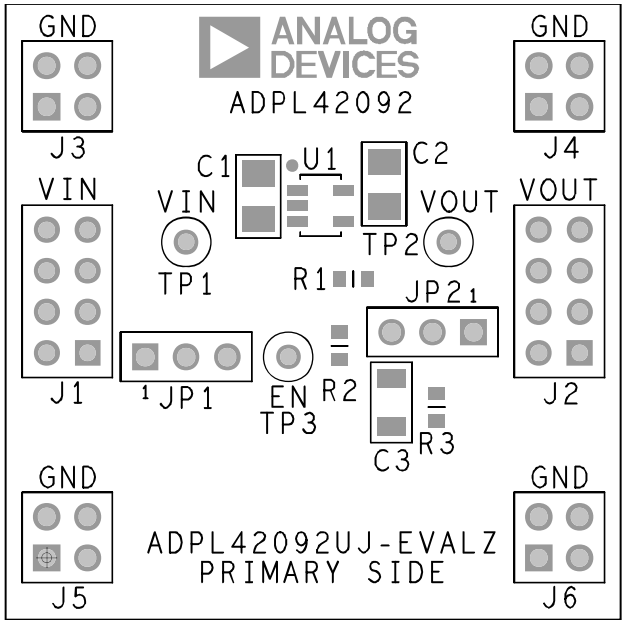

Figure 9. ADPL42092UJ-EVALZ Component Placement Guide—Top Silkscreen

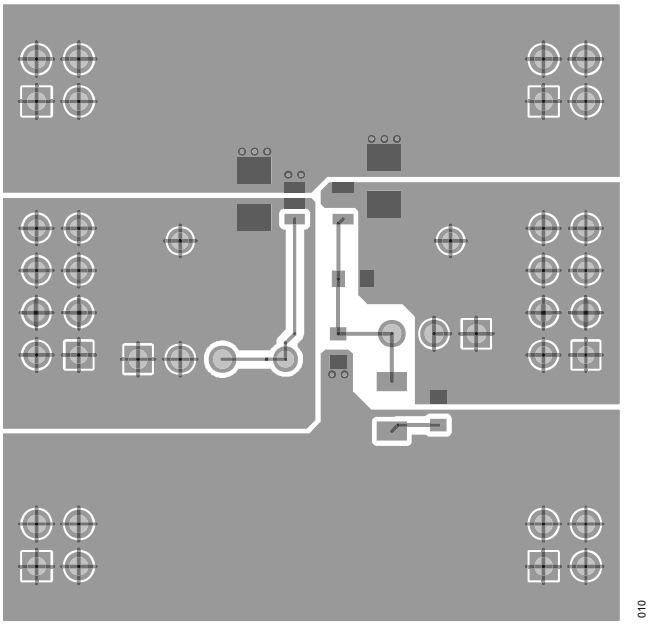

Figure 10. ADPL42092UJ-EVALZ PCB Layout—Top Layer

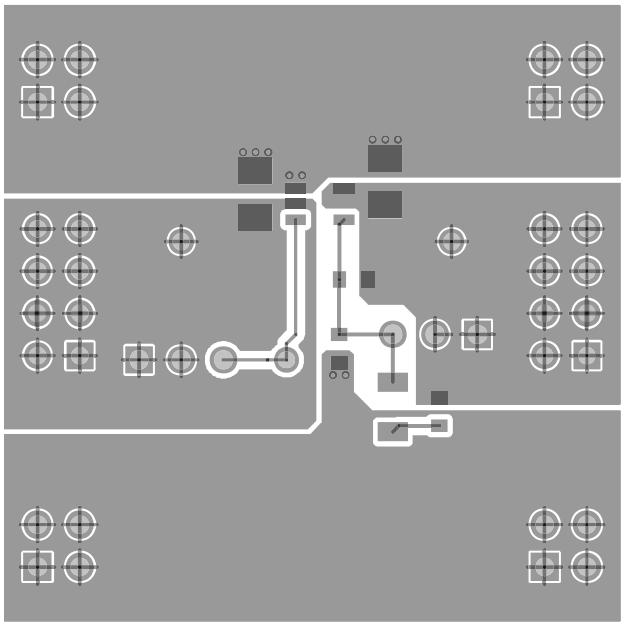

Figure 11. ADPL42092UJ-EVALZ PCB Layout—Bottom Layer

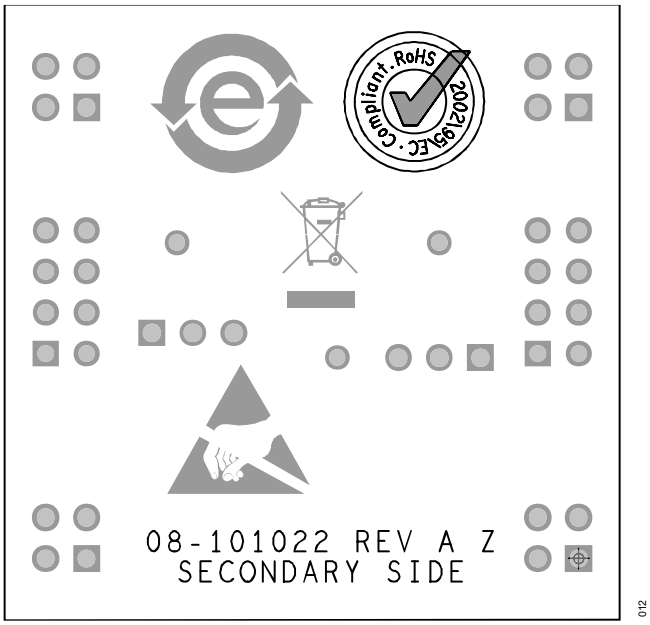

Figure 12. ADPL42092UJ-EVALZ PCB Layout—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/26	Initial release	—

Notes