Evaluation Board User Guide

ADPL40505A Evaluation Kit

Evaluates: ADPL40505A

General Description

The ADPL40505A evaluation kit (EV kit) evaluates the ADPL40505A. The ADPL40505A is a P-Channel Metal-Oxide Semiconductor (PMOS) Low Drop-Out (LDO) linear regulator. The ADPL40505A EV kit operates over an input range of 1.7V to 5.5V, provides an output-voltage range from 0.8V to 5.0V, and can deliver up to 500mA of current. The EV kit comes with the ADPL40505AATA+ installed.

Benefits and Features

- Evaluates the ADPL40505A in an 8-pin (2mm x 2mm) Thin Dual Flat No-Lead Package (TDFN) Package
- 1.7V to 5.5V Input Supply Range
- 0.8V to 5.0V External Feedback Resistor Configuration
- Up to 500mA Output Current
- Jumper-Selectable Operating Modes
- Proven 2-Layer 1oz Copper Printed Circuit Board (PCB) Layout
- Demonstrates Compact Solution Size
- Fully Assembled and Tested

***Ordering Information* appears at end of data sheet.**

Evaluation Kit Photo

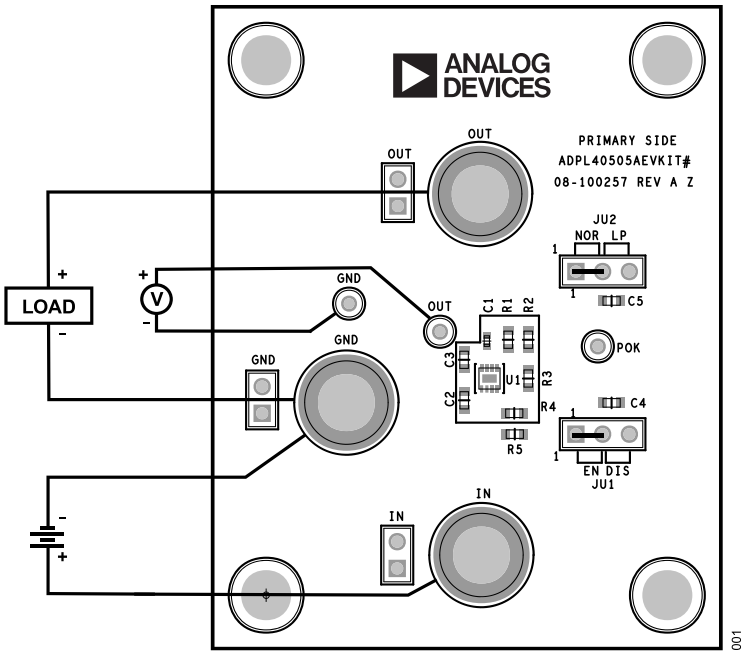

Figure 1. Proper Measurement Equipment Setup

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

©2025 Analog Devices, Inc. All rights reserved.

Quick Start

Required Equipment

- ADPL40505AEVKIT#
- 5.5V, 1A DC Power Supply
- Electronic Load capable of 500mA
- Digital Voltmeter (DVM)

Procedure

The ADPL40505A evaluation kit is easy to set up for evaluating the ADPL40505A. See *Figure 1* for the evaluation kit connections and use the following steps.

Caution: Do not turn on the power supply until all connections are completed.

1. Verify that the jumper JU1 has a shunt across pins 1 and 2 (EV kit enabled) as shown in *Table 1*.
2. Verify that the jumper JU2 has a shunt across pins 1 and 2 (Normal mode) as shown in *Table 2*.
3. Connect the 1.7V power supply between the IN and GND banana jacks.
4. Connect the 500mA electronic load between the OUT and GND banana jacks.
5. Connect the DVM between the OUT and GND test points.
6. Turn on the power supply.
7. Enable the electronic load.
8. Verify that the output voltage is approximately 1.0V.

Detailed Description of Hardware

The ADPL40505A evaluation kit evaluates the ADPL40505A. The ADPL40505A is a PMOS linear regulator that delivers 500mA of output current with 45μV_{RMS} of output noise from 10Hz to 100kHz. The ADPL40505A has a Power Supply Rejection Ratio (PSRR) of 60dB at 10kHz, 250mA load, and a 300mV input and output voltage separation.

The EV kit operates over an input range of 1.7V to 5.5V. The EV kit comes with the ADPL40505AATA+ installed. The EV kit's output voltage is set to 1.0V by external feedback resistors R1 and R2. The EV kit can deliver up to 500mA of current in Normal mode. In Low-Power mode (LPM), the output current limit is configured up to 20mA, and has a no-load quiescent current of 20µA.

EN (Enable)

The EV kit provides a jumper JU1 to enable or disable the ADPL40505A. See *Table 1* for JU1 jumper settings.

Table 1. EN (JU1)

JU1 SHUNT POSITION	DESCRIPTION
1 to 2*	Enabled. EN = IN
2 to 3	Disabled. EN = GND

**Default* *Position*

MODE (Mode Selection)

The EV kit provides a jumper JU2 to select between Normal and Low-power modes for the ADPL40505A. See *Table 2* for JU2 jumper settings.

Table 2. MODE (JU2)

JU2 SHUNT POSITION	DESCRIPTION
1 to 2*	Normal. MODE = IN (Output Current up to 500mA)
2 to 3	LPM. MODE = GND (Output Current up to 20mA)

**Default Position*

POK (Power OK)

The EV kit provides a test point to monitor the POK status of the ADPL40505A. POK is pulled up to OUT via resistor R3 to create a signal that goes high after the regulator output has reached its regulation voltage. POK can also be pulled up to IN, the input supply via resistor R4 (after removing R3 and installing a resistor on R4).

Evaluating Other Output Voltages

The EV kit can evaluate the ADPL40505A in other output voltages, between 0.8V and 5.0V, after replacing external feedback resistors R1 and R2. For more information on calculating the output voltage feedback resistor values, refer to the *Output Voltage Configuration* section in the *ADPL40505A IC data sheet*.

Ordering Information

PART	TYPE
ADPL40505AEVKIT#	EV Kit

#Denotes RoHS-compliant.

ADPL40505A EV Kit Bill of Materials

ITEM	QUANTITY	REFERENCE DESIGNATOR	PART DESCRIPTION	MANUFACTURER, PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	1	C1	0.01µF Capacitor, X7R, 50V, 10%, 0402	MURATA, GRM155R71H103KA88D
2	2	C2, C3	4.7µF Capacitor, X7R, 16V, 10%, 0603	MURATA, GRM188Z71C475KE21D
3	1	R1	200kΩ Resistor, 1%, 1/10W, 0603	VISHAY, CRCW0603200KFK
4	1	R2	301kΩ Resistor, 1%, 1/16W, 0603	TE CONNECTIVITY, CPF0603F301KC
5	1	R3	100kΩ Resistor, 0.1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERA-3AEB104V
6	1	R5	0Ω Resistor, Jumper, 1/10W, 0603	VISHAY, CRCW06030000Z0EA
7	1	U1	5.5V, 500mA LDO Linear Regulator with Low-Power Mode	ANALOG DEVICES INC., ADPL40505AATA+
OPTIONAL EVALUATION KIT COMPONENTS				
1		C4, C5	Capacitor, 0603, Optional	
2		R4	Resistor, 0603, Optional	
HARDWARE				
1	3	J1 (IN), J2 (GND), J3 (OUT)	Banana Jack Connector, Female, Non-insulated, Swage	KEYSTONE, 575-4
2	2	JU1, JU2	Connector, Header, Male, 1 x 3, 2.54mm, Vertical, Straight, through Hole	SULLINS, PEC03SAAN
3	1	TP3 (POK)	Test Point, through Hole, White	KEYSTONE, 5002
4	1	TP4 (OUT)	Test Point, through Hole, Red	KEYSTONE, 5000
5	1	TP5 (GND)	Test Point, through Hole, Black	KEYSTONE, 5001
6	2	XJU1, XJU2	Test Point; Shunt and Jumper, 2 (1 x 2) Position, Black	SAMTEC INC, SNT-100-BK-G

ADPL40505A EV Kit Schematic Diagram

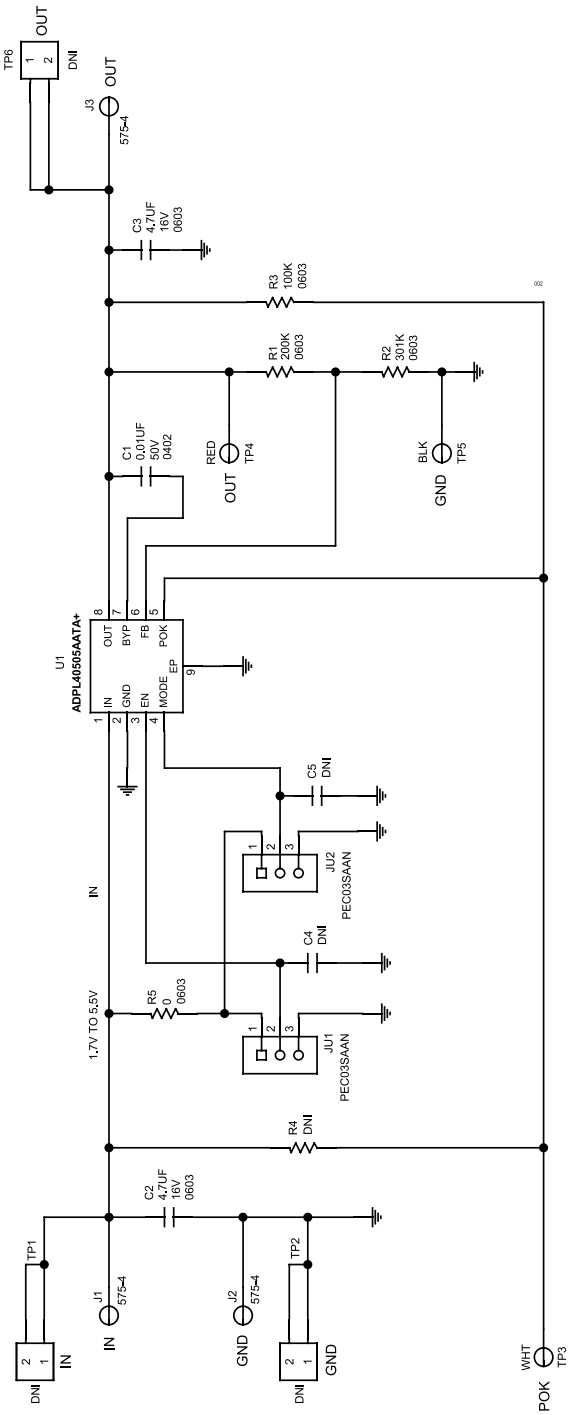

Figure 2. ADPL40505A EV Kit Schematic Diagram

ADPL40505A Evaluation Kit PCB Layout Diagrams

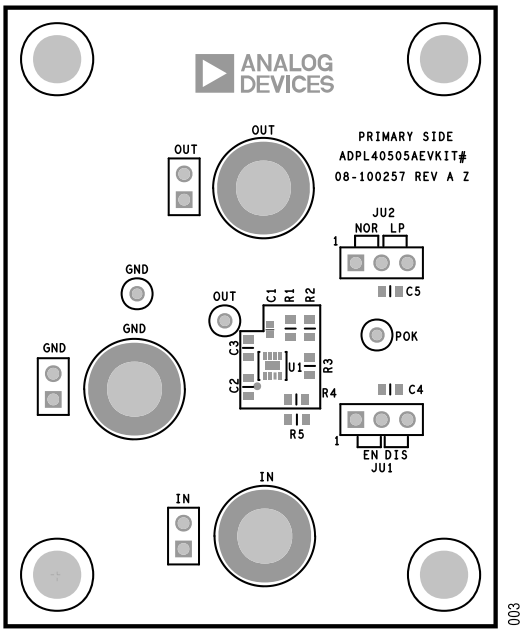

Figure 3. ADPL40505A EV kit Component Placement Guide—Top Silkscreen

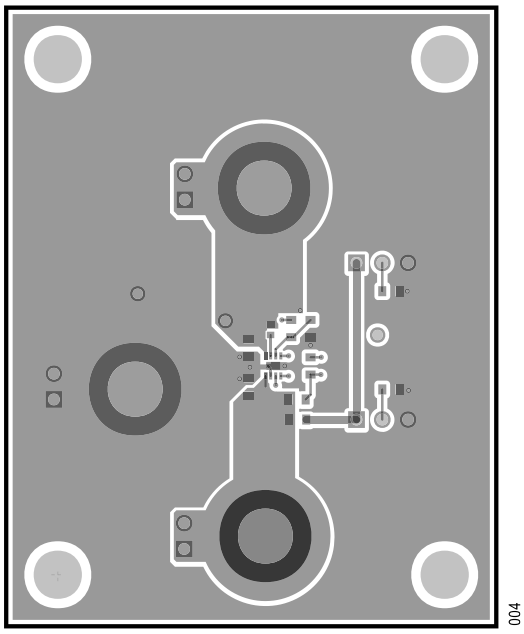

Figure 4. ADPL40505A EV kit PCB Layout—Top Layer (Top View)

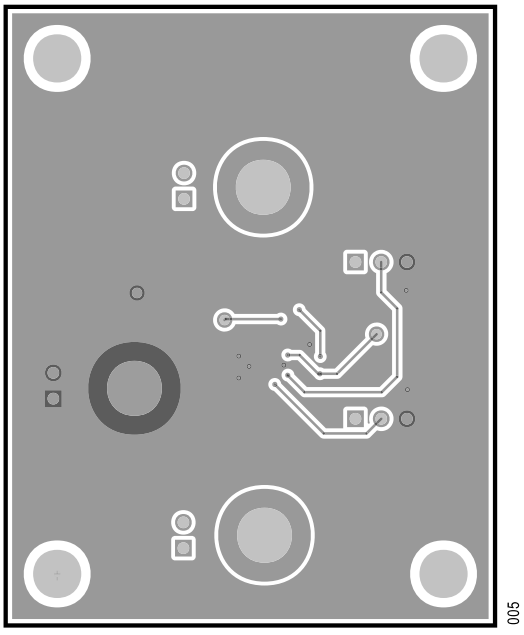

Figure 5. ADPL40505A EV kit PCB Layout—Bottom Layer (Top View)

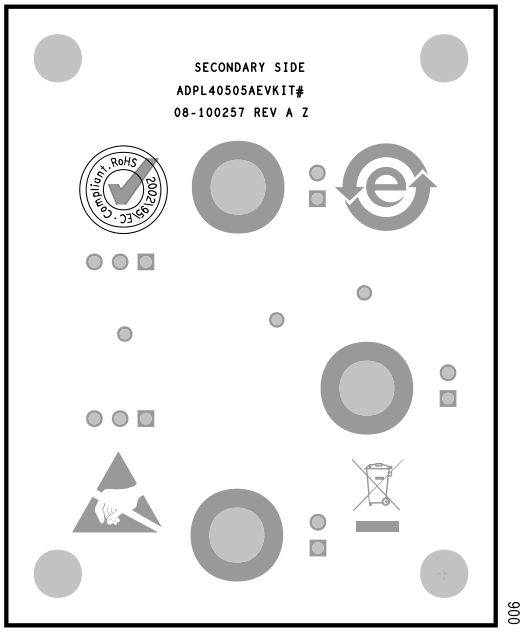

Figure 6. ADPL40505A EV kit Component Placement Guide—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/25	Initial release	—

Notes

ALL INFORMATION CONTAINED HEREIN IS PROVIDED “AS IS” WITHOUT REPRESENTATION OR WARRANTY. NO RESPONSIBILITY IS ASSUMED BY ANALOG DEVICES FOR ITS USE, NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THIRD PARTIES THAT MAY RESULT FROM ITS USE. SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. NO LICENSE, EITHER EXPRESSED OR IMPLIED, IS GRANTED UNDER ANY ADI PATENT RIGHT, COPYRIGHT, MASK WORK RIGHT, OR ANY OTHER ADI INTELLECTUAL PROPERTY RIGHT RELATING TO ANY COMBINATION, MACHINE, OR PROCESS, IN WHICH ADI PRODUCTS OR SERVICES ARE USED. TRADEMARKS AND REGISTERED TRADEMARKS ARE THE PROPERTY OF THEIR RESPECTIVE OWNERS. ALL ANALOG DEVICES PRODUCTS CONTAINED HEREIN ARE SUBJECT TO RELEASE AND AVAILABILITY.