Evaluation Board User Guide

ADPL40501 Evaluation Board

Evaluates: ADPL40501

General Description

The ADPL40501 evaluation board evaluates the ADPL40501, a 5.5V, 100mA, low noise, CMOS, linear regulator. The board features a 5-lead TSOT package.

The evaluation board provides an adjustable output over an input range of 2.2V to 5.5V. The maximum output current is 100mA. The evaluation board uses the adjustable version of the ADPL40501. A resistor divider programs the output of the adjustable ADPL40501 to 2V. The evaluation board can easily be configured for fixed output versions of the ADPL40501 by removing the jumper, which normally connects the resistor divider to the output.

In addition to connectors for the input voltage, output voltage, EN control signal and ground, the evaluation board provides test points for the input, output, ADJ, and EN voltages. A jumper normally connects the EN pin to the VIN input, but it can be removed so that EN can be driven externally at its connector instead.

For more details, refer to the ADPL40501 data sheet, which must be consulted in addition to this user guide when using the ADPL40501 evaluation board.

Features and Benefits

- Input Voltage Range for Programmed Output Voltage of the Board: 2.5V to 5.5V
- Resistor Programmed: 2V Output Voltage
- Maximum Output Current: 100mA
- Jumper Turns the Regulator On by Connecting the EN Pin to the VIN Pin, or Using an External EN Signal to Turn the Regulator ON When the Jumper is Removed
- Jumper Connects the ADJ Pin to the VOUT Pin Through a Resistor Divider
- VIN, VOUT, and GND Test Points for Regulations and Dropout Voltage Monitoring
- ADJ Test Point for Adjustable Output Voltage Monitoring
- 5-Lead (1.5mm x 1.5mm) TSOT Package

Ordering Information ***appears at end of data sheet.***

Quick Start

Required Equipment

- DC power supply
- Multimeters for voltage and current measurements
- Electronic or resistive loads

Procedure

The ADPL40501 evaluation board is simple to set up to evaluate the performance of the ADPL40501. See *Figure 1* for the evaluation board connections, and follow the steps below:

1. Connect the load between the VOUT and GND terminals.
2. With the input power supply off and turned down, connect the input supply to the V_{IN} and GND terminals. Ensure that the shunt on JP1 connects EN to VIN, according to the jumper connection guide. Also, ensure that the shunt on JP2 allows the resistor divider to program the output to 2V, according to the jumper connection guide.
3. With the load turned down, turn on the input power supply and increase the voltage to 2.5V or higher.
4. Vary V_{IN} from 2.5V to 5.5V and the load current from 0A to 100mA. Observe conservative power dissipation limits.
5. Monitor the regulation and dropout voltage at the VIN, VOUT, and GND test points.
6. To monitor the operating supply current, connect the evaluation board as shown in *Figure 2*. It is highly recommended to use a resistor as the load for this parameter. Because the expected value is small, ensure that there are no other connections on the evaluation board.
7. To apply an EN signal externally, remove jumper JP1 and apply the EN signal to the EN connector.
8. If an output voltage other than 2V is desired, change resistors R1 and R2.
9. JP2 is a convenient way to disconnect the ADJ pin from the output if a fixed-output ADPL40501 is installed. The feedback divider resistors, R1 and R2, may also be removed.

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Evaluation Board Connection

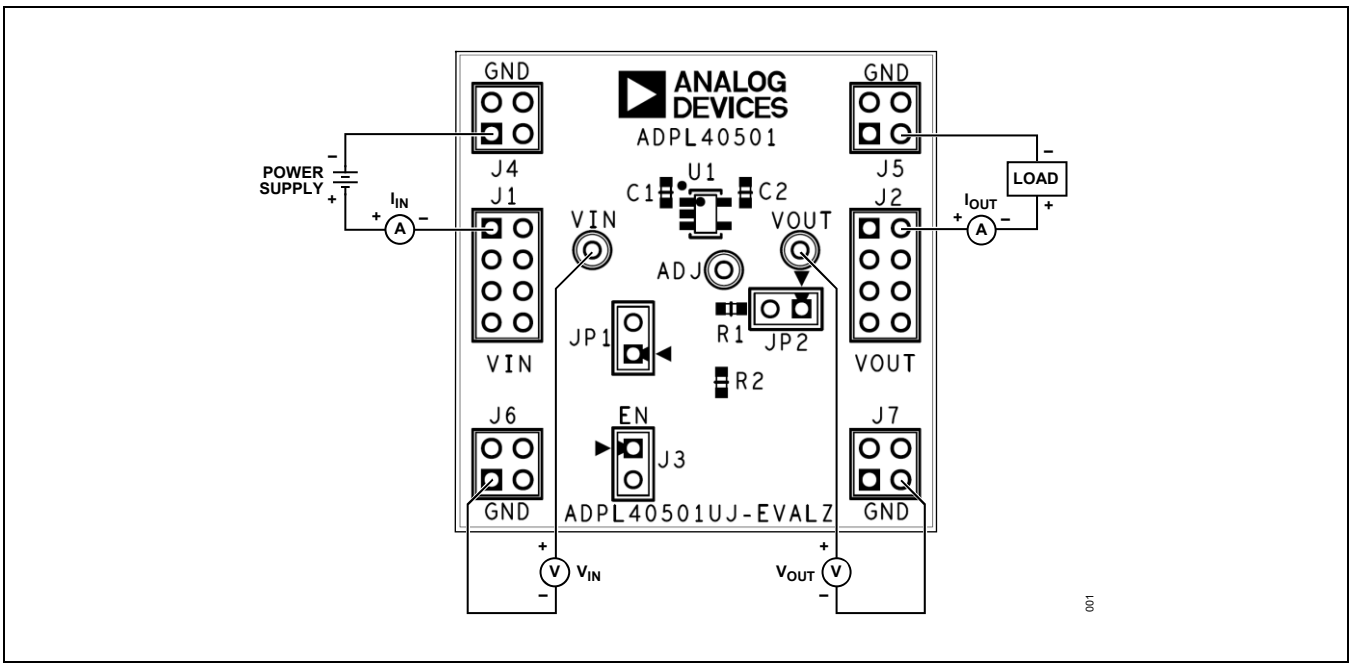


Figure 1. Input and Output Voltage and Current Measurement Setup

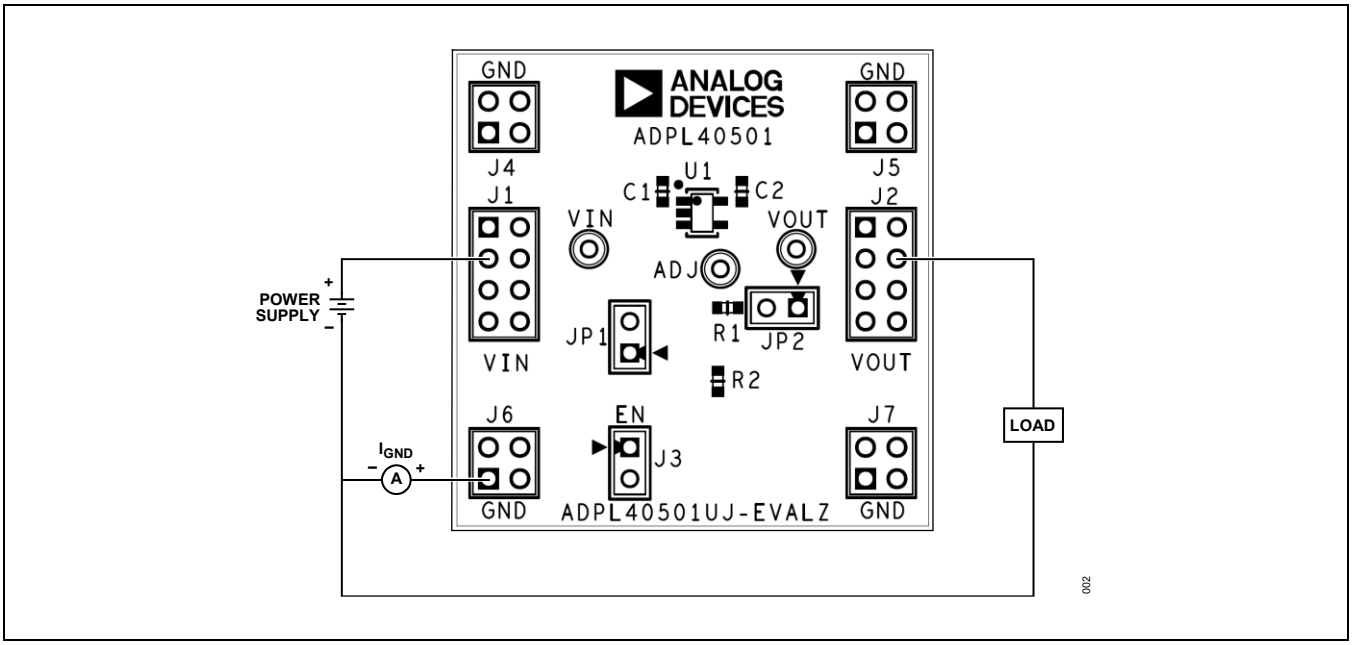


Figure 2. Ground Current Measurement Setup

ADPL40501 Evaluation Board

Performance Summary

Specifications are at T_A = +25°C, unless otherwise noted.

Table 1. Performance Summary of the Evaluation Board

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	I_{OUT} = 10mA to 100mA, V_{OUT} = 2V	2.5		5.5	V
Output Voltage	V_{OUT}	V_{IN} = 5V, I_{OUT} = 100mA, R1 = 100kΩ, R2 = 100kΩ	1.97	2.00	2.03	V
Operating Supply Current	I_{GND}	I_{OUT} = No load, R1 = 100kΩ, R2 = 100kΩ			12	µA
		I_{OUT} = 100mA, R1 = 100kΩ, R2 = 100kΩ		40		µA
Shutdown Current	I_{GND_SD}	Remove jumper JP1, EN = GND, V_{IN} = 5V			1	µA

Printed Circuit Board (PCB) Layout

The printed circuit board (PCB) for this evaluation board is 0.0625 inches thick and 1.5 inches square. It has two copper layers, and the finished copper thickness is 1 ounce. The input capacitor, ADPL40501, and output capacitor are all placed on the top side of the PCB. The input and output capacitors are placed near the ADPL40501, with their ground terminals close to each other. The input capacitor, output capacitor, and ADPL40501 grounds all connect on one side of the device, while the grounds for control signals connect to the ADPL40501 on the other side. The bottom side of the PCB is a solid ground plane that connects to the ground on the top PCB layer through thermal vias located under or near the ADPL40501 and at other points. Layout can significantly affect the electrical performance and reliability of the circuit.

Jumper Connection Guide

JUMPER	DEFAULT CONECTION	FEATURE
JP1	Pin 1-2	Turns regulator on
JP2	Pin 1-2	Connects the resistor divider to the output

Ordering Information

MODEL[1], [2]	PACKAGE DESCRIPTION
ADPL40501UJ-EVALZ	TSOT package evaluation board

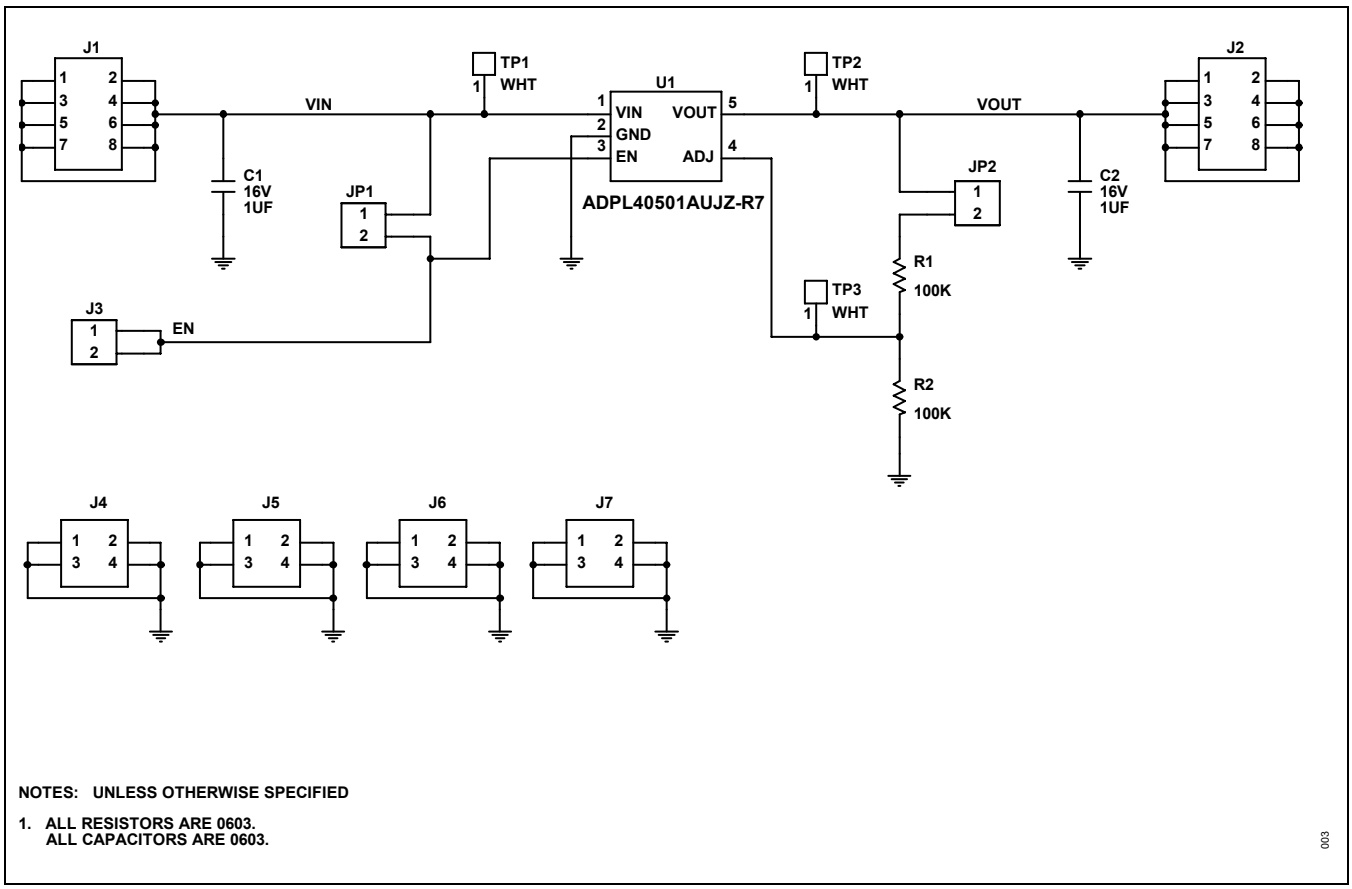
[1] *Z = RoHS compliance part.*

[2] *The evaluation board is preconfigured with an adjustable ADPL40501.*

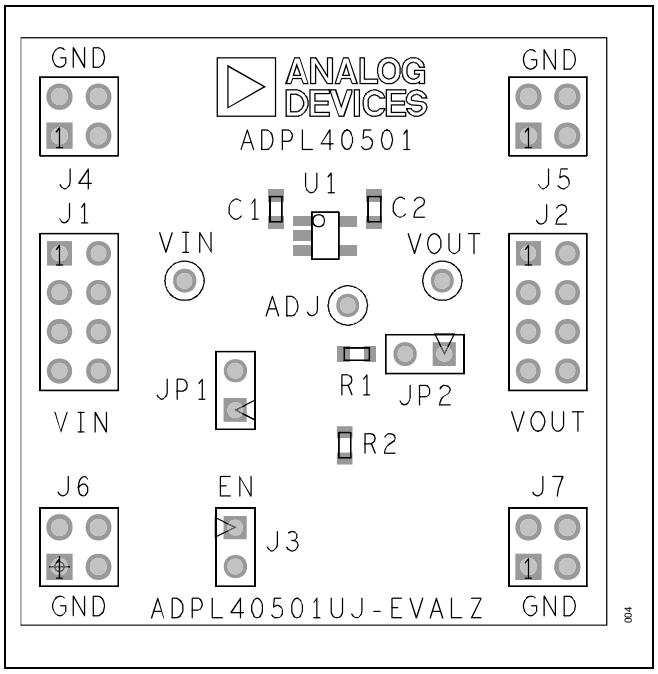
ADPL40501 Evaluation Board Bill of Materials

ITEM	QUANTITY	REFERENCE DESIGNATOR	PART DESCRIPTION	MANUFACTURER, PART NUMBER
Required Circuit Components				
1	2	C1, C2	1µF, capacitors, X7R, 16V, 10%, 0603, AEC-Q200	MURATA, GCM188R71C105KA64D
2	2	R1, R2	100kΩ, resistors, 1%, 1/10W, 0603, AEC-Q200	VISHAY, CRCW0603100KFKEA
5	1	U1	5.5V, 100mA, ultra-low quiescent current, CMOS linear regulator	Analog Devices Inc., ADPL40501AUJZ-R7
Hardware				
1	2	J1, J2	Connectors, header, male, 2 x 4, 2.54mm, vertical, straight, through hole	SULLINS, PEC04DAAN
2	3	J3, JP1, JP2	Connectors, header, male, 1 x 2, 2.54mm, vertical, straight, through hole	SULLINS, PEC02SAAN
3	4	J4 to J7	Connectors, header, male, 2 x 2, 2.54mm, vertical, straight, through hole	SULLINS, PEC02DAAN
4	2	XJP1, XJP2	Connectors, shunt, female, 2 position, 2.54mm	SULLINS, SPC02SYAN

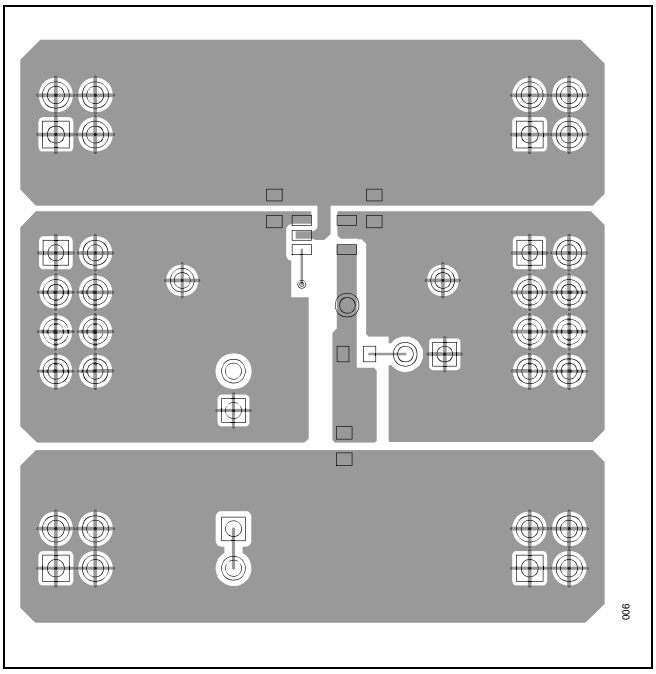
ADPL40501 Evaluation Board Schematic



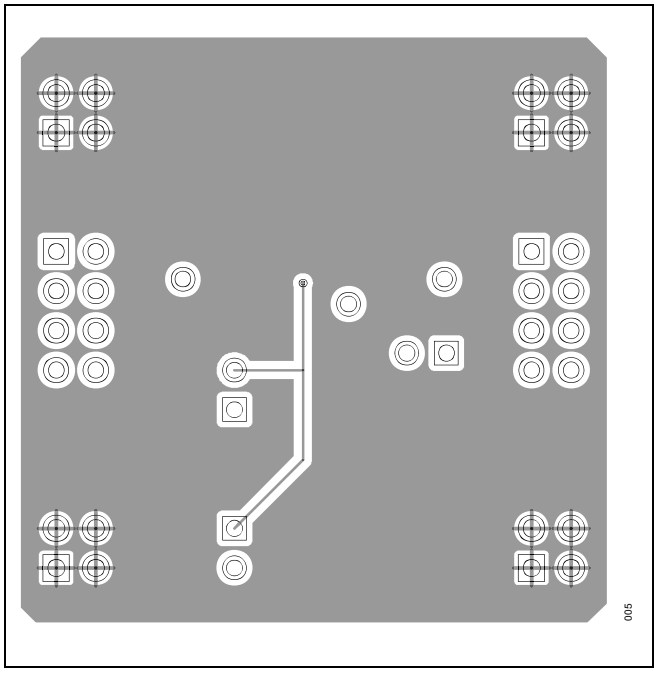
ADPL40501 Evaluation Board PCB Layouts



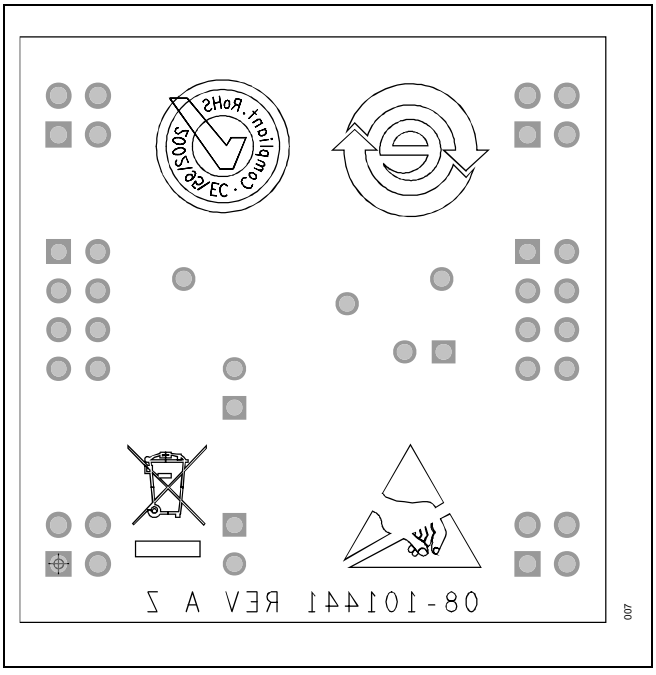
ADPL40501 Evaluation Board—Top Silkscreen



ADPL40501 Evaluation Board—Top



ADPL40501 Evaluation Board—Bottom



ADPL40501 Evaluation Board—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/26	Initial release	—

Notes