Evaluation Board User Guide

ADPL12003 EV KIT

Evaluates: ADPL12002 and ADPL12003

General Description

The ADPL12003 evaluation kit (EV kit) provides a proven design to evaluate the ADPL12002/ADPL12003, high input-voltage, mini buck converter in a 15-pin, 17-pin flip-chip quad flat no-lead (FC2QFN) package. Various test points and jumpers are included for evaluation. The ADPL12003 EV kit comes with the ADPL12003AFLB+ installed (3.3V, 1.5MHz). This EV kit can be used to evaluate all variants of the ADPL12002/ADPL12003 with minimal component changes.

Benefits and Features

- Input Supply Range from 3V to 20V
- Adjustable Output Voltage Range between 0.8V and 12V
- Delivers up to 3.5A Output Current (up to 2.5A for the ADPL12002)
- Frequency Synchronization Input
- 99% Duty Cycle Operation with Low Dropout
- Voltage-Monitoring PGOOD Output with UV/OV Feature
- Proven Printed Circuit Board (PCB) Layout
- Fully Assembled and Tested

***Ordering Information* appears at end of data sheet.**

Quick Start

Required Equipment

- ADPL12003 EV Kit
- Power Supply (PS)
- Voltmeter
- Electronic Load

Procedure

The EV kit is fully assembled and tested. Use the following steps to verify board operation:

1. While observing safe Electrostatic discharge (ESD) practices, carefully unbox the ADPL12003 EV kit board from its packaging. Inspect the board to ensure that no damage has occurred during the shipment. Jumpers/shunts are preinstalled before testing and packaging.
2. Verify that all jumpers are in their default positions, as shown in *Table 1*.
3. Connect the positive and negative terminals of the power supply to the VSUP and GND2 test pads, respectively.
4. Connect the positive terminal of the voltmeter to V_{OUT}, and the negative terminal to GND3.
5. Set the power supply to 12V and a 3A current limit. Turn on the power supply.
6. The voltmeter should display an output voltage of 3.3V.
7. Connect an electronic load to the V_{OUT} and GND3 terminals and set it to 1A.
8. Turn on the electronic load and increase the current to 3.5A. The voltmeter should display an output voltage of 3.3V.

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Detailed Description

This ADPL12003 EV kit should be used with the following documents:

- ADPL12002/ADPL12003 data sheet
- ADPL12003 EV kit data sheet (this document)

The EV kit provides a proven layout for all ADPL12002/ADPL12003 synchronous buck converter variants. The device accepts input voltages as high as 20V and delivers up to 3.5A (2.5A for the ADPL12002).

Switching Frequency/External Synchronization

The device can operate in two modes: Forced–Pulse-width modulation (PWM) or Skip mode. Skip mode has better efficiency for light-load conditions. When SYNC is pulled low, the device operates in skip mode for light loads and PWM mode for larger loads. When SYNC is pulled high, the device is forced to operate in PWM across all load conditions. Use jumper J2 to switch modes.

SYNC can also be used to synchronize with an external clock. The device operates in FPWM mode when SYNC is connected to an external clock. To do this, uninstall the J2 shunt and connect an external clock to the SYNC pin.

Buck Output Monitoring (PGOOD)

The EV kit provides a power-good output test point (PGOOD) to monitor the status of the buck output. PGOOD is high impedance when the output voltage is in regulation. PGOOD is low impedance when the output voltage drops below 7% (typ) or exceeds 4% (typ) of its nominal regulated voltage. To obtain a logic signal, pull up PGOOD to V_{BIAS} by installing a shunt on jumper J3.

Programming Buck Output Voltage

The ADPL12002/ADPL12003 has an adjustable 0.8V to 12V output. An external divider connected between the buck output (FB) and GND sets the output voltage. To program the output voltage, place the appropriate resistors in the positions of R4 and R5 according to the following equation:

$$R_4 = R_5 \times \left[\left[\frac{V_{OUT}}{V_{FB}}\right] - 1\right]$$

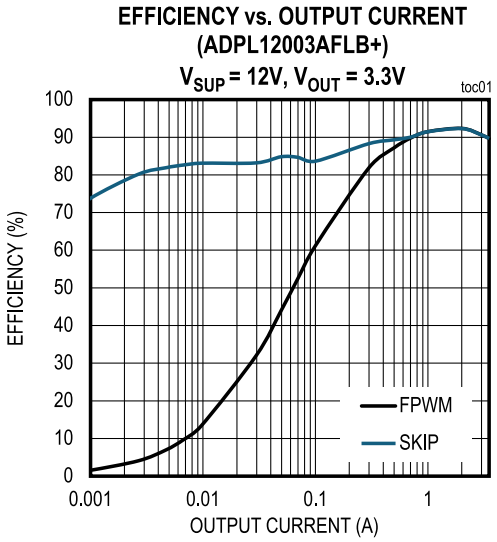
Where V_{FB} = 0.8V and R_5 = 10kΩ–50kΩ, and replace the output capacitors C12–C17 with appropriate capacitors. Refer to *Table 1* in the *ADPL12002/ADPL12003 IC data sheet* for the C19 value.

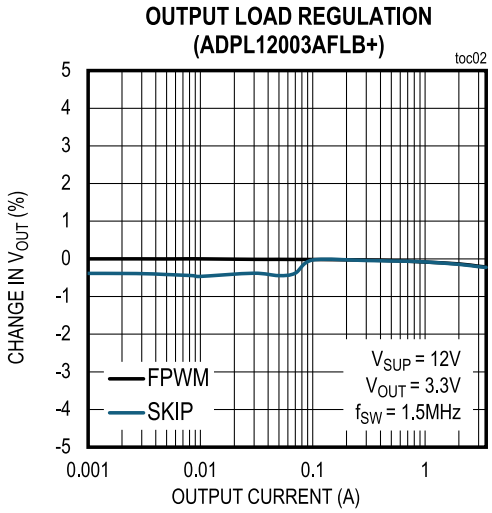
A feedforward capacitor, C19, in parallel with R_4 is also recommended to improve loop stability and bandwidth. Refer to *Table 1* in the *ADPL12002/ADPL12003 IC data sheet* for the C19 value.

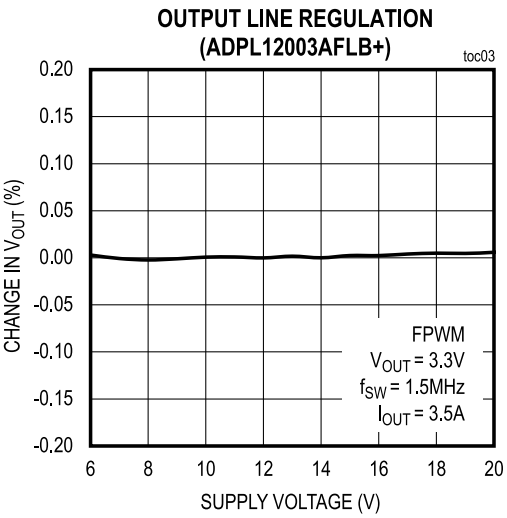
Evaluating Other Variants

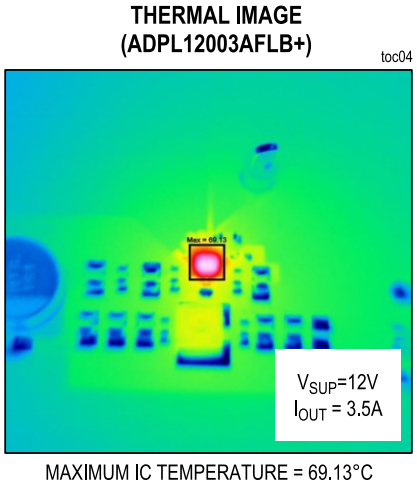
The ADPL12003 EV kit comes installed with the 3.3V/1.5MHz, 3.5A variant (ADPL12003AFLB+). Additionally, a 400kHz variant with an inductor for a 3.3V output is also available. The other ADPL12002/ADPL12003 variants can be installed with minimal component changes.

Evaluation Data









MAXIMUM IC TEMPERATURE = 69.13°C

Table 1. Default Jumper Settings

JUMPER	SHUNT POSITION	FUNCTION
J1_EN	Pins 1–2	Buck controller enabled
J2_SYNC	Pins 1–2	FPWM mode
J3_PGOOD	Installed	PGOOD is pulled up to BIAS when OUT is in regulation
J4_SPS	Pins 1–2	Spread spectrum disabled

Ordering Information

PART	TYPE
ADPL12003EVKIT#	3.3V Output, 1.5MHz EV Kit

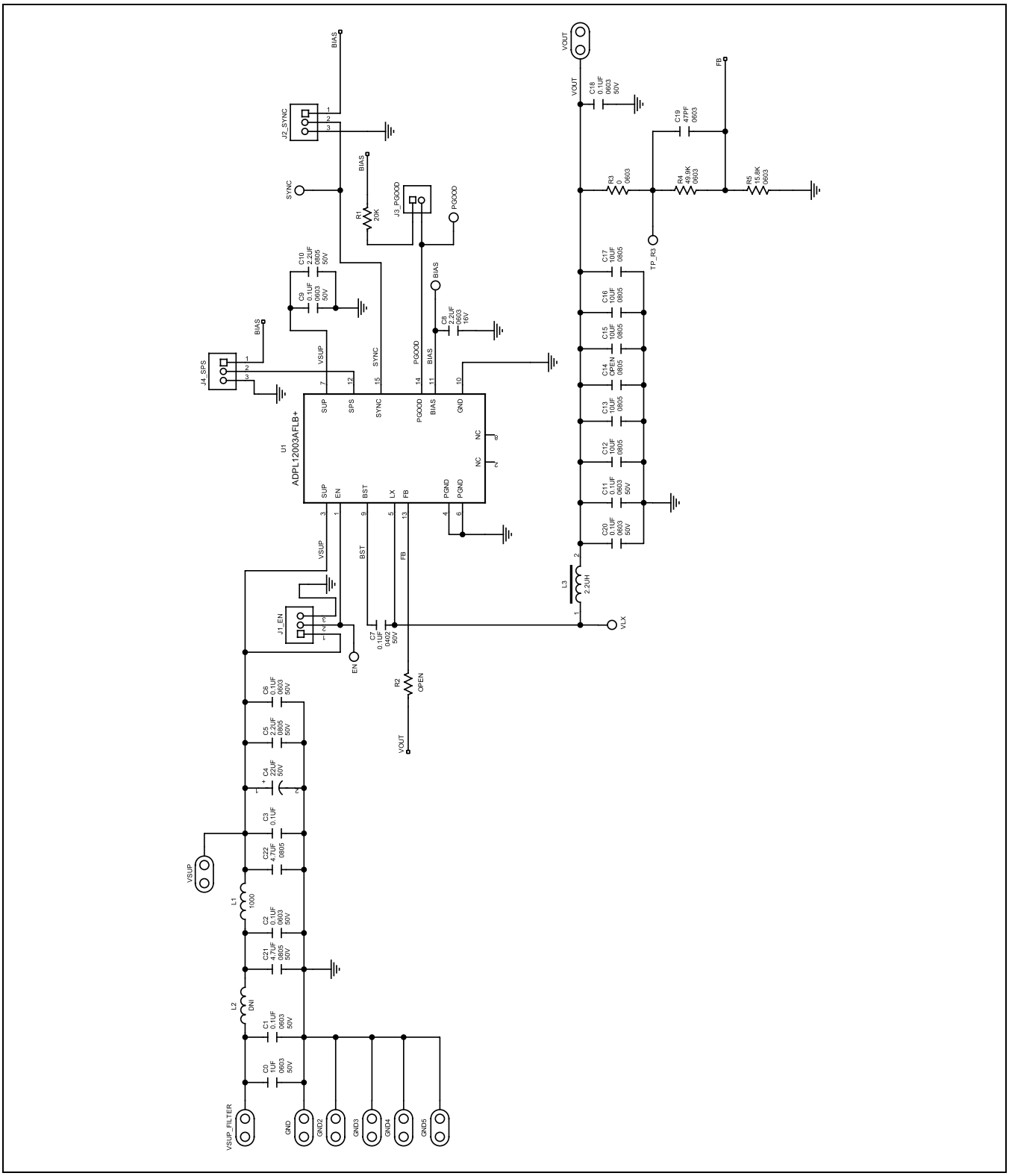
 # Denotes RoHS-compliant.

ADPL12003 EV Kit Bill of Materials

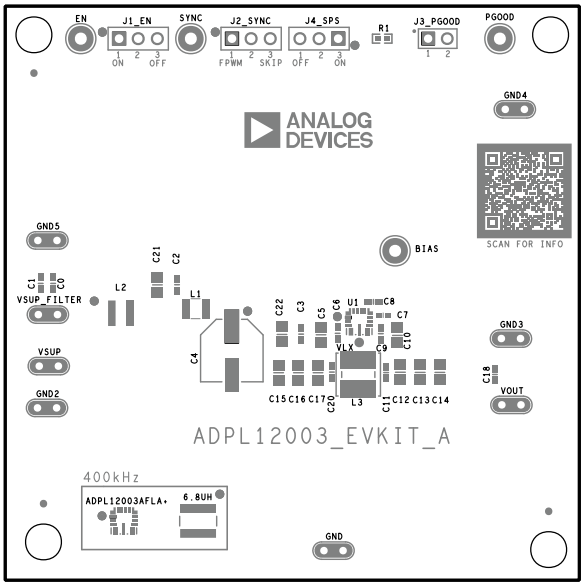
PART	MFG PART #	MANUFACTURER	VALUE	DESCRIPTION
BIAS, EN, PGOOD, SYNC	5012	KEYSTONE	N/A	Test Point Pin Diameter 0.125 inches
C0	UMK107AB7105KA; CC0603KRX7R9BB105	TAIYO YUDEN; YAGEO	1µF	CAP; SMT (0603); 1UF; 10%; 50V; X7R; CERAMIC
C1-C3, C6, C9, C11, C18, C20	CGA3E2X7R1H104K080AE; UMK107B7104KAH	TDK	0.1µF	CAP; SMT (0603); 0.1UF; 10%; 50V; X7R; CERAMIC
C4	EEE-TG1H220P	PANASONIC	22µF	CAP; SMT (CASE_E); 22UF; 20%; 50V; ALUMINUM-ELECTROLYTIC
C5, C10	C2012X7R1H225K125AC	TDK	2.2µF	CAP; SMT (0805); 2.2UF; 10%; 50V; X7R; CERAMIC
C7	CGA2B3X7R1H104M050BB	TDK	0.1µF	CAP; SMT (0402); 0.1UF; 20%; 50V; X7R; CERAMIC
C8	GRM188Z71C225KE43; EMK107BB7225KA	MURATA; TAIYO YUDEN	2.2µF	CAP; SMT (0603); 2.2UF; 10%; 16V; X7R; CERAMIC
C12, C13, C15-C17	CGA4J1X7S1C106K125	TDK	10µF	CAP; SMT (0805); 10UF; 10%; 16V; X7S; CERAMIC
C19	GRM1885C1H470JA01	MURATA	47pF	CAP; SMT (0603); 47PF; 5%; 50V; C0G; CERAMIC
C21, C22	GRM21BZ71H475KE15; C2012X7R1H475K125AC	MURATA; TDK	4.7µF	CAP; SMT (0805); 4.7UF; 10%; 50V; X7R; CERAMIC
GND, GND2-GND5, VOUT, VSUP, VSUP_FILTER	5020	KEYSTONE	N/A	Test Point Diameter 0.094 inches
J1_EN, J2_SYNC, J4_SPS	PEC03SAAN	SULLINS	N/A	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 3PINS
J3_PGOOD	PEC02SAAN	SULLINS	N/A	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 2PINS
L1	FBMH3225HM102N	TAIYO YUDEN	1000	INDUCTOR; SMT (1210); FERRITE-BEAD; 1000 IMPEDANCE AT 100MHZ; TOL=+/-30%; 2A
L2	XGL4020-222ME	COILCRAFT	2.2µH	INDUCTOR; SMT; COMPOSITE; 2.2UH; 20%; 8.9A
L3	XGL4030-222ME	COILCRAFT	2.2µH	INDUCTOR; SMT; COMPOSITE; 2.2UH; 20%; 8.7A

PART	MFG PART #	MANUFACTURER	VALUE	DESCRIPTION
MH1-MH4	9032	KEYSTONE	9032	MACHINE FABRICATED; ROUND-THRU HOLE SPACER; NO THREAD; M3.5; 5/8IN; NYLON
R1	CRCW040220K0FK	VISHAY DALE	20K	RES; SMT (0402); 20K; 1%; +/-100PPM/DEGC; 0.0630W
R3	CRCW06030000Z0EAHP	VISHAY DRALORIC	0	RES; SMT (0603); 0; JUMPER; JUMPER; 0.2500W
R4	CRCW060349K9FK; ERJ-3EKF4992	VISHAY DALE; PANASONIC	49.9K	RES; SMT (0603); 49.9K; 1%; +/-100PPM/DEGC; 0.1000W
R5	AC0603FR-0715K8L; CRCW060315K8FK; ERJ-3EKF1582	YAGEO; VISHAY; PANASONIC	15.8K	RES; SMT (0603); 15.8K; 1%; +/-100PPM/DEGC; 0.1000W
U1	ADPL12003AFLB+	ANALOG DEVICES	N/A	IC ADPL12003 1.5MHz
ADPL12003AFLA+	ADPL12003AFLA+	ANALOG DEVICES	N/A	IC ADPL12003 400kHz
6.8UH	XAL5050-682ME	COILCRAFT	6.8µH	EVKIT PART – INDUCTOR; SMT; COMPOSITE CORE; 6.8UH; TOL=+/-20%; 6.4A

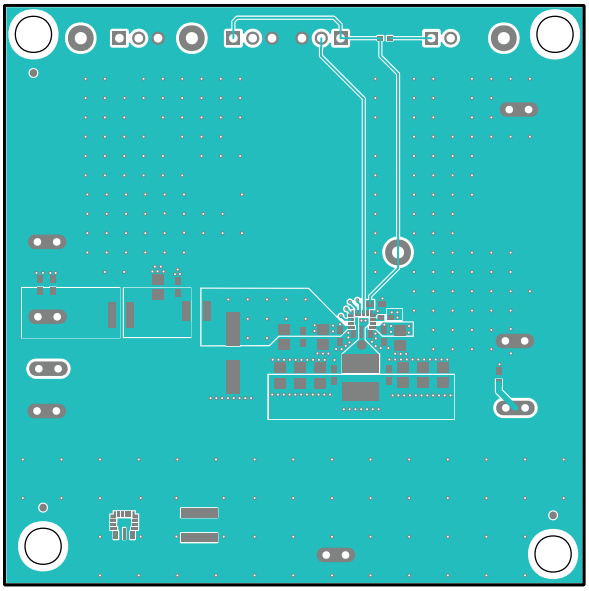
ADPL12003 EV Kit Schematic Diagram



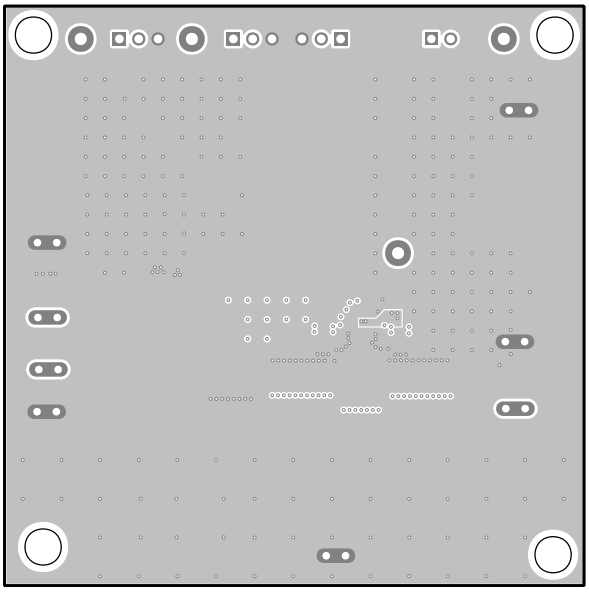
ADPL12003 EV Kit PCB Layout Diagrams



ADPL12003 EV kit Component Placement Guide—Top Silkscreen

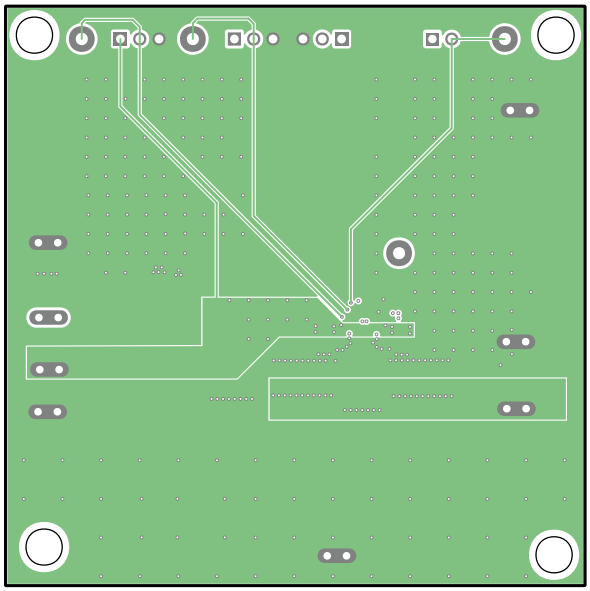


ADPL12003 EV kit PCB Layout—Top View

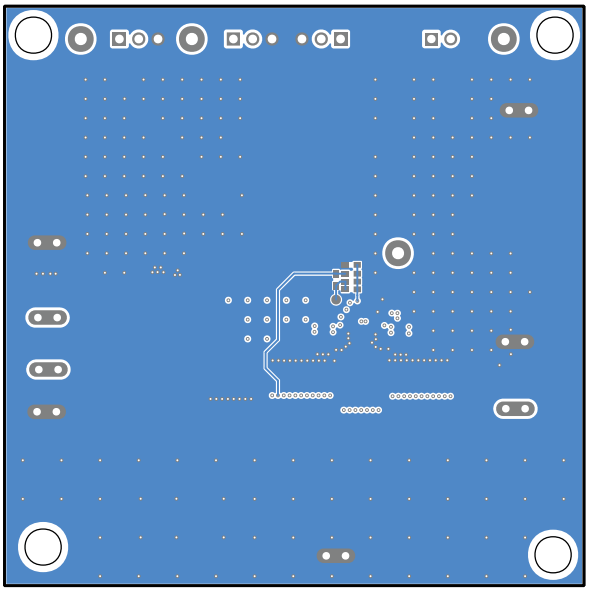


ADPL12003 EV kit PCB Layout—Layer 2

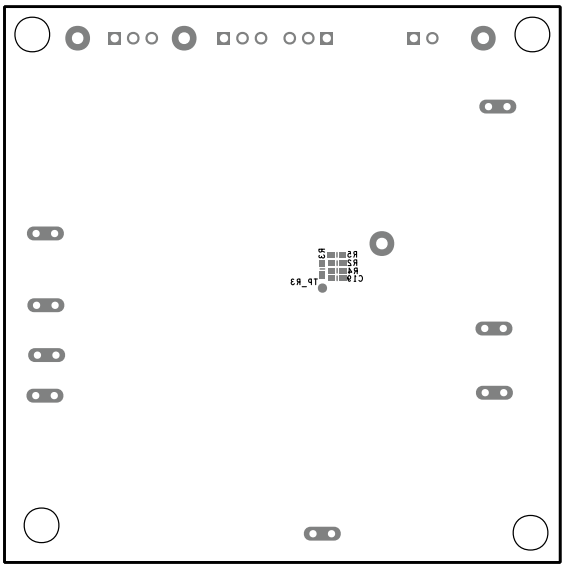
ADPL12003 EV Kit PCB Layout Diagrams (continued)



ADPL12003 EV kit PCB Layout—Layer 3



ADPL12003 EV kit PCB Layout—Bottom View



ADPL12003 EV kit Component Placement Guide—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/25	Initial release	—

Notes