

INTRODUCTION

Accurate energy measurement requires calibration of the measurement system. This reference manual details the calibration procedure of the [ADEMA124/ADEMA127](#). Equations and examples are provided.

The ADEMA124/ADEMA127 have a flexible interface and integrated DSP. Each ADC channel can support voltage dividers, shunts, current transformers (CT) and Rogowski coils. Properly calibrated, the ADEMA124/ADEMA127 will output ADC waveform samples ready for processing by energy metering algorithms.

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REVISION HISTORY

10/2025—Revision 0: Initial Version

ADC CHANNEL CONFIGURATION

ADC timing and channel configuration must be complete before any calibration. The following is general guidance for ADC timing and channel configuration.

ADC TIMING CONFIGURATION

The DATARATE register controls ADC timing. The register contains bit fields to set the clock prescaler, sinc filter decimation rate, and enable the decimation-by-2 feature. Full details on available configurations are described in the Output Sample Rate section of the [ADEMA124/ADEMA127](#) data sheets.

Setting the $\Sigma\Delta$ modulator frequency, f_{MOD} , to 2.048MHz is recommended for the highest ADC resolution. Note that lower f_{MOD} settings may require adjustment of the external anti-aliasing filters to prevent foldback of frequencies greater than $f_{MOD}/2$. See the Anti-Aliasing Filters section of the ADEMA124/ADEMA127 for additional information.

The sinc filter decimation rate sets the DSP frequency, f_{DSP} . The ADC output sample rate, f_S , will be the same as f_{DSP} if the decimate-by-2 feature is not enabled.

The decimate-by-2 feature extends the analog bandwidth for a given output sample rate. This decimation is performed at the output of the DSP. When the DSP_DECIMATION_X2 bit is set, the digital low pass filter block of all active ADC channels must also be enabled to avoid foldback from frequencies greater than $f_{DSP}/2$. See the Bandwidth and Pass-band Flatness section of the ADEMA124/ADEMA127 data sheets for related specifications.

RECOMMENDED DSP CONFIGURATION BY SENSOR

The ADEMA124/ADEMA127 support voltage dividers, shunts, CTs, and Rogowski coils. The DATAPATH_CONFIG_CHx register controls which DSP blocks are enabled on a given ADC channel.

- ▶ Digital Low Pass Filter (LPF_EN_CHx). Enables a low pass filter on the ADC channel. Always enable this filter when the decimate-by-2 feature is enabled in the DATARATE register.
- ▶ Sinc Compensation Filter (COMP_FLT_CFG_CHx and COMP_FLT_EN_CHx). Enables and sets the mode of the sinc compensation filter which corrects for phase and amplitude effects of other filters in the system to improve passband flatness. Two sets of default DSP coefficients are available for this filter. Generally, the COMP_FLT_CFG_CHx bit will be set to 0 for Sinc Droop mode. When the ADC channel is paired with the [ADEMO139A](#), set the COMP_FLT_CFG_CHx to 1 for external BLF and sinc droop compensation. Be aware that if using an input clock frequency not equal to 16.384MHz, the “External BLF and Sinc Droop” mode will not work as expected using the default DSP coefficients.
- ▶ 2nd Order High Pass Filter (HPF) (HPF_EN_CHx). Enables a high-pass filter on the given ADC channel. Recommended to be used on all AC metering channels. This filter is required for any ADC channel connected to an ADEMO139A.
- ▶ Digital Integrator (SCF_EN_CHx). Enables a digital integrator on the selected ADC channel. Required to recover the current waveform from a Rogowski di/dt sensor if not using an external analog integration circuit.
- ▶ All Pass Filter (ALLPASS_EN_CHx). The group delay of this block is matched to the digital integrator block. When the Enable the APF on any channel with the digital integrator not enabled, if using the digital integrator. See [Figure 4](#).
- ▶ Gain, Offset and Crosstalk Correction (GAIN_OFFSET_XT_EN_CHx). Enables the gain and offset DSP correction. Enable this to use high-resolution DSP gain and offset correction for calibration.

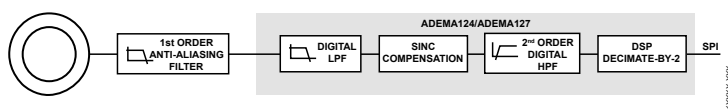


Figure 1. Recommended DSP Configuration for CT

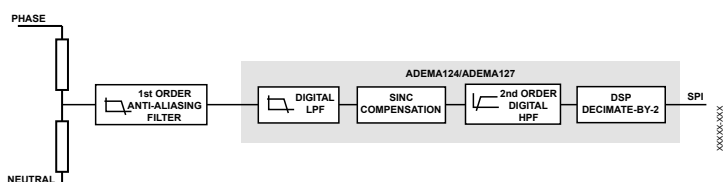


Figure 2. Recommended DSP Configuration for Phase Voltage Sense

ADC CHANNEL CONFIGURATION

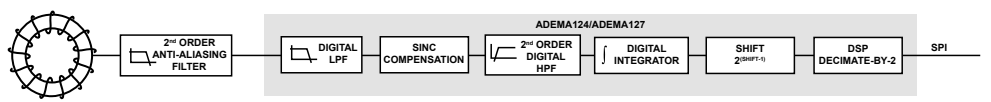


Figure 3. Recommended DSP Configuration for Rogowski Coil

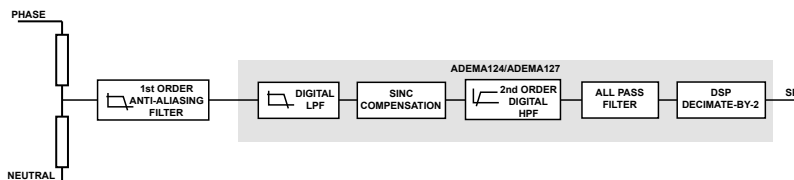


Figure 4. Recommended DSP Configuration for Phase Voltage Sense with for Matched Group Delays to Digital Integrator

SHIFT SETTING

When using the digital integrator DSP block in conjunction with an external Rogowski coil, on the ADC input side the unintegrated signal will be proportional to the di/dt of the measurement current. This means headroom is required to capture faster current signals at the ADC input. After the signal is integrated, the output will therefore occupy a small percentage of the available SPI max codes. The internal digital result from the integrator output is internally represented as a number wider than 24 bits, to avoid quantization errors and make better use of the SPI output headroom the 24-bit “piece” of this result can be moved using the SHIFT field.

This has the effect of multiplying the output codes by $2^{(\text{SHIFT}-1)}$ where SHIFT is the number programmed into the SHIFT byte in the ADC DSP RAM for a given channel.

It is recommended to pick a sensible value of SHIFT such that the maximum value the system is expected to measure does not cause the output signal to clip while also leaving enough headroom.

DSP RAM INITIALIZATION

The ADEMA124/ADEMA127 loads DSP coefficients based on decimation rate and DSP filter selections. The DSP coefficients are characterized for $f_{\text{XTALIN}} = 16.384\text{MHz}$. Other f_{XTALIN} frequencies may require adjustment of the DSP coefficients.

Note the ADEMA124/ADEMA127 DSP initialization routine occurs each time the DATAPATH_CONFIG_LOCK bit changes set from 0 to 1. The implication is all writes to MMR must be completed first or any non-default DSP RAM values will need to be rewritten after accessing the MMR address space. See the Configuration Lock and Access Bits section in the ADEMA124/ADEMA127 data sheets for further information.

COMMON-MODE OFFSET

The ADC_CMI_CHx bits sets the input common-mode voltage expected at the ADC input. For any ADC channels driven by an ADEMO139A, the ADC_CMI_CHx will be set to 1 and ADC_GAIN_CHx set to 0 to accommodate the output characteristics of the amplifiers.

Setting common-mode 1.2V, ADC_CMI_CHx = 1, and gain of 2x, ADC_GAIN_CHx = 1, is not a valid ADC channel configuration.

GAIN CALIBRATION

The DSP gain correction fields are held in the DSP RAM memory area in the [ADEMA124/ADEMA127](#) and the correct sequence must be followed to access them, see the ADEMA124/ADEMA127 data sheets for more information.

In order to simplify PCB layout or optimize channel-channel crosstalk it might be advantageous to wire up some of the ADC channels with inverse polarity. In these cases, you can either use the channel's ADC_INV bit or set a negative value in the GAIN DSP RAM location to correct for this on-chip.

GAIN CALIBRATION: VOLTAGE CHANNELS

The DSP gain correction feature in the ADEMA127 has a correction range of nearly -2 to +2 so should be used to correct for small mismatches in the voltage and current sensors.

For a voltage channel, if using resistor dividers as the voltage sensor, the circuit should look like [Figure 5](#).

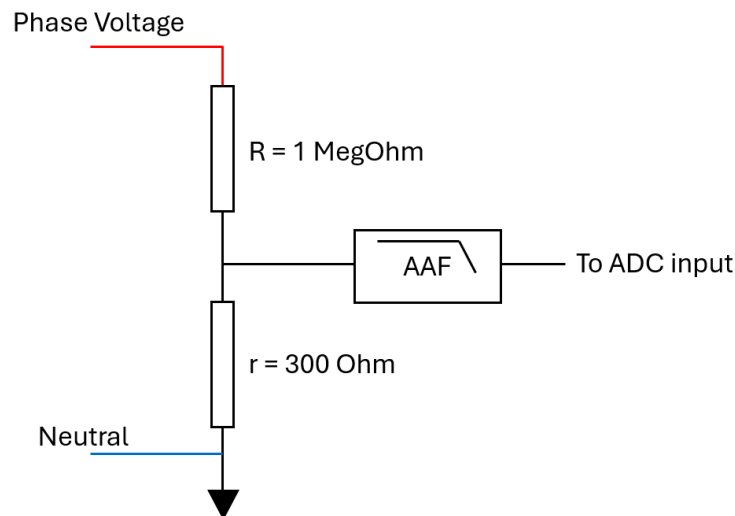


Figure 5. Voltage Sense

In practice, the larger resistor “R” will be split into a number of smaller resistors in a string to achieve PCB creepage and clearance specifications.

The gain correction in this case will correct for component tolerance errors in the resistor divider.

If $V_{\text{PHASE}} = 230\text{Vrms}$ at 50Hz, the voltage at the ADC input ideally should then be

$$V_{\text{ADC_IDEAL}} = 230\text{V} \times \frac{300\Omega}{(300\Omega + 1\text{M}\Omega)} = 68.979\text{mVrms} \quad (1)$$

If you passed an accurate calibration reference voltage of 230Vrms to the phase voltage input and measured $V_{\text{ADC_REAL}} = 70\text{mV}$ this would mean you would need a gain of slightly less than 1 to correct the gain error. This can be calculated by

$$\text{Gain} = \frac{V_{\text{ADC_IDEAL}}}{V_{\text{ADC_REAL}}} = \frac{68.979\text{mV}}{70\text{mV}} = 0.985 \quad (2)$$

To program this value correctly into the ADEMA124/ADEMA127 ADC, it needs to be scaled to the correct 2.22, 24-bit format and then split into bytes, for example:

- ▶ GAIN_LO = 0xFF && (0.987 << 22)
- ▶ GAIN_MD = 0xFF00 && (0.987 << 22)
- ▶ GAIN_HI = 0xFF0000 && (0.987 << 22)

GAIN CALIBRATION

GAIN CALIBRATION: CURRENT CHANNELS

For a Rogowski sensor current channel, the circuit should look like this:

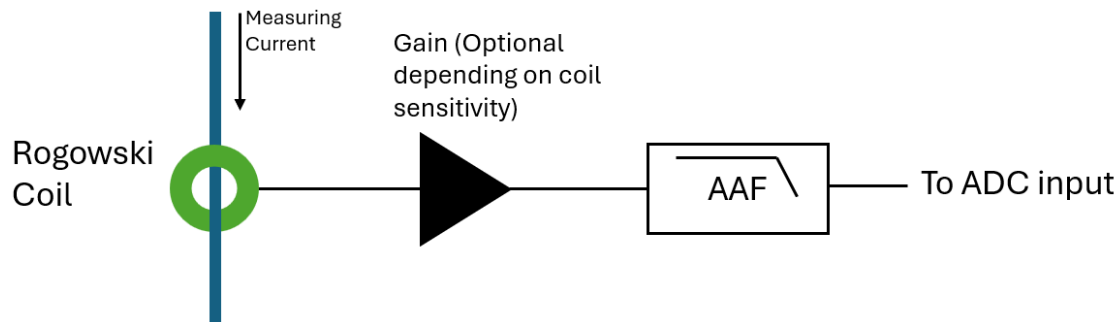


Figure 6. Rogowski Coil Current Sense

In general, a Rogowski coil has a characteristic sensitivity, also referred to as “coil gain” expressed in microvolts per ampere. A coil gain of $4.5\mu\text{V/A}$, for example, would yield $4.5\mu\text{V}$ of voltage at the coil outputs per ampere of current flowing through the inner hole. This number is only valid at one frequency, usually quoted at 50Hz or 60Hz.

If you were to pass an accurate calibration current of known value through the Rogowski coil, the equation to describe the expected ADC input voltage would then be

$$V_{ADC_IDEAL} = I_{IN} \times \text{CoilGain} \times \text{AmpGain} \quad (3)$$

For a worked example, if we pick some values here, say:

- ▶ $I_{IN} = 10\text{Arms}$
- ▶ $\text{CoilGain} = 4.5\mu\text{V/A}$
- ▶ $\text{AmpGain} = 26.37$

We get $V_{ADC_IDEAL} = (10)(4.5 \times 10^{-6})(26.37) = 1.19\text{mV rms}$.

Then if we do an ADC measurement and find that $V_{ADC_REAL} = 1.15\text{mV rms}$, to correct the current channel to its ideal value we will need a value slightly larger than 1, given by

$$\text{Gain} = \frac{V_{ADC_IDEAL}}{V_{ADC_REAL}} = \frac{1.19\text{mV}}{1.15\text{mV}} = 1.03478 \quad (4)$$

The format for loading this value into the ADC DSP RAM and enable its effect is the same as described for the voltage channels.

PHASE ANGLE CALIBRATION

Each ADEMA124/ADEMA127 ADC channel can introduce a time delay to correctly align the ADC channels and correct for small phase differences caused by analog signal conditioning with filters and amplifiers.

Each channel's delay can be set independently. The on-chip delay is a subsample delay and therefore has a range from 0 to 1 sample only. Delays longer than one ADC output sample in time must be performed in software on the host MCU.

Therefore, if a delay corresponding to 2.3 ADC samples in time is needed, the integer part of the delay must be done in software by delaying the desired channel by 2 samples. The fractional 0.3 samples can then be handled on-chip by programming the PHASE_OFFSET_CHx_HI and PHASE_OFFSET_CHx_LO registers.

Table 1 shows the amount of angular correction achievable for subsample time correction.

Table 1. Angular Correction

Line Frequency (Hz)	ADC Data Rate (Samples/Second)	Number of Samples Per Line Cycle	Phase Angle Change Per Sample (Degree)
50	250	5	72
	500	10	36
	1000	20	18
	2000	40	9
	4000	80	4.5
	8000	160	2.25
	16000	320	1.125
	32000	640	0.5625
	64000	1280	0.28125
60	250	4.17	86.4
	500	8.33	43.2
	1000	16.67	21.6
	2000	33.33	10.8
	4000	66.67	5.4
	8000	133.33	2.7
	16000	266.67	1.35
	32000	533.33	0.675
	64000	1066.67	0.3375

In metering systems, the on-chip phase correction can be used to calibrate the meter for an accurate power factor measurement. It is recommended to do this correction with a 60 degree phase shift between voltage and current channels, that is, use a power factor of 0.5 in the calibration signal.

There are a number of ways to measure the angle between two channels:

- ▶ If looking at ADC samples only, an FFT can be performed and the difference between the phase components of the fundamental bin can be converted to an angular measurement in degrees or radians.
- ▶ If metrology is present in the system, it is possible to use power/energy measurements to get the angle (θ) according to the following equation:

$$\tan^{-1}\left(\frac{VarHr}{WattHr}\right) = \theta \quad (5)$$

The other trigonometric identities involve using the apparent power output. VA measurements are often measured in an inherently noisier way than the active and reactive power, so it is recommended to use these instead if possible.

Once the user measures this angle, they can calculate the angular error in the measurement by subtracting it from the ideal angle set by the calibrator.

$$\theta_{ERR} = \theta_{MEAS} - \theta_{IDEAL} \quad (6)$$

Lastly, the angular error needs to be converted from degrees to units of time in terms of number of ADC samples which is described by

$$T_{ERR}(in\ samples) = \frac{\theta_{ERR} \times f_S}{360 \times f_{LINE}} \quad (7)$$

PHASE ANGLE CALIBRATION

Say that $\theta_{ERR} = 0.3^\circ$ with $f_{LINE} = 50\text{Hz}$ and the ADC data rate $ODR = 4\text{ksps}$, then

$$T_{ERR} = (0.3 \times 4000) / (360 \times 50) = 0.0666 \text{ samples of delay.}$$

The correct format for writing these to the part is as follows:

- ▶ `PHASE_OFFSET_CHx_HI = (T_ERR << 13) && 0xFF00`
- ▶ `PHASE_OFFSET_CHx_LO = (T_ERR << 13) && 0x00FF`

It is important to take note that the time delay only works in one direction because it stands to reason that the ADC cannot delay samples before it has measured them. This means that depending on the sign of θ_{ERR} , either the voltage channel or the current channel will need to be delayed to correct for a slightly lagging or leading uncalibrated power factor respectively.

The `PHASE_OFFSET_CHx` registers are not located in DSP RAM in the ADC and require the datapath to be unlocked to write to them. The user should also rewrite previously obtained calibration values (such as channel gains and `SHIFT` value) after re-locking the datapath, because locking the datapath resets the entire DSP RAM. See the Configuration Lock and Access Bits section in the [ADEMA124/ADEMA127](#) data sheets for further information.

SOFTWARE CALIBRATION (PERFORMED AFTER ADC, IN HOST MICROCONTROLLER)

INTEGER SAMPLE DELAY

To extend the phase angle calibration range of the ADC, samples can be buffered in host microcontroller memory to effectively delay them, by aligning them with samples that are captured later.

The amount of memory required for this will be

$$Memory\ Needed\ (bytes) = \frac{N_{samples} \times N_{channels} \times 24bits}{8}$$

(8)

Where N_{samples} is number of samples to delay and N_{channels} is how many channels need to be delayed.

The process of how to go about this is outlined in [Figure 7](#) to [Figure 10](#).

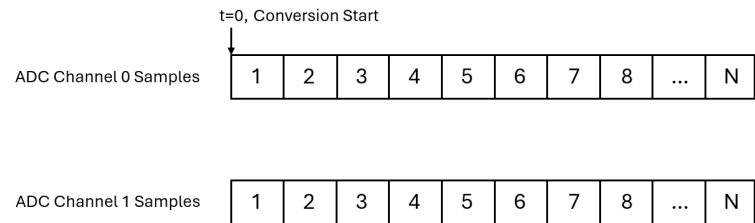


Figure 7. Conversion Start

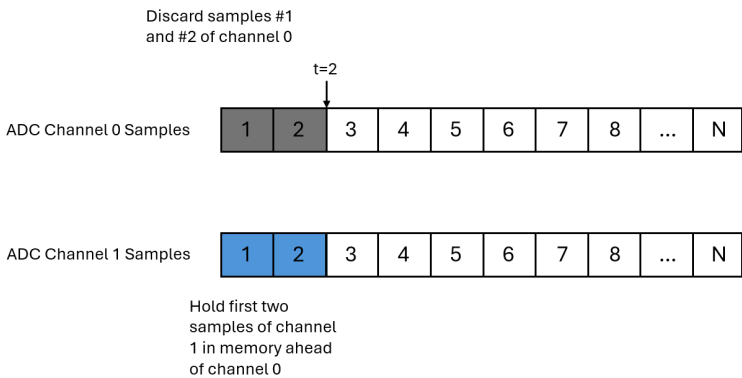


Figure 8. Sample Array Construction

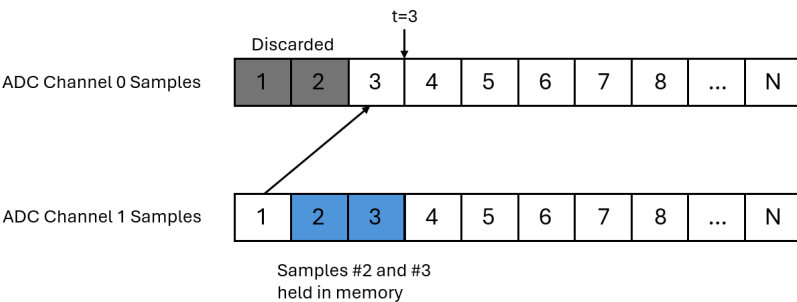
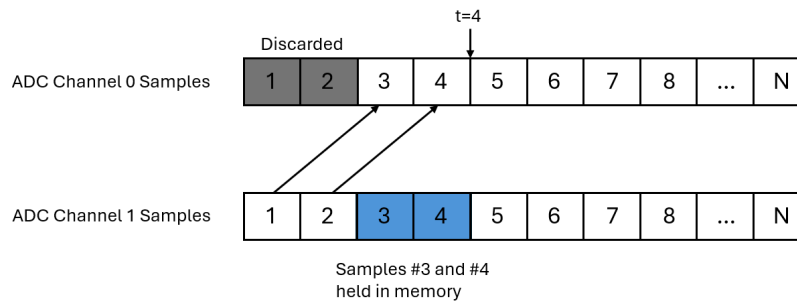


Figure 9. Sample Array Offset for Energy Calculations

SOFTWARE CALIBRATION (PERFORMED AFTER ADC, IN HOST MICROCONTROLLER)**Figure 10. Continued Energy Calculations**

In this way, ADC Channel 1 has effectively been delayed by two samples. For time correction in finer, subsample resolution, the PHASE_OFFSET_CHx registers in the part can be used.

RMS OFFSET CALIBRATION

In an RMS calculation, often the noise is squared with the signal before the samples are averaged together and then the square root is obtained. This introduces a noise-related offset in the RMS readout which can become a significant error source at low currents in Rogowski systems, especially if using a coil with a low sensitivity.

This offset can be corrected by removing it underneath the square root in the RMS equation.

To do this, set the calibrator output to a relatively low current, then read back the RMS using their metrology. The difference between the ideal and measured values of the squared RMS result can be used to correct for this error beneath the square root in the RMS equation, for example.

$$RMS_{CORRECTED} = \sqrt{\frac{1}{n} \sum_{i=1}^n (x_n)^2 - RMS_{OFFSET}^2} \quad (9)$$

$$RMS_{OFFSET} = (RMS_{MEAS})^2 - (RMS_{IDEAL})^2 \quad (10)$$

where:

x_n refers to samples read back from the ADC and subsequently squared and averaged.

RMS_{MEAS} is the readback value before RMS offset correction (that is, the value from Equation 9 with $RMS_{OFFSET} = 0$).

RMS_{IDEAL} is an accurate RMS value read back from the calibration reference equipment.

$RMS_{CORRECTED}$ is the final, calibrated value.

This type of correction is only useful for RMS measurements with challenging system SNR, it should not be required for measurements such as active power and energy.

ELECTROSTATIC COUPLING CORRECTION

In Rogowski systems, there will be some capacitive coupling between the conductor being measured and the Rogowski coil. Although the parasitic capacitance could be in the order of <1pF, the electrostatically coupled signal scales with phase voltage and can introduce an error current signal in the Rogowski coil in the order of a few hundred microamps. This issue is exacerbated if using low sensitivity Rogowski sensors.

At low currents, this will appear as a percentage error in the measurement which can be significant, e.g. 500µA of error at 100mA input current is 0.5%.

The error signal scales with the voltage, and the voltage is being measured in the system- so we can apply gain factor ES_CORR to the voltage signal and subtract it from the current signal.

SOFTWARE CALIBRATION (PERFORMED AFTER ADC, IN HOST MICROCONTROLLER)

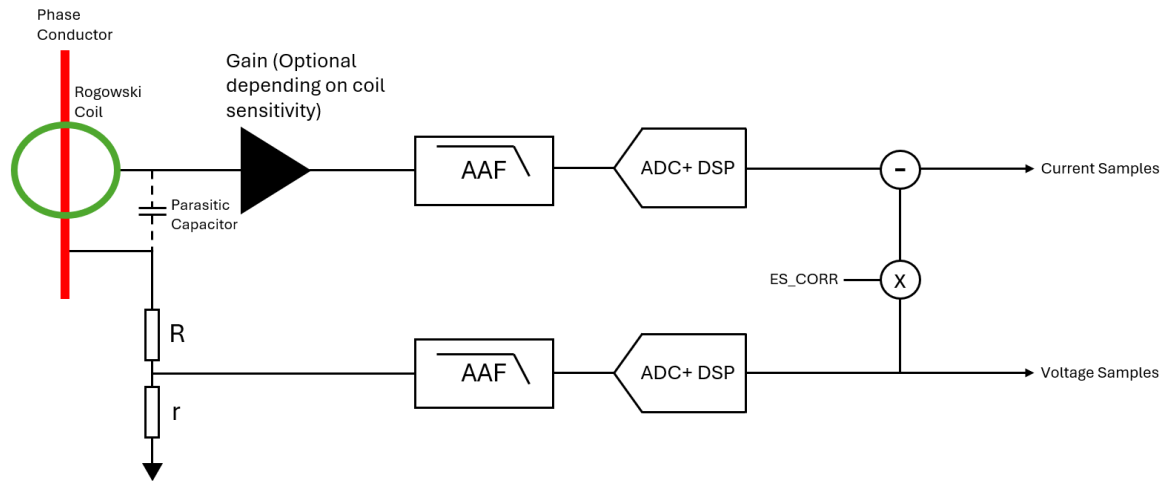


Figure 11. Electrostatic Coupling Correction

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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