A²B ® AD2437 System Specification

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ANALOG DEVICES

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Preface

Thank you for purchasing and developing systems using A^{2}B® transceivers from Analog Devices.

Purpose of This Manual

The *A^{2}B AD2437 System Specification* describes the technical requirements for the A^{2}B® technology which enables next-generation audio connectivity. It describes the functional model, identifies the fault diagnostics, and provides the system level test requirements. This document shall be used to define and develop all production intended solutions. This specification only addresses the lower two layers of the ISO network reference model (physical layer, data link layer). It remains the responsibility of each node supplier to ensure that their nodes fully comply with the requirements set forth in this specification.

WARNING: Failure to comply with the requirements defined in this specification can result in an inability to communicate on the network and lead to degraded performance.

See the applicable programming reference manual for information about the transceivers, including register and bit descriptions.

- *AD2437 A^{2}B Transceiver Technical Reference*

For timing, electrical, and package specifications, see the applicable data sheet.

- *AD2437 A^{2}B Transceiver Data Sheet*

ADI reserves the right to withdraw, modify or replace this specification at any time, without notice.

If there is a difference between the information in this manual and the product data sheet, see the applicable data sheet for the latest specifications.

Revision History

The revision history provides a summary of the major changes in each revision of this document.

Revision	Description of Change
1.0	Initial release

Manual Contents

This manual consists of the following chapters:

- ***Overview*** – Provides an overview of the A^{2}B transceiver and describes the functional blocks.

- ***Transceiver Specifications*** – Describes the operating conditions required for the A^{2}B transceiver.
- ***Functional Model*** – Describes the physical layer and data link layer specifications for the A^{2}B transceiver.
- ***Fault Diagnostic Requirement*** – Describes the line diagnostics during and after discovery, the different types of line faults and the pins affected by the faults.
- ***System Level Test Requirements*** – Provides information on the system level tests that must be performed for A^{2}B operation.
- ***Appendix A:*** – Provides the BOM associated with the A^{2}B transceiver system.
- ***Appendix B:*** – Provides the power supply design recommendations.

Intended Audience

This manual is intended for OEM engineers who write A^{2}B system requirement specifications.

A^{2}B Terminology

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

To make the best use of the A^{2}B system, it is helpful to understand the following terms.

A-Side or A-Port

A^{2}B transceiver interface that faces toward the main node (toward the immediately upstream node).

AN

Negative terminal of the A-side.

AP

Positive terminal of the A-side.

B-Side or B-Port

A^{2}B transceiver interface that faces toward the last-in-line subordinate node (toward the immediately downstream next-in-line subordinate node).

BN

Negative terminal of the B-side.

BP

Positive terminal of the B-side.

Bus Link

The A^{2}B bus can consist of multiple daisy-chained subordinate nodes connected to a single main node. The physical connection between the main node and subordinate node 0, as well as all physical A^{2}B connections between subordinates, are called bus links. Unshielded twisted-wire pair, shielded twisted pair, or Cat5e are typically used for each bus link.

Daisy Chain

An interconnection of A^{2}B nodes (and peripherals) in series.

Data Channel

A data channel carries the synchronous I^{2}S/TDM data for a single sensor/actuator (for example, an ADC, a microphone, or a speaker). The I^{2}S/TDM interface uses equally-sized data channels, where the width of the data word is often smaller than the width of the I^{2}S/TDM data channel. The I^{2}S/TDM interface of the transceiver supports programmable data channel lengths of 16 or 32 bits.

Data Slot

A synchronous data word of a single sensor/actuator (for example, an ADC, a microphone, or a speaker), as mapped onto the A^{2}B bus.

Downstream

Communication flow from the main node toward the subordinate nodes, terminating at the last-in-line subordinate node.

EMC

Electromagnetic Compatibility. The ability of equipment to satisfactorily function in its EM environment without introducing intolerable electromagnetic disturbances to other equipment in that environment.

EMI

Electromagnetic Interference. The electromagnetic emissions caused by the device during its operation. This interference must be kept within the EMI standard limits.

Host

Processor that programs the main transceiver. The host is also the source for the synchronous clock on the A^{2}B bus. The clock signal (BCLK) is part of the I^{2}S/TDM interface between the host and main transceiver.

I ^{2} S/TDM

The inter IC sound (I^{2}S) bus carries pulse code modulated (PCM) information between audio chips on a PCB. The I^{2}S/TDM interface extends the I^{2}S stereo (2-channel) content to multiple channels using time-division multiplexing (TDM).

Local Power

Subordinate nodes that do not operate on A^{2}B bus power use local power, which is sourced from an external supply.

LVDS

Low voltage differential signaling.

Main Node

Originator of the clock (derived from the I^{2}S input), downstream data, network control, and power. The main node is comprised of the host processor and an A^{2}B main transceiver, which receives payloads from the host and sends payloads to the host.

PDM

Pulse Density Modulation (PDM) is used in sigma delta converters. PDM format represents an over-sampled 1-bit sigma delta ADC signal before decimation and is often used as the output format in digital microphones.

Preamble

Synchronization bits to signal the start of a control or response frame. The downstream control frame preamble is sent by the main node for every superframe. Subordinate transceivers synchronize to the downstream control preamble and generate a local, phase-aligned main node clock from it.

Shielded Twisted Pair

A twisted pair of copper wires with an outer covering or a shield that functions as a ground.

Subordinate Node

Addressable network connection point. Possible destination for downstream data slots and source of upstream data slots. Every A^{2}B subordinate node has an A^{2}B subordinate transceiver.

SigmaStudio/SigmaStudio+ ®

A graphical development tool used for programming, developing, and tuning software for ADI DSP audio processors. A^{2}B networks are configurable with the SigmaStudio/SigmaStudio+ graphical software tool.

Synchronization Control and Response Frames (SCF/SRF)

Control frame for nodes (control header) and response frame from nodes (response header). Headers include a preamble for synchronization and enable read and write access to all nodes.

Synchronous Data

Data streamed continuously (for example, audio signals) with a fixed time interval (typically, 48 kHz) between two successive transmissions to and from the same node.

Superframe

The overall frame structure for the A^{2}B bus. It starts with an SCF, includes optional data slots, and concludes with an SRF. Superframes repeat every 1024 bus clock cycles.

Unshielded Twisted Pair (UTP)

Cabling that consists of two unshielded copper wires (no meshes, aluminum foil, etc.) that are twisted around each other. The UTP cancels electromagnetic interference (EMI) from external sources.

Untwisted Cable

A straight-through cable is called an untwisted cable.

Upstream

Communication flow from the last-in-line subordinate node to the main node.

1 A2B Overview

The A2B ® system communicates multichannel I2S synchronous PCM data over a distance of up to 30m between nodes. It also extends the synchronous, time-division multiplexed (TDM) nature of I2S to a system that connects multiple nodes, where each node can consume data, provide data, or both.

The transceivers support these A2B functions with a direct interface to general-purpose digital signal processors (DSPs), field programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs), microphones, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and codecs through a multichannel I2S/TDM interface. They also provide a PDM interface for direct connection of up to four PDM digital microphones. Enabling the A2B bus-power feature supplies voltage and current to the subordinate nodes over the same, daisy-chained, twisted-pair cable as used for the communication link. The transceiver also fully supports I2C and SPI communication over the A2B link.

The A2B transceivers can be used to form the following nodes:

- Main node and local powered subordinate nodes (LPS) that are powered by an external supply.
- Bus-powered subordinate nodes (BPS) that are powered by the main node or local powered subordinate node. The current to power the BPS is sourced by the main node or preceding LPS node and sent via the A2B differential pair. The supply network of the main (or local powered subordinate node) must be designed accordingly. A typical BPS node is a microphone or line level analog converter module which consumes relatively low power.

A2B Bus Features

The A2B bus has the following features:

- Single-main, multiple-subordinate line topology – the multiplex network consists of twisted wire cables between daisy-chained nodes. The first node in the daisy chain is the main node; subsequent nodes are either local-powered or A2B bus-powered subordinate nodes. A2B is electrically a point-to-point network.
- Deterministic data transfer with low-latency subordinate-to-subordinate communication
- A2B bus-powered or local power subordinate nodes
    - Local power subordinate nodes can source A2B bus power to compatible downstream subordinates

- Configurable with SigmaStudio+ graphical development tool
- Supports I^2C, SPI, PDM, and I^2S/TDM transmission protocols
    - PDM inputs for up to 4 high dynamic range microphones per node
        - PDM programmable data rate
    - 8-bit to 32-bit multichannel I^2S/TDM interface
        - I^2S/TDM programmable data rate
        - Up to 32 channels of 24-bit data, mapped to upstream and downstream A^2B bus slots
- Supports both unshielded and shielded twisted cables

A^2B Bus Specifications

The following specifications apply to the A^2B bus:

- Network speed: 49.152 Mbps
- Maximum node-to-node cable length: 30 m
- Maximum network cable length: 300 m
- Maximum number of nodes: 17 (1 main node and 16 subordinate nodes)
- Maximum number in-line connections between nodes (applicable to all nodes): 2
- Maximum A^2B bus power current sourced by main or local power subordinate: 2.1 A
- Maximum A^2B cable DC line bias: 24 V
- A^2B has been proven to meet the most stringent automotive EMI/EMC standards

Transceiver Blocks

The transceiver consists of analog and digital blocks used for configuration, communication, and diagnostics. Reliable communication and detection of A^2B network errors occurs simultaneously without degrading EMI/EMC performance. The ***A^2B Transceiver Block Diagram*** shows the functional blocks of the A^2B transceiver.

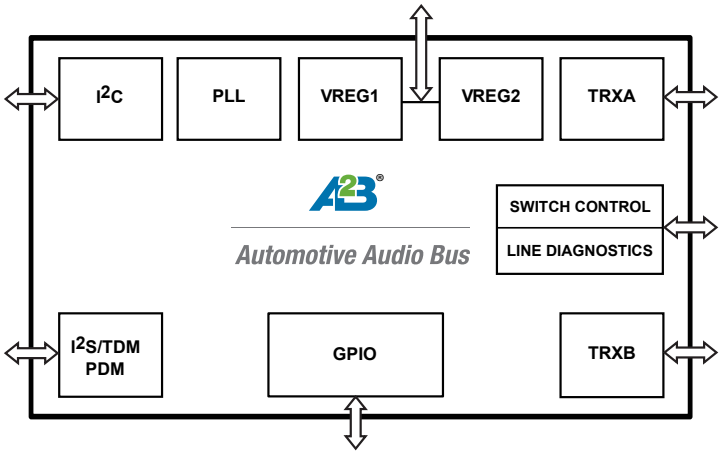

Figure 1-1: A2B Transceiver Block Diagram

The A2B transceiver consists of the following blocks:

LVDS Transceiver (A2B TRX A and A2B TRX B)

Used to transmit and receive all the A2B protocol data over the twisted pair communications link between nodes.

Diagnostics

Used to identify and report faults in the A2B system during and after node discovery. The A2B software stack can handle fault detection and events.

PLL

Used to generate the system clock. At the main node, the PLL locks on the SYNC input signal. At subordinate nodes, the PLL locks on the preamble of the SCF coming from the immediately upstream node.

In a subordinate node, the PLL is used for data recovery of the ~50 Mb/s Manchester-encoded serial data on the A2B bus and for transmitting data to the next-in-line A2B node. The PLL lock takes a maximum of 360 frames to lock, based on a digital counter that is not affected by temperature or aging.

Typically, the maximum PLL lock time is 7.5 ms. The PLL lock may fail if the SYNC signal is missing or due to the presence of excessive jitter on the SYNC input signal. In a subordinate node, the PLL may fail to lock if the communication channel corrupts the preamble of the SCF coming from the upstream nodes. If the node does not lock within the specified 7.5 ms, then it reattempts to lock the PLL until it succeeds. The host must set up a timeout to ensure that the PLL lock is not reattempted indefinitely.

Voltage Regulators

There are two on-chip linear voltage regulators in the transceiver:

- VREG1 provides 1.9V to power the digital and PLL domains
- VREG2 provides 3.3V to power the LVDS transceiver

Each voltage regulator can typically supply up to 100 mA of current to external devices. They can also be used to power the system IOVDD, if desired.

SPI Interface

Used by a locally connected host to access the transceiver register space. The SPI interface is also used to transmit control information over the A^{2}B bus.

The maximum SCK clock frequency into the A^{2}B main or subordinate devices must not exceed 12.288 MHz.

I^{2}C Interface

Used by a locally-connected host to access the transceiver register space. The I^{2}C interface is also used to transmit control information over the A^{2}B bus.

The maximum SCL clock frequency into the A^{2}B main or subordinate devices must not exceed 400 kHz.

I^{2}S/TDM Interface

The I^{2}S/TDM serial port operates in full-duplex mode. The transmitter and receiver operate simultaneously using the same critical timing bit clock (BCLK) and synchronization (SYNC) signals.

The SYNC signal is the fundamental clock for the main A^{2}B transceiver. Its frequency must be either 44.1 kHz or 48 kHz. All subordinate nodes support multiples and divisors of the frame rate.

PDM Interface

The PDM block converts a PDM input stream into PCM data to be sent over the A^{2}B bus and/or out to the local node through the I^{2}S/TDM port.

2 A2B Transceiver Specifications

This section describes the operating conditions of the A2B transceiver.

Operating Conditions

The ***Operating Conditions*** table shows the parameters that specify the operating conditions of the A2B transceiver. For more operating conditions, see the product-specific data sheet.

Table 2-1: Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
Power Supplies					
Digital Core Logic Supply Voltage (V_{DVDD})		1.7	1.9	1.98	V
Phase-Locked Loop (PLL) Supply Voltage (V_{PLLVDD})		1.7	1.9	1.98	V
Transceiver Supply Voltage (V_{TRXVDD})	Applies to the TRXVDD pin	3.0	3.3	3.63	V
Digital Input/Output (I/O) Supply Voltage (V_{IOVDD})	3.3 V I/O	3.0	3.3	3.63	V
	1.8 V I/O	1.7	1.9	1.98	V
Regulator Input Supply Voltage (V_{VIN})	Specification must be met at the VIN pin of each A2B bus transceiver	3.7	5.0	9.0	V
Regulator Input Supply Voltage (V_{VIN}) LVI mode	Low Voltage Input (LVI) node only (3.3V regulator bypass)	3.0	3.3	3.63	V

Power-Up Sequencing

The A2B transceiver has the following power-up sequencing restriction:

- V_{DVDD} and V_{IOVDD}, when externally supplied, must reach at least 90% of the specification before V_{VIN} begins ramping.
- V_{IOVDD} must be supplied within the voltage specified in the data sheet before driving the input pins.

Timing Specifications

This section provides clock timing specifications for the A^{2}B transceiver.

Clock Jitter

The SYNC pin is an input to the main node, which is typically driven by the host in the system. Upon receiving the SYNC signal, the main node locks its PLL. The clock and synchronization information are embedded in the data and sent over the LVDS interface. The subordinate node recovers the clock and synchronization information from the received LVDS signals to drive the attached peripherals (for example, a codec). Each node adds self-jitter to the incoming signal, which results in jitter growth from the main to the last-in-line subordinate.

Asynchronous sample rate converters (ASRC) or an external clock regeneration circuit can be added to further eliminate clock jitter. Refer to engineering note EE-452 *AD2437 A2B Transceiver Audio Performance Testing and Results.*

- The RMS cycle-to-cycle jitter of the SYNC signal provided by the host (at the main node) shall not exceed 1ns.
- The RMS cycle-to-cycle jitter of the SYNC signal from the A^{2}B subordinate transceiver shall not exceed 2.2ns.

3 Functional Model

This section describes the physical and data link layer specifications that establish data communication over the A²B bus system.

Physical Layer Requirements

The A²B bus typically consists of multiple daisy-chained subordinate nodes connected to a single main node. A twisted-pair wire is typically used for each bus link for the upstream and downstream data transfer. Peripheral devices can be connected to the subordinate nodes through the I²S/TDM interface and are accessible over the A²B bus. The *Simplified A²B System with Four Nodes* figure shows a typical A²B system.

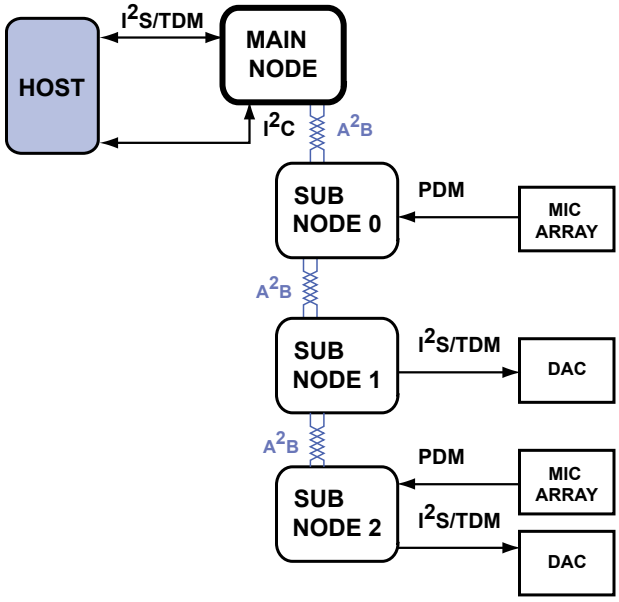

Figure 3-1: Simplified A²B System with Four Nodes

An A²B system has the following characteristics:

Types of Subordinate Nodes

Subordinate nodes can be bus-powered or local-powered. An A^{2}B system can have a combination of both local-powered and A^{2}B bus-powered subordinate nodes.

A^{2}B Bus-Powered Node

A^{2}B bus-powered subordinate transceivers derive power from the immediately upstream node. The following requirements must be met for proper functionality and optimal EMC performance for A^{2}B bus-powered subordinates.

- Whether powered by the main or the immediately upstream local-powered subordinate, the total current drawn by all bus-powered nodes must not exceed 2.1 A.
- The voltage at the VIN pin must be at least 3.7 V when not in LVI mode.

Local-Powered Subordinate (LPS) Node

A local supply powers the A^{2}B transceiver and other peripherals; it uses no current from the bus.

Maximum Number of Nodes

The AD2437 A^{2}B bus system supports up to a maximum of 17 nodes (1 main node and 16 subordinate nodes).

Maximum Load Current

The maximum bus current that can be sourced by the main or local-powered subordinate is 2.1A for power over a single twisted pair, XLR cable, or CAT5e cable.

Maximum Cable Length

The maximum cable length between nodes is 30m, and the total cable length used in the complete A^{2}B system must not exceed 300m. It is essential to adhere to the Cable Requirements, Connector Requirements, and BOM to achieve the required cable length and desired EMI/EMC performance.

Cable and Connector Requirements

The A^{2}B system uses twisted pair CAT and XLR cables. The system uses connectors that meet EMI/EMC standards. The following sections detail the cable and connector requirements and placement recommendations.

Cable Requirements

The A^{2}B system must use cables that meet the following requirements:

Characteristic Impedance

The characteristic impedance must be 100 Ω with 15% tolerance.

Cable Twists

Cables used with the A^{2}B transceiver have a typical lay length of 20 mm and a maximum lay length of 30 mm.

Bending Radius

The minimum bending radius is typically 5x the diameter of the cable and depends on the physical properties of the cable. The OEM must ensure that the cables do not bend below the minimum bending radius specified by the cable vendor.

Conductor Stranding

Cable vendors offer different numbers of strands, diameters, thicknesses, and tolerances to match electrical properties and mechanical requirements. Connectors must have suitable support for the cable cores specified.

Cable Handling

Avoid unnecessary bends and conductor compression. Conductor diameter variations and effective dielectric constant changes have implications on cable characteristics.

Cable Materials

Material properties have a direct influence on the electrical performance of a cable, as well as its aging and thermal effects.

Conductor

For the bare copper strand, the metal composition is specified by the cable vendor.

Sheath

Because cable parameters are sensitive to moisture, a sheath is required in high-moisture environments. A sheath also protects the cable from mechanical stress and untwisting.

CAT Cable Requirements

For 8P8C/RJ45 connectors, CAT5e (as defined ANSI/TIA-568) or better cable must be used. Shielded or unshielded CAT cable may be used. The length of a CAT cable between nodes is limited to 30m.

XLR Cable Requirements

The A2B system must use cables that meet the following requirements for XLR systems.

Cable Types

XLR cables designed for use with analog signals such as microphones and line level applications do not conform to any industry standard and often do not have the necessary specifications listed. There are many different types of analog XLR cables on the market with wide ranges of performance. Many different cables have been successfully tested up to 30m in A2B systems, however because of the uncertainty of cable specifications, it is recommended to use DMX or AES/EBU cables at longer distances.

Cable AC and DC Characteristics

The cables used in the XLR system must satisfy all of the AC and DC characteristics in the ***Cable DC Characteristics*** and ***Cable AC Characteristics*** tables.

Table 3-1: Cable DC Characteristics

Parameter	Min.	Max.	Unit
Conductor Resistance		150	mΩ/m
DC Current per Conductor	1.25		A
Operating Voltage	30		V

Table 3-2: Cable AC Characteristics

Parameter	Condition	Min.	Max.	Unit
Characteristic Impedance		85	115	Ω
Insertion Loss	1 MHz		0.09	dB/m
	10 MHz		0.20	dB/m
	33 MHz		0.32	dB/m
	66 MHz		0.58	dB/m
Return Loss	1 MHz	12		dB
	20 MHz	15		dB
	66 MHz	15		dB
Mode Conversion Loss	1 MHz	36		dB
	50 MHz	26		dB
	200 MHz	26		dB

Connector Mechanicals

The A^{2}B transceiver does not mandate a specific connector. The choice of a connector can influence the performance margin in EMC tests. Connectors may impose discontinuities to the characteristic impedance and affect the symmetry of the A^{2}B system. Use a connector that matches the characteristic impedance of the cable.

Connector Requirements

To be compliant with the industry EMI/EMC standards, the connectors used in the A^{2}B system must satisfy all of the AC and DC characteristics described in the ***Connector Characteristics*** table.

XLR

Pinout must follow ADI XLR3 reference design.

RJ45 (8P8C)

Pinout must follow ADI reference design.

Table 3-3: Connector Characteristics

Parameter	Condition	Min	Typ	Max	Unit
DC Characteristics					
Conductor Resistance			20	80	mΩ
DC Current per Conductor	XLR	3			A
DC Current per Conductor	RJ45	1			A
Operating Voltage		30			V DC
AC Characteristics					
Characteristic Impedance		90	100	110	Ω
Insertion Loss	1 MHz			0.025	dB
	10 MHz			0.038	dB
	33 MHz			0.050	dB
	66 MHz			0.075	dB
Return Loss	1 MHz	38			dB
	20 MHz	38			dB
	66 MHz	30.5			dB
Mode Conversion Loss	1 MHz	46			dB
	50 MHz	46			dB
	200 MHz	34			dB

Connector Pin Assignment

A^{2}B contact pairs provide the best EMC performance when used with dedicated connectors. In designs where dedicated connectors for A^{2}B signal pairs are not possible, A^{2}B differential pairs can be included in a custom multi-pin, multi-function connector. However, the A^{2}B differential signal pairs must retain impedance balance between signal pairs and care must be taken when pin spacing is smaller than 0.15 inches. This configuration reduces crosstalk and improves the symmetry of the differential pairs. System EMC performance improves with better symmetry of differential pairs.

Use the following guidelines for the A^{2}B bus on a multi-pin, multi-signal on-board, and inline connector:

- Place A^{2}B differential pin pairs physically closer to each other than to other high-frequency, dynamic signals, like Ethernet, CAN, or a second A^{2}B pin pair. This layout reduces crosstalk and improves the symmetry of the pin pairs. Allocate the A^{2}B bus on the sides so that they are away from other noisy signals.
- Allocate adjacent pins in a multi-pin, multi-function connector as ground, or, make it a no connect (NC) pin by following symmetry (same pin assignment on both sides of the A^{2}B differential pair). When possible, avoid metal tabs for NC pins.
    - Place the A^{2}B differential pairs on the same row to avoid pin length mismatches that can lead to an impedance mismatch.
    - Place only static signals (like power or GND) or low frequency control signals (like an enable signal).
    - Avoid placing any high frequency signals nearby (like Ethernet bus, CAN bus, etc).
    - Follow symmetry in signal placement. Any asymmetries can introduce skew between the differential signals that generate common mode noise, and, consequently, degrade EMC performance.

The ***Symmetrical A^{2}B Pin Assignment on Multi-Pin Connector*** figure shows a recommended implementation on a single-row connector with signal spacing.

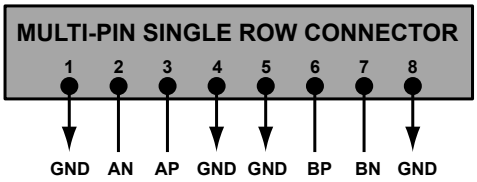

Figure 3-2: Symmetrical A^{2}B Pin Assignment on Multi-Pin Connector

Pigtail Requirements

In space-constrained applications such as a microphone, pigtails can be used instead of dedicated connectors to save module space. Refer to the ***Pigtail Connections*** figure. Take care when implementing a pigtail to reduce the amount of untwist to a minimum at the module (<10mm). The entire pigtail harness shall be sheathed or tightly taped to reduce the probability of the cable becoming untwisted. When sheathed, limit the distance between the shrink tubing and the connector to less than or equal to 10 mm.

Use the following practices for pigtail connections:

- Minimize W (pin width)
- Minimize U and U1 (untwist < 10 mm) and reduce the untwist as much as possible
  - Tape or use shrink tube if the untwist cannot be reduced
- Minimize P so that the differential pair is close together
- Maximize S (separation between the pairs S > 2P)
- Maximize T, ensuring T is sufficient to solder the cable of require gauge
- Cables can be attached to the module through a solder joint

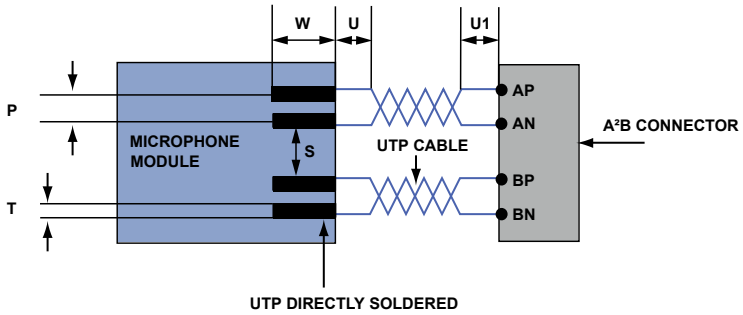

Figure 3-3: Pigtail Connections

Designer Reference

The following sections provide front end circuit requirements and PCB layout recommendations.

A²B Front End Circuit Requirements

This section describes the recommended front end circuitry and the critical components to use with the A²B transceiver. The ADI recommendation is to follow the mandatory front end circuitry guidance, including observing the maximum distance between components to meet industry EMI/EMC standards, in order achieve better signal integrity.

NOTE: Contact your Analog Devices representative for the latest recommended front-end circuit schematics and Bill of Materials (BOM) to fit your application.

- A²B AD2437 Circuit
- A²B XLR B-Port Circuit
- A²B Local-powered Subordinate XLR A-Port Circuit
- A²B Bus-powered Subordinate XLR A-Port Circuit
- A²B RJ45 B-Port Circuit
- A²B Local-powered Subordinate RJ45 A-Port Circuit

- A2B Bus-powered Subordinate RJ45 A-Port Circuit

A2B AD2437 Circuit

The ***A2B AD2437 Circuit*** figure shows the recommended front-end circuitry for the transceiver power supply pins and data ports. The following notes apply to the figure:

- See the BOM for recommended component values.
- Pull-up resistors on SDA and SCL connect to the IOVDD power supply. For more information on resistor values, see the pin descriptions in the product-specific data sheet.
- Use an RC low-pass filter for clock and data pins ensuring identical filters on corresponding signals. Place filter close to source pins.
- Pull-up and pull-down resistors for I2C address pins connect to IOVDD power supply or ground. Please see the transceiver reference manual for configuration and address options.

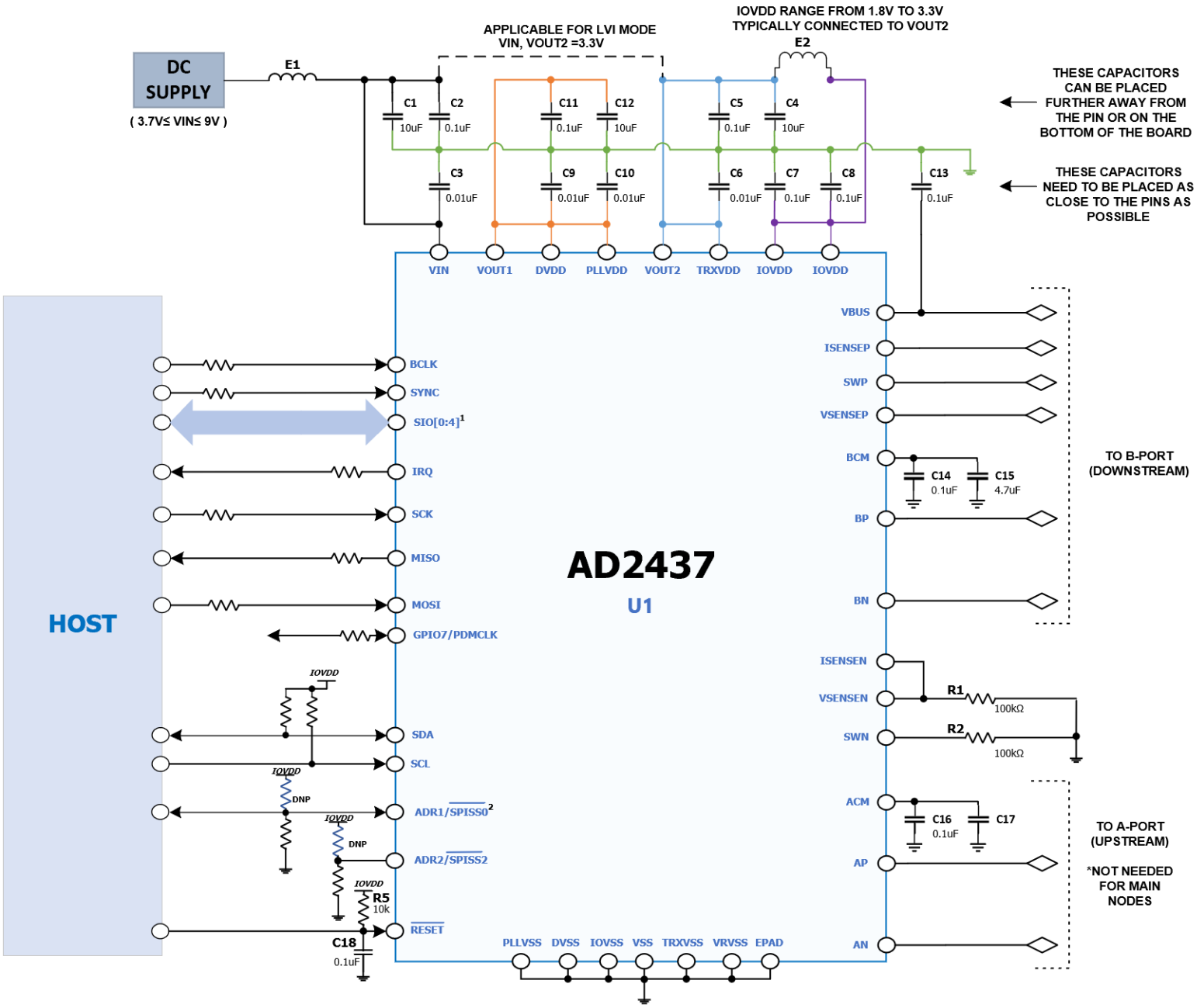

Figure 3-4: A2B AD2437 Main Node Transceiver Circuit

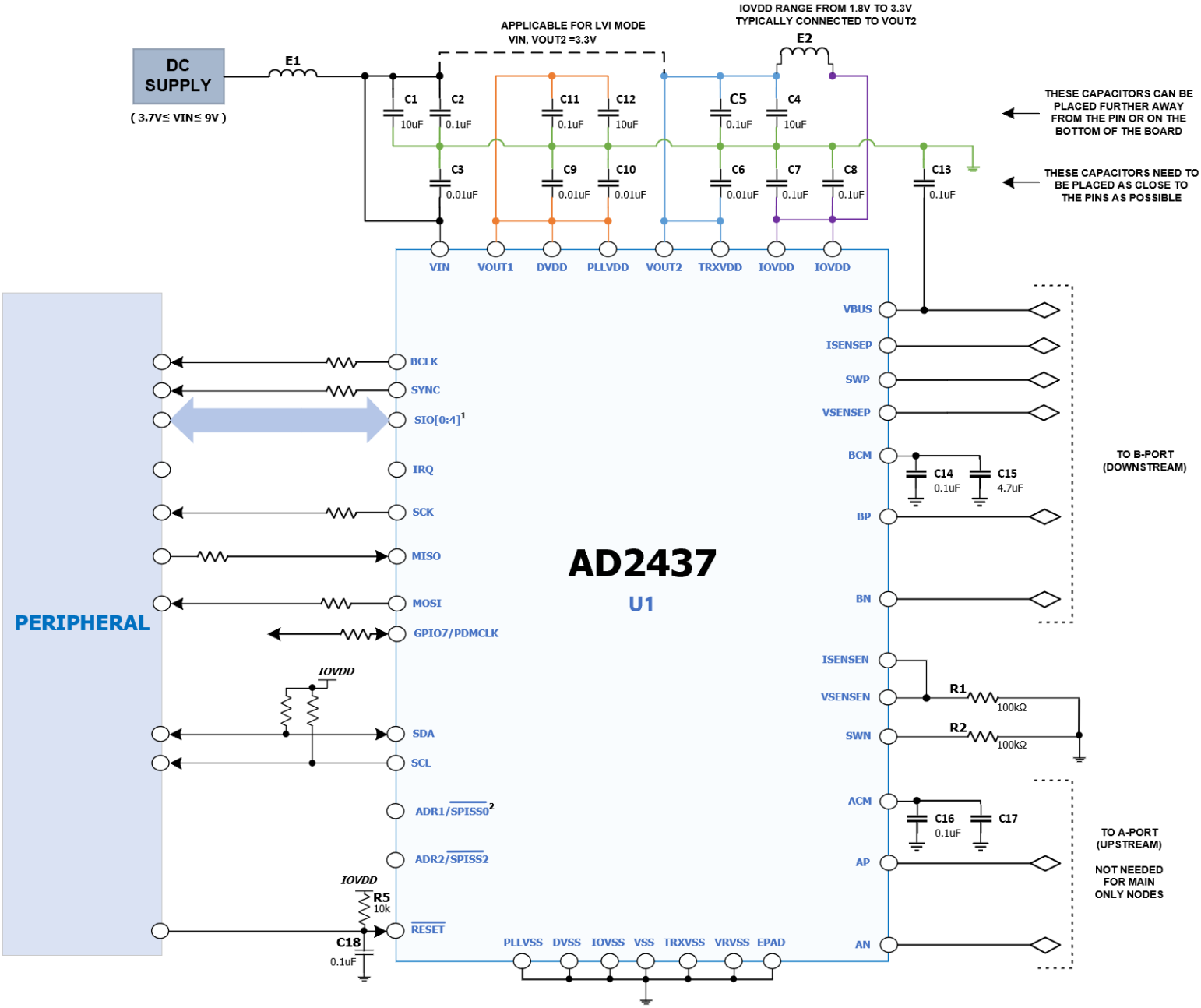

Figure 3-5: A2B AD2437 Sub Node Transceiver Circuit

NOTE:

1. Refer to the ***AD2437 Transceiver Technical Reference Manual*** to configure SIO functionality. The SIO2 pin can be configured as the SPI target select ($\overline{\text{ASPISS}}$/SISSEL1).
2. The ADR1/$\overline{\text{SPISS0}}$ pin can select the AD243x transceiver as the SPI target.
3. The reservoir bulk capacitor should discharge to < 3.3V within 250 ms.
4. The maximum load capacitance supported on an adjacent downstream subordinate node is ≤ 1000 µF.

A2B XLR B-Port Circuit

The *A2B XLR B-Port Circuit* figure shows the recommended front-end circuitry for the transceiver B-port configured for use with XLR connectors. The following notes apply to the figure:

- See the BOM for recommended component values.
- U2 (MAX17612A) is the recommended device to limit and monitor current during two-step discovery. The FLAG_N pin connects to the transceiver GPIO7 and is used to indicate an overcurrent condition during two-step discovery.
- Q1 is an NMOS switch used to enable the 24V bus bias.
- R6 is a current sense resistor. V_{BUS} and I_{SENSEP} connections back to the transceiver need to be kelvin connected (matched traces) for accurate current monitoring.
- Zener diode D2 protects against electrostatic discharge (ESD) and over voltage conditions.
- LED1 and LED2 are optional for use with Neutrik Light Ring XLR connectors or other indicators. Adjust R8 for brightness.

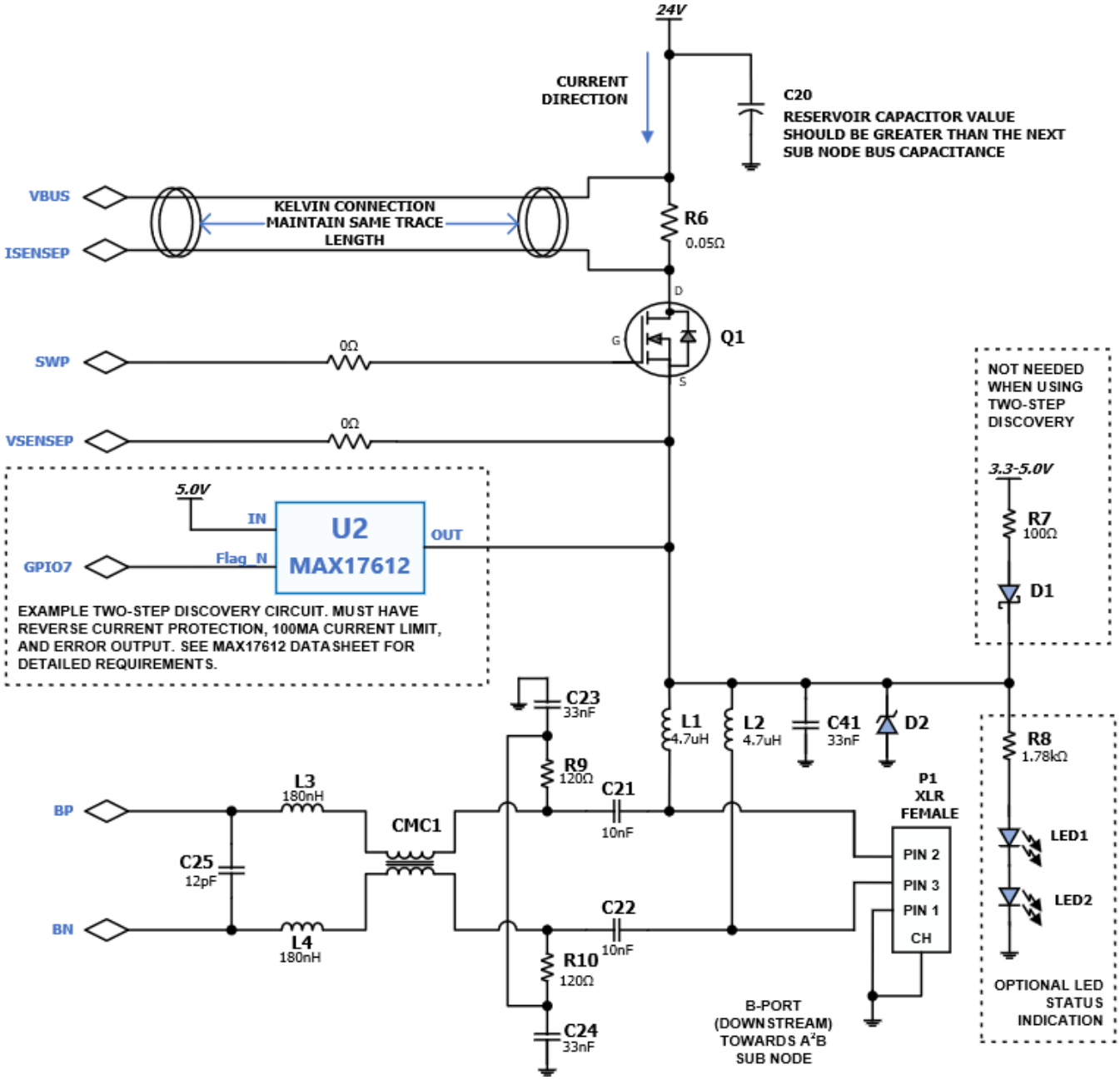

Figure 3-6: A2B XLR B-Port Circuit

A2B Local-powered Subordinate XLR A-Port Circuit

The *A2B Local-Powered Subordinate XLR A-Port Circuit* figure shows the recommended front-end circuitry for the local-powered subordinate node. The following notes apply to the figure:

- See the BOM for recommended component values.
- Transformer T1 is used to galvanically isolate the node from the upstream node. The bias current is only used for diagnostics and the LED indicators, LED3 and LED4.

- Diode D3 is required to protect against over voltage conditions.
- Isolated ground requires connecting pin 1 and shield of P2, LED4, D3, and R19.

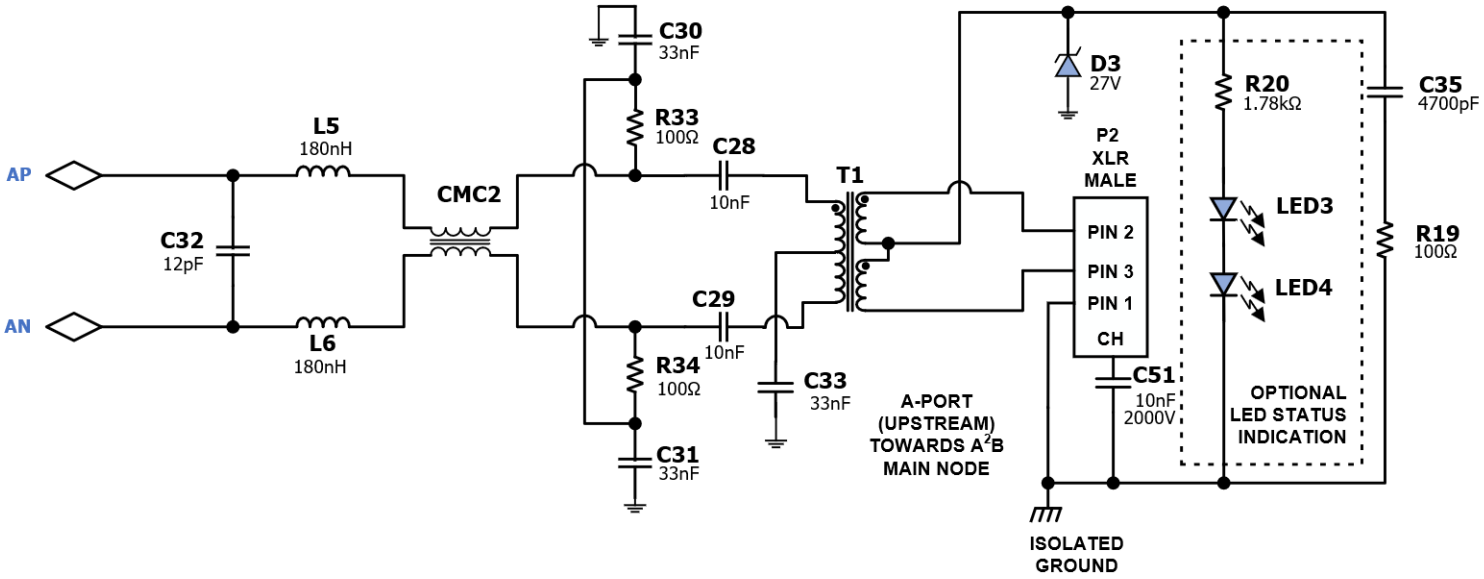

Figure 3-7: A2B Local-powered Subordinate XLR A-Port Circuit

A2B Bus-powered Subordinate XLR A-Port Circuit

The *A2B Bus-Powered Subordinate XLR A-Port Circuit* figure shows the recommended front-end circuitry for the A2B bus-powered subordinate node. The following notes apply to the figure:

- See the BOM for recommended component values.
- U3 is part of an example 5V regulator circuit that is needed to provide power to VIN of the transceiver. This regulator can be used for other devices as long as they are disabled during the first step of the two step discovery process.
- R21 and R22 are used to provide an enable voltage for peripherals when bus bias is above 18V. Adjust values depending on the thresholds of peripherals.

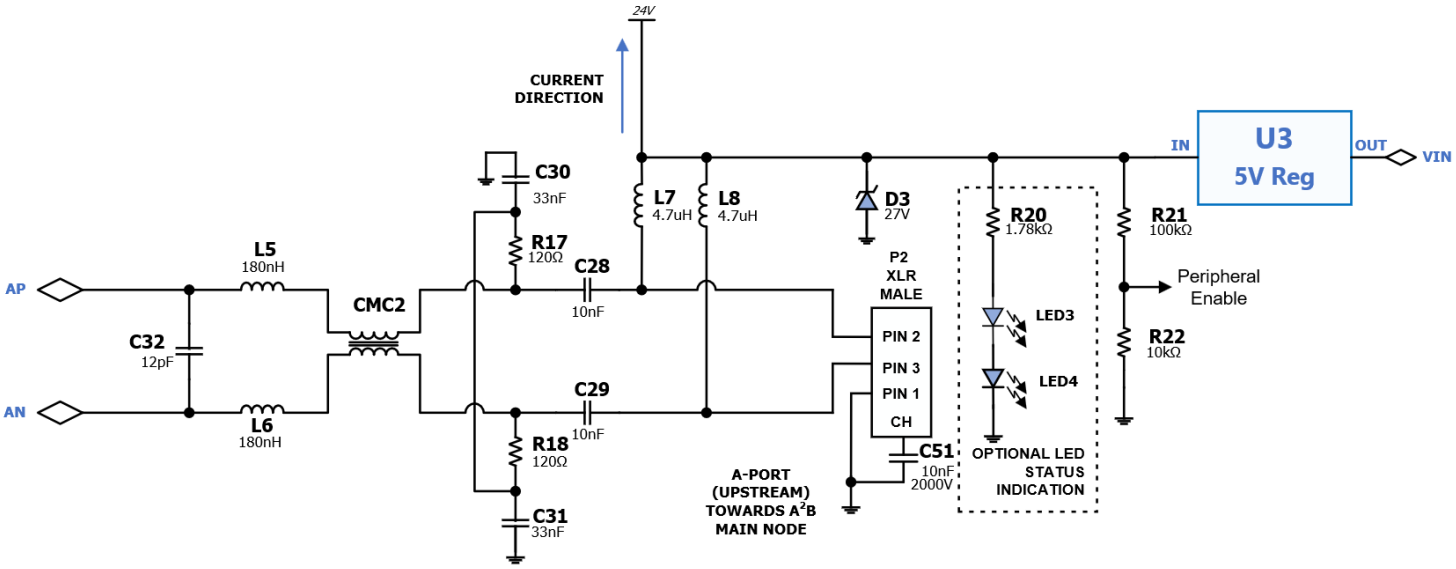

Figure 3-8: A2B Bus-powered Subordinate XLR A-Port Circuit

A2B RJ45 B-Port Circuit

The *A2B RJ45 B-Port Circuit* figure shows the recommended front-end circuitry for the A2B bus-power subordinate. The following notes apply to the figure:

- See the BOM for recommended component values.
- L9 and L10 are used to bias the central twisted pair with a 5V bias. This voltage source must be current limited to 50 mA and provide a *power-good* logic line to the transceiver GPIO7. Shown is an example circuit using the ADP2360. This regulator should not power any other devices.
- ADI recommends using RJ45 connectors with built in LEDs. Use one to indicate the 5V bias and the other to indicate 24V enable.
- Only the central pair of the RJ45 is used for data. The other three pairs are used for 24V and ground.

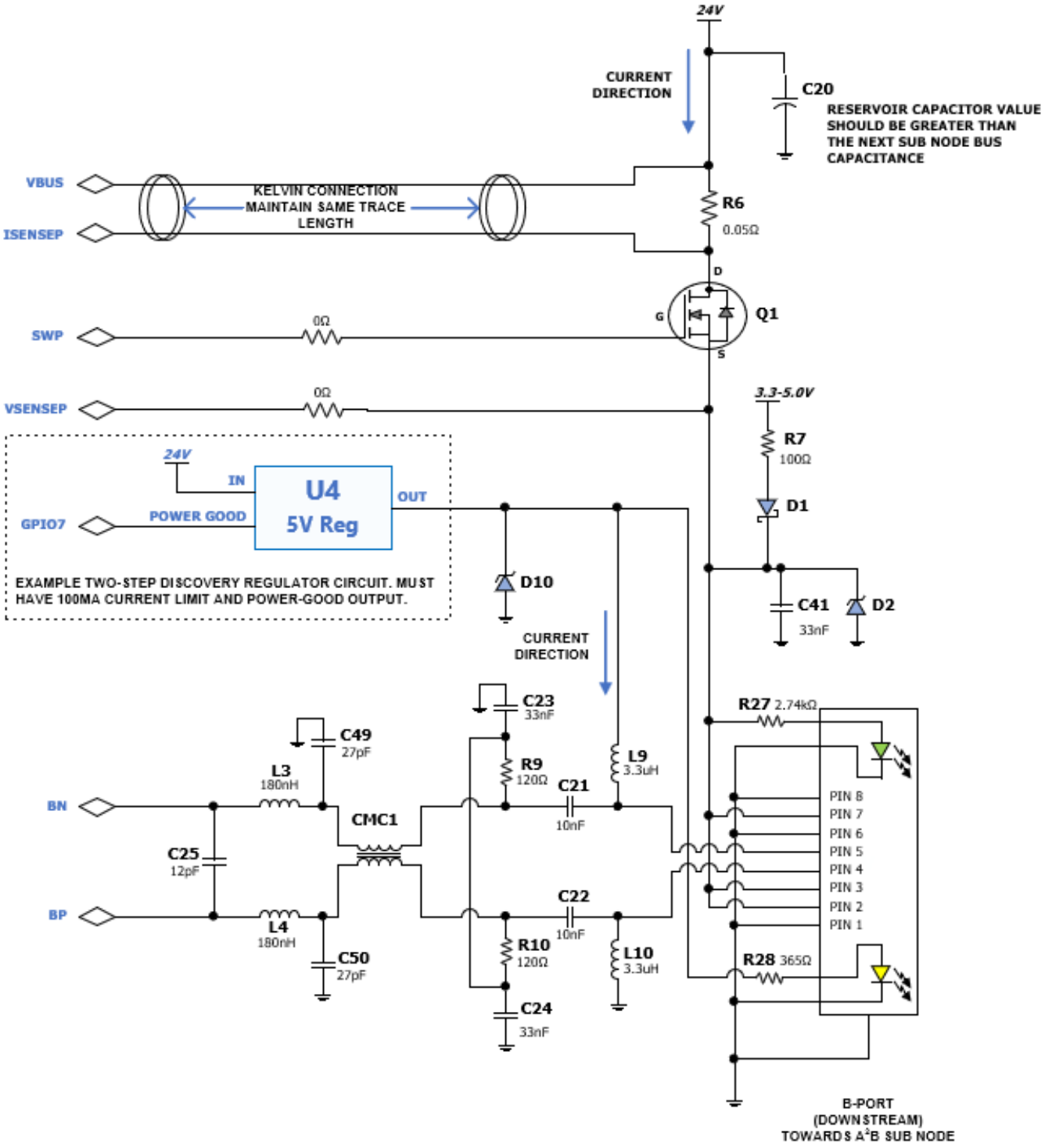

Figure 3-9: A2B RJ45 B-Port Circuit

A2B Local-powered Subordinate RJ45 A-Port Circuit

The *A2B Local-powered Subordinate RJ45 A-Port Circuit* figure shows the recommended front-end circuitry for a A2B local-power subordinate node. The following notes apply to the figure:

- See the BOM for recommended component values.
- Transformer T1 is used to galvanically isolate the local-powered sub node from the upstream network.
- ADI recommends using RJ45 connectors with built in LEDs. Using one to indicate the 5V bias, and the other to indicate 24V enable.
- 5V bias only used for LED indication and an optional optocoupler wakeup circuit.
- 24V bias used for LED indication; but is also necessary for line diagnostics.

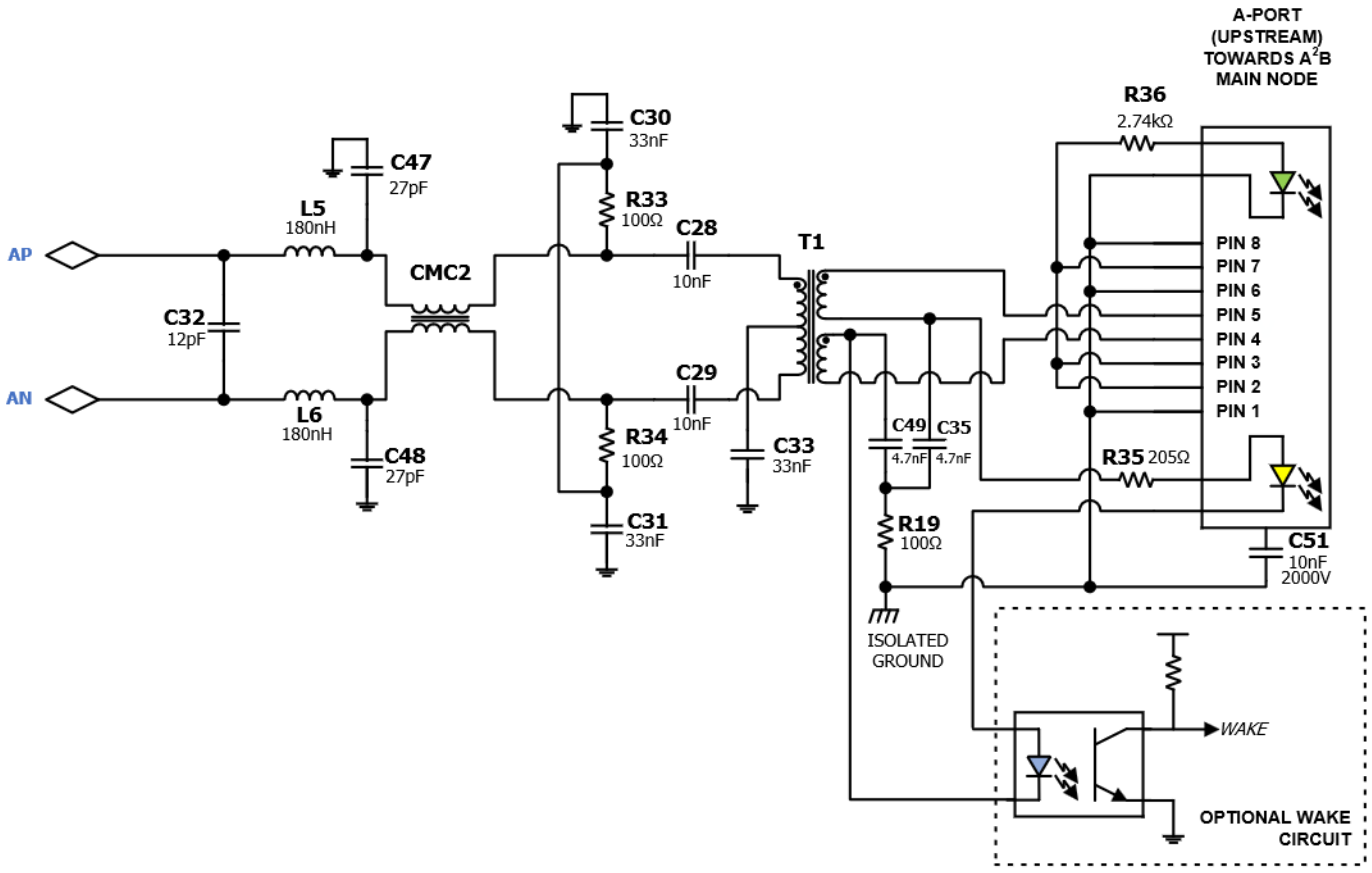

Figure 3-10: A2B Local-powered Subordinate RJ45 A-Port Circuit

A2B Bus-powered Subordinate RJ45 A-Port Circuit

The *A2B Bus-powered RJ45 A-Port Circuit* figure shows the recommended front-end circuitry for the A2B bus-power subordinate node. The following notes apply to the figure:

- See the BOM for recommended component values.

- 5V bias must connect to VIN to power transceiver and internal regulators used for *plug and pray* Electrical Erasable Read-Only Memory (EEPROM) and IOVDD.
- C51 is used to AC couple the shield of the cable to the board ground.
- ADI recommends using RJ45 connectors with built in LEDs. Use one to indicate the 5V bias, and the other to indicate the 24V enable.
- Only the central pair of the RJ45 is used for data. The other three pairs are used for 24V and ground.

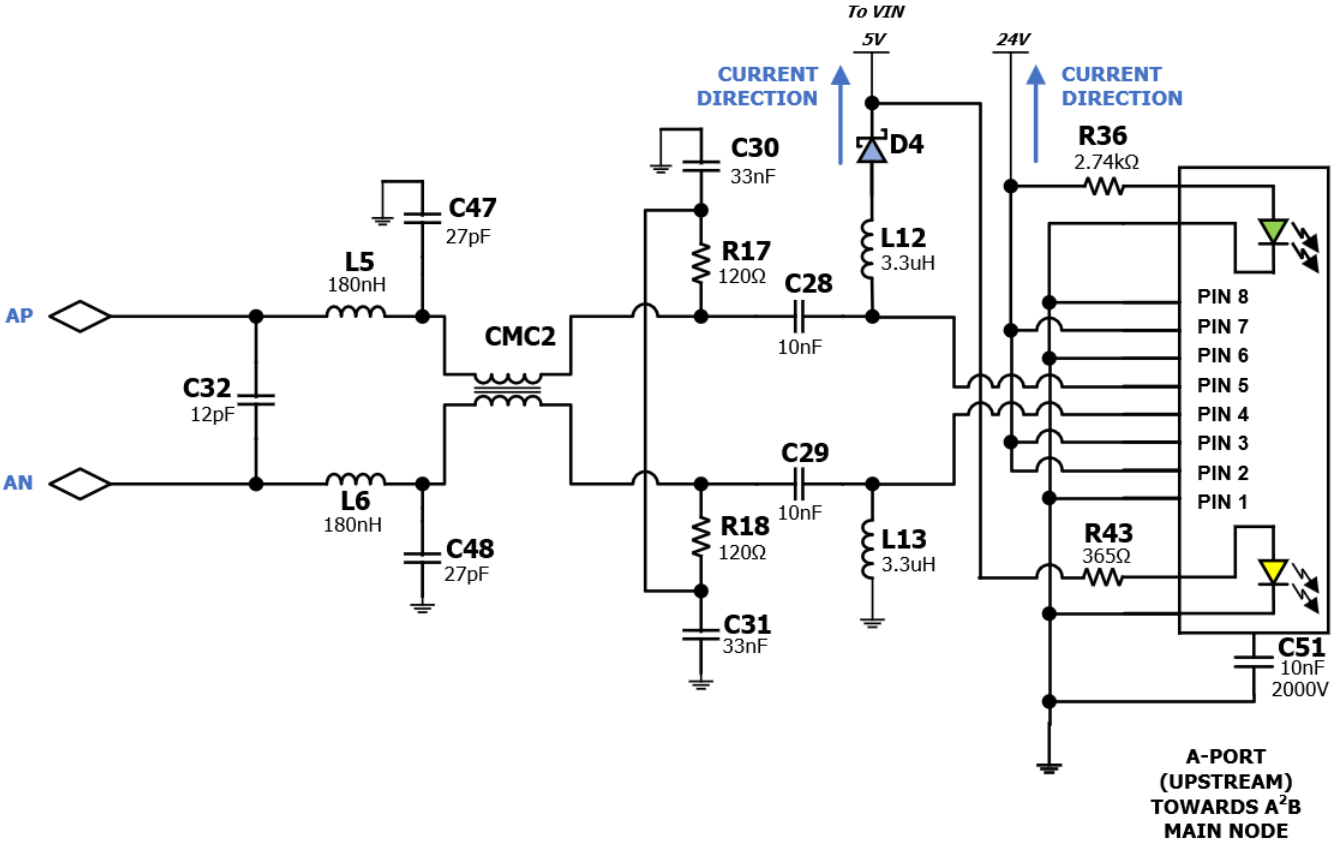

Figure 3-11: A^{2}B Bus-powered RJ45 A-Port Circuit

Critical Components

This section details the critical components in the A^{2}B front end circuitry.

It is recommended to use these components for best reliability and EMC performance. Similar replacements are available but performance is not guaranteed. Please refer to component data sheets and match specifications listed as closely as possible.

WARNING: Failure to use the specified components can result in reduced system EMC performance.

Common Mode Choke (CMC)

Use a symmetric ACT1210L-101-2P-TL00 common mode choke (100uH) from TDK or DLW32MH101XK2L from Murata Electronics or AMCW3225L-2-101T from Sunlord Electronics or VFC3225-101 from Cyntec.

In order to use a different device than listed, verify that it is suitable for 100BASE-T1 and closely matches the inductance and impedance curves of the preferred devices.

Inductors

Use balanced MLZ2012M3R3ATD69 8% tolerance inductors from TDK or LQH32NH3R3J23 5% tolerance inductors from Murata Electronics for L9, L10, L12, and L13.

For the higher current inductors L1, L2, L7, and L8, the preferred device is 7440530047 from Wurth Electronik. Devices with similar specifications, the same or higher current ratings, and, the same or lower resistance are also suitable.

AC-Coupling Capacitors

Use 10nF-15nF C0G/NP0 type and 5% tolerance capacitors for better symmetry, DC bias characteristics, and consistent EMI/EMC performance across temperature.

NMOS Switch

Proper selection of this device is critical to proper operation. The preferred choice is the DMTH8012LPSQ-13 from Diodes, Inc. However, many other devices are suitable. The safe operating area (SOA) and specifications of the device must meet the following criteria:

Criteria	Requirement
Vth	1.2V – 2.0V
Id max	20A or more
Id Continuous	10A or more
Vgs	-20V, +20V
VDS	40V or more
High power SOA	20V/ 3A / 10ms

TVS Diode

Use TVS diode TPSMF4L30A or equivalent to prevent damage during ESD tests.

Layout Recommendations

This section provides recommended layout practices for component placement and signal routing in an A^{2}B system. The recommendations are intended for systems to meet industry EMC requirements and best performance. See the BOM for component recommendations.

PCB Layers

The circuit board must be at least four layers. It must include at least a power layer, a ground layer, and two signal layers. Spacing and width of the differential trace depend on the PCB stack-up and should be designed to have 100 Ω differential impedance. The *Four-Layer Stack Up* figure shows the recommended circuit board stack-up for a four-layer board.

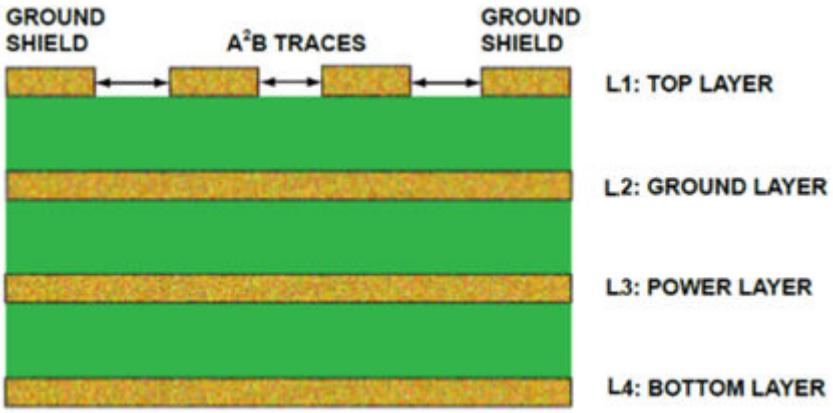

Figure 3-12: Four-Layer Stack Up

Component Placement

Place components based on the following recommendations.

Front End Component Placement Near the Transceiver

The components include the equalization capacitor (C25 and C32), the low-pass filter (L3, L4, L5, L6, C47, C48, C49 and C50). Please note C47-C50 are not needed in XLR configuration. This placement improves EMC performance and signal integrity. It is important to place these components symmetrically on the differential pair. The *Component Placement - Transceiver* figure shows the components that are recommended to be placed near the transceiver.

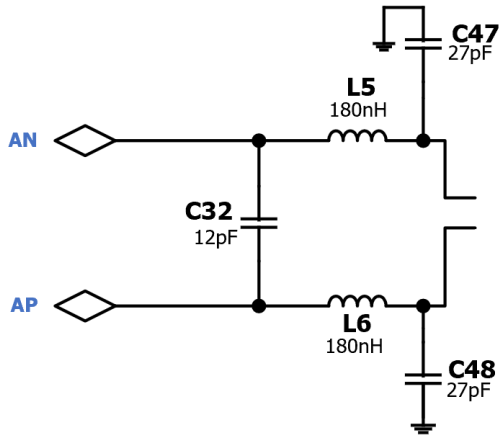

Figure 3-13: Component Placement - Transceiver

Front End Component Placement Near the A²B Connector

The components include the common mode choke (CMC1 and CMC2), split termination resistors (R9, R10, R17, R18, R33, and R34), split termination capacitors (C23, C24, C30, and C31), AC coupling capacitors (C21, C22, C28, and C29), DC bias inductors (L1, L2, L7, L8, L9, L10, L12, and L13), transformers (T1 and T2), and ESD suppression diodes (D2 and D10). The *Component Placement Schematic - A²B Connector* figure shows the components that are recommended to be placed near the A²B connector.

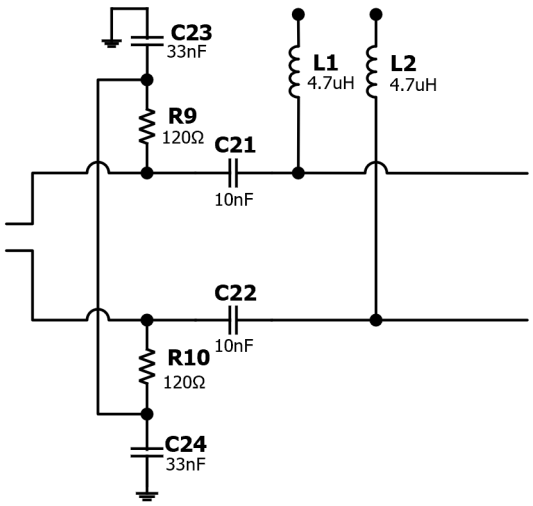

Figure 3-14: Component Placement - A²B Connector

Signal Pair Component Placement

Place the split termination resistors (R9, R10, R17, R18, R33, and R34) perpendicular to the CMC (CMC1 and CMC2). To maintain differential trace routing, it is important that the signals route through the pads of the termination resistors and are not branched to the resistors. Place the A^{2}B components symmetrically along the AP/AN and BP/BN signal pair traces.

The ***Signal Pair Component Placement*** figure shows the recommended placement of the resistors, capacitors, and inductors in the data path of the bus interface network.

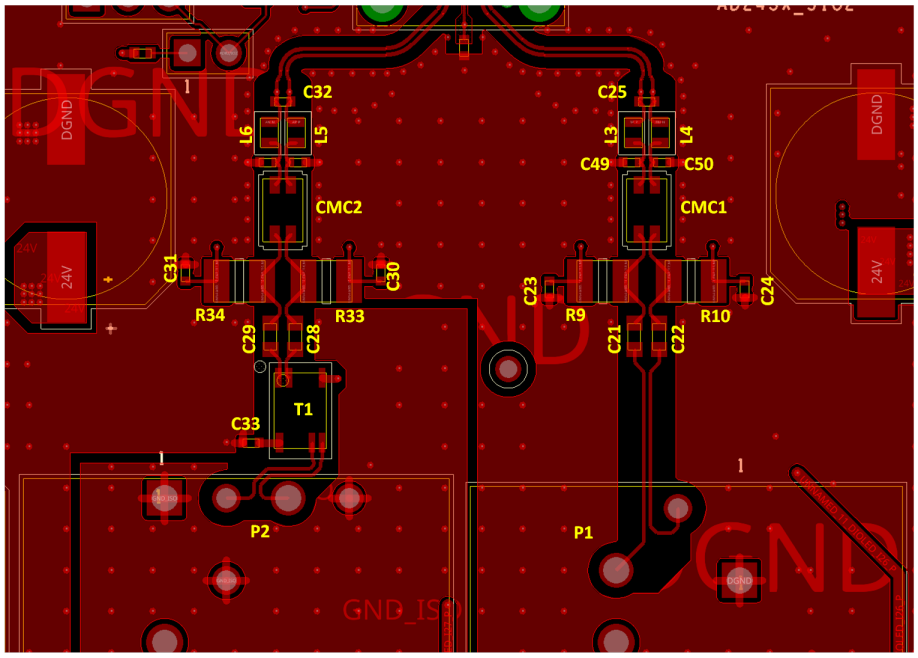

Figure 3-15: Signal Pair Component Placement

DC Bias Component Placement

It is recommended to separate the DC bias components on the opposite side of the board than the data path components. If it is preferred to keep all components on the same side, it is important to keep the bias inductors (L1, L2, L7, L8, L9, L10, L12, L13) perpendicular to each other. If the inductors are connected on the bias side, as in the XLR configuration, they can be placed in parallel if on the opposite side of the board.

Keep traces between R6 and VBUS, and R6 and ISENSEP matched length or Kelvin connected. These are sense traces for the current monitor and any major variation between these paths can cause error in that measurement. the main current path is from the 24V source through R6 and Q1 to either the bias inductors or the separate connector pins. The VBUS pin on the transceiver does not sink current so a large trace is not necessary.

The *DC Bias Component Placement* figure shows an example layout of these components for the XLR configuration.

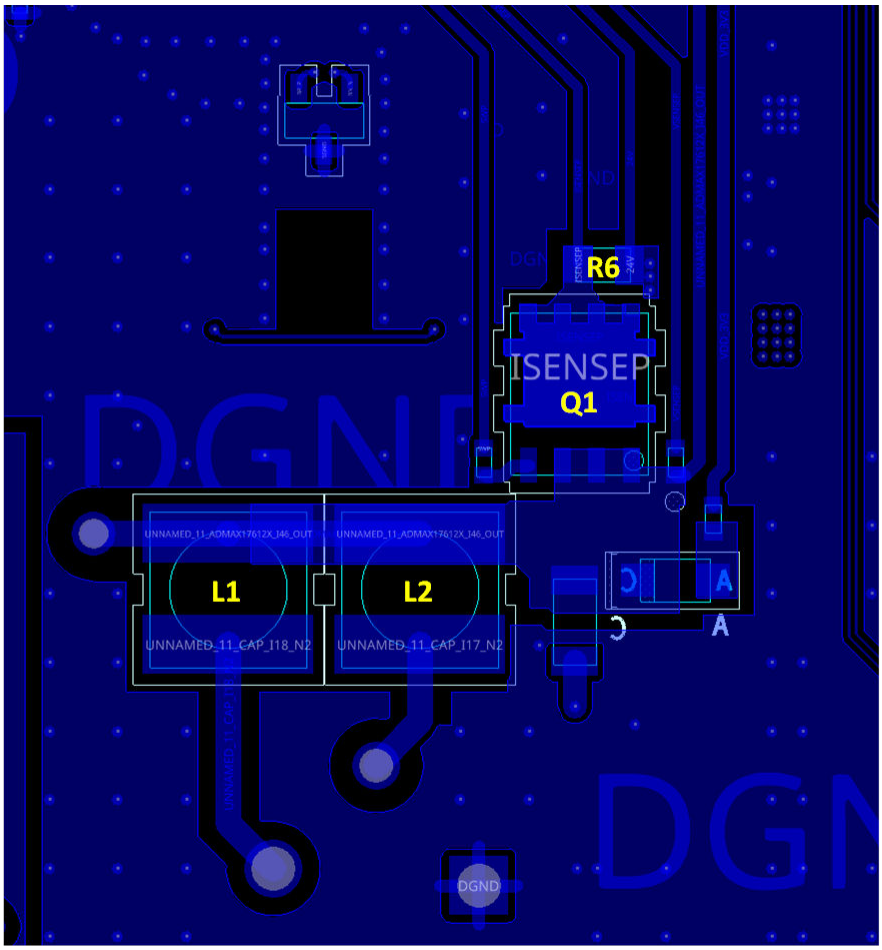

Figure 3-16: DC Bias Component Placement

Decoupling Capacitor Placement

Place power supply decoupling capacitors near IC pins. When multiple decoupling capacitors are specified, the lowest-capacitance component must be located closest to the pin. Refer to Power Supply Design for decoupling capacitor requirements for the A^{2}B transceiver.

Place the ACM and BCM decoupling capacitors as close as possible to transceiver pins. Place the smallest value capacitor (for example, 100 nF) on the same layer as the A^{2}B transceiver and mounted close to the transceiver pin (pin 27 and 35). Place the 4.7 µF capacitor as close as the layout allows to the ACM/BCM pin.

Place the 10 µF capacitor close to the VOUT1 pin (pin 47). Place the PLLVDD/DVDD decoupling capacitor, the smallest value (for example, 10 nF) capacitors on the same layer as the A^{2}B transceiver and mounted close to the PLLVDD (pin 48) and to the DVDD pin (pin 2 and 3).

Place the VOUT2 decoupling capacitor, the smallest value (for example, 10 nF) capacitor on the same layer as the A^{2}B transceiver and mounted close to the TRXVDD pin (pin 31). Place the 100 nF capacitor close to the TRXVDD pin (pin 31). Place the 10 µF capacitor close to the VOUT2 pin (pin 45).

Place the IOVDD decoupling capacitors, the smallest value (for example, 100 nF) capacitor on the same layer as the A^{2}B transceiver and mount close to the IOVDD pins (pin 11 and 21).

Place the VIN decoupling capacitor, the smallest value (for example, 100 nF) capacitor on the same layer as the A^{2}B transceiver and mount close to the VIN pin (pin 46). Place the 10 µF capacitor close to the VIN pin (pin 46).

Place the RC filter circuit for the I^{2}S signals close to the source to control emissions.

For the main transceiver, place the RC filter circuit for BCLK, SYNC, DRX0, and DRX1 signals close to the host (MCU). Place the RC filter circuit for DTX0 and DTX1 signals close to the A^{2}B transceiver.

For subordinate transceivers, place the RC filter circuit for BCLK, SYNC, DTX0, and DTX1 signals close to the A^{2}B transceiver. Place the RC filter circuit for DRX0 and DRX1 signals close to the peripheral.

Signal Routing

Route the signals based on the following recommendations.

1. The AP/AN and BN/BP signal pairs must be routed differentially at 100 Ω ±10% . The differential impedance depends on:
   - S1 – Separation between the signals (BP and BN, AP and AN)
   - S2 – Separation between the signal and ground shield (on the same plane)
   - H – Height from the reference ground plane
   - W – Trace width of the signal. Choose a wider trace width to minimize the mismatch created by component pads.

   The impedance also depends on the PCB material (for example, the dielectric constant of the substrate material). The condition

   S2 >2 * MAX (S1, H, W) and S1 < H must be satisfied.

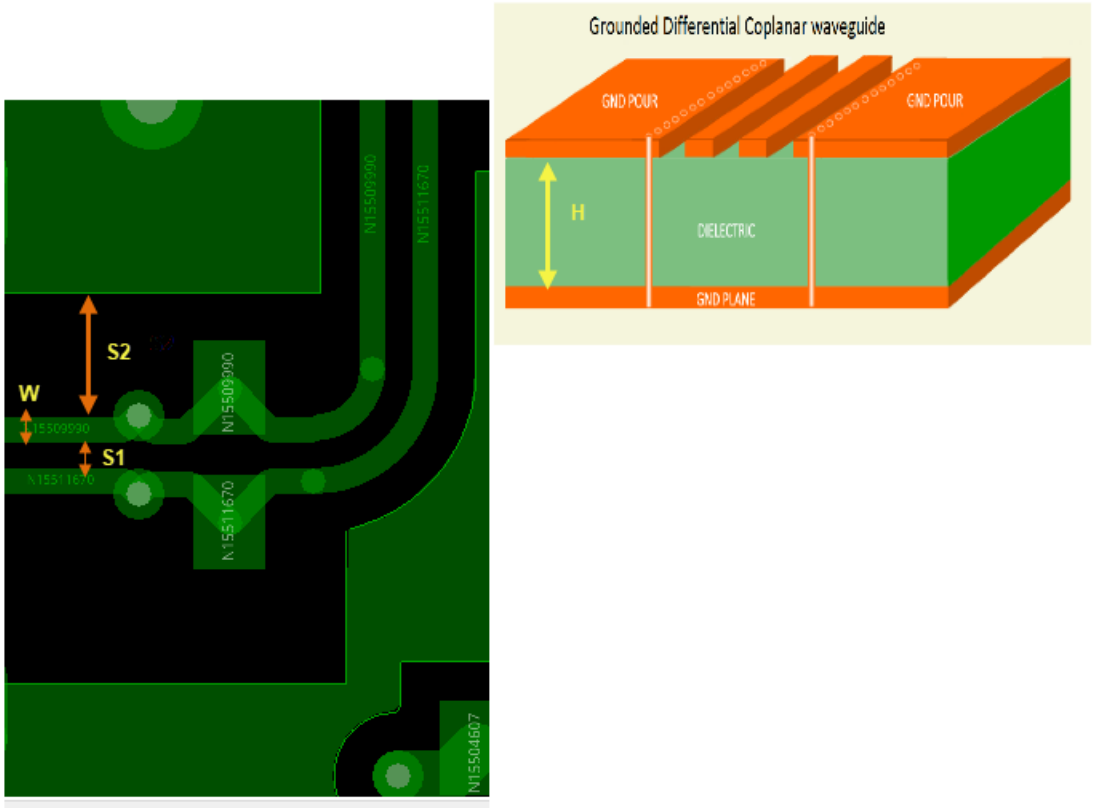

Figure 3-17: Impedance Variables

2. Route the P and N lines of differential pair (AP/AN, BP/BN) symmetrically and ensure that trace length of P and N lines of differential pair (AP/AN, BP/BN) symmetrically is matched within typical 10 mils to maximum 100 mils.

   - Avoid serpentine routing on only one of the differential pair line (either AP/AN or BP/BN) to match length. When using serpentine routing, use it for both differential signals (P and N) to maintain differentiality.
   - Use the shortest possible AP/AN and BP/BN signal pair traces between the A^2B connector and transceiver.
   - Avoid B-port and A-port differential signals crossing in the PCB layout.

   The *A^2B Signal Routing* figure shows the A^2B signals routed as a differential pair with 100 Ω differential impedance.

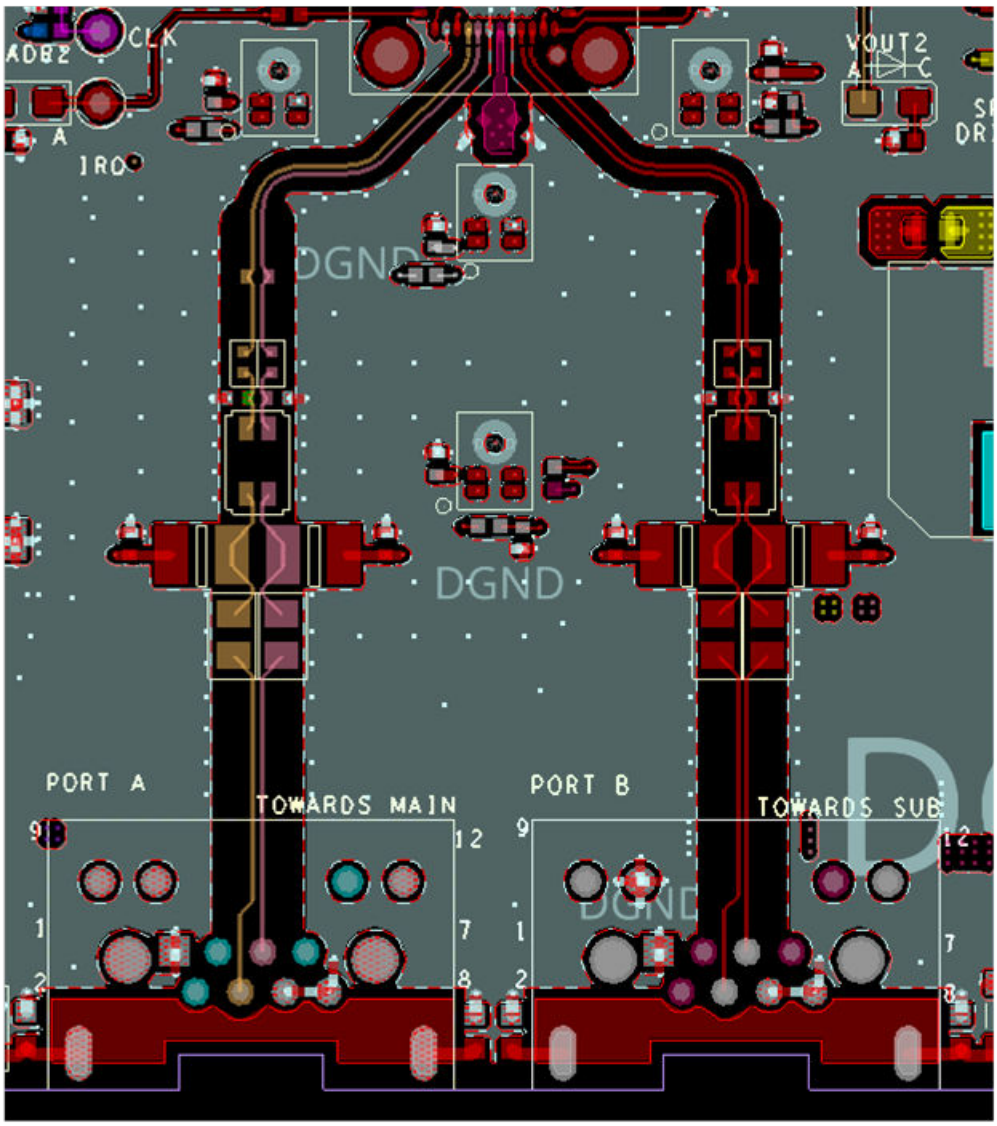

Figure 3-18: A^{2}B Signal Routing

3. Provide symmetrical ground guarding and ground vias for A^{2}B signals.
   - The minimum width of the AP/AN and BP/BN ground shield is 0.5 mm.
   - Provide symmetrical ground stitching vias around A^{2}B differential traces for symmetry and shielding.
   - Provide symmetrical ground shielding for equal parasitic capacitance and inductance on adjacent sides of the A^{2}B differential signals.
4. Place and route bias components and traces on the opposite side of the board as the transceiver, while data traces and components are located on the same side as the transceiver.
5. Add a ground shield between A-port and B-port differential signals/components to reduce cross talk.
6. Avoid trace stubs in AP/AN and BP/BN signal routing.

7. There must be no unnecessary layer transitions. The *A²B Signal Routing* figure shows the recommended layer transitions. Traces should be routed with the reference ground plane adjacent to the A²B signal on the top and bottom layers (adjacent). Provide a minimum of two ground stitching vias close to the A²B signal vias when a layer transition is required.

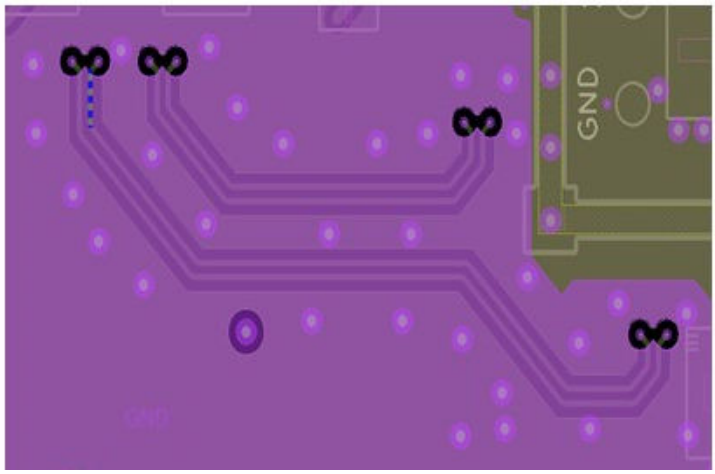

Figure 3-19: A²B Signal Routing

8. Remove the ground plane under the CMC (CMC1, CMC2) on all PCB layers. See the *CMC Keep Out Area* figure.

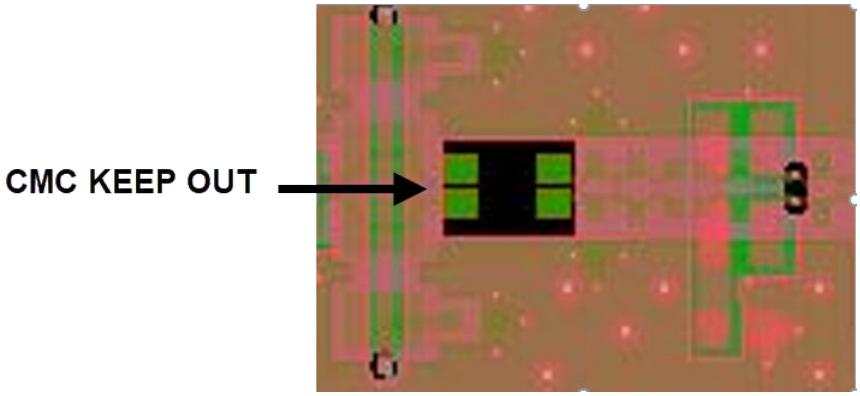

Figure 3-20: CMC Keep Out Area

9. Do not route any signals close to the CMC (CMC1, CMC2) on all layers; provided at least 0.5 mm spacing from the route keep-out area to any other signals on all layers.
10. Remove ground pouring in between the component pads of AC coupling capacitors, split termination resistors and inductors of the bus interface networks as shown in below figure.

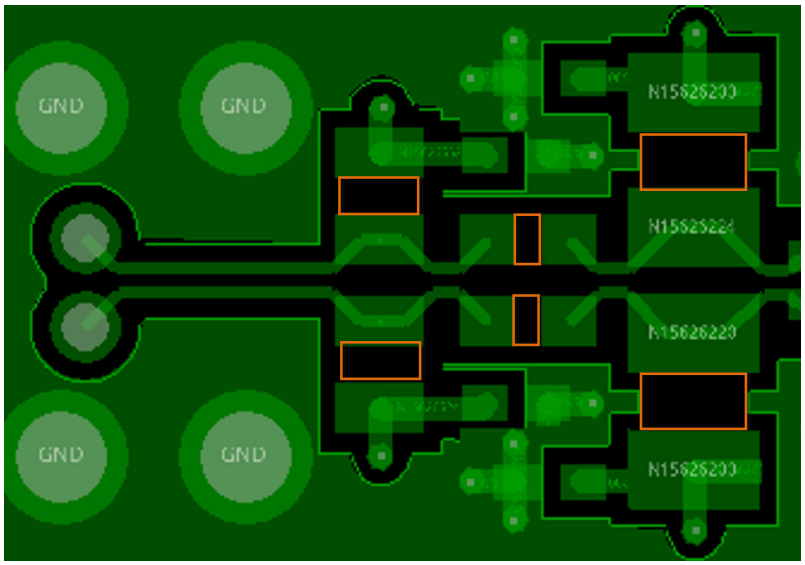

Figure 3-21: Ground Pour Removed

11. Separate all magnetic components (for example, inductors and chokes) by at least 2 mm.

    The *CMC Separation* figure shows the recommended common mode choke separation.

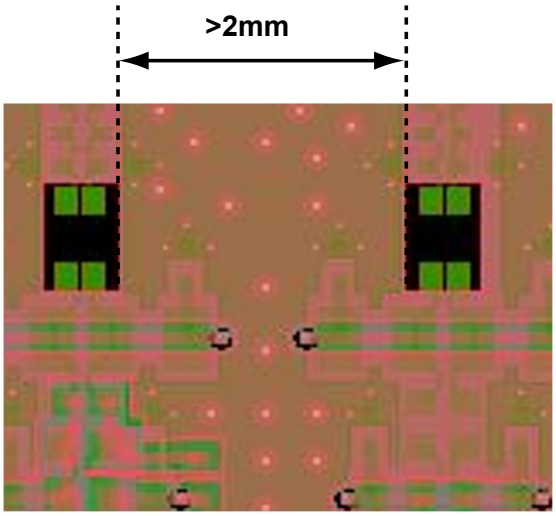

Figure 3-22: CMC Separation

12. When routing the signal near the connector, make the signal path on the connectors as short as possible (inner row on right-angled connectors). Remove the ground pouring in between BP and BN pins in the connector on all layers for through hole connectors. Remove ground pouring in between AP and AN pin in the connector on all layers for through hole connectors.

13. The VBUS pin is not a power input pin and does not draw a substantial amount of current. This pin is a sense pin that works in conjunction with the ISENSEP pin to measure the current across the sense resistor R6. It is critical that these traces are matched for best measurement. The primary current path of the bus bias flows through R6 and Q1and does not flow to or through the VBUS pin.

Footprint

Follow the recommended land pattern for the footprint creation and thermal via consideration. Follow the recommendations given in the product-specific data sheet. The *Thermal Vias* figure shows the thermal vias recommendation.

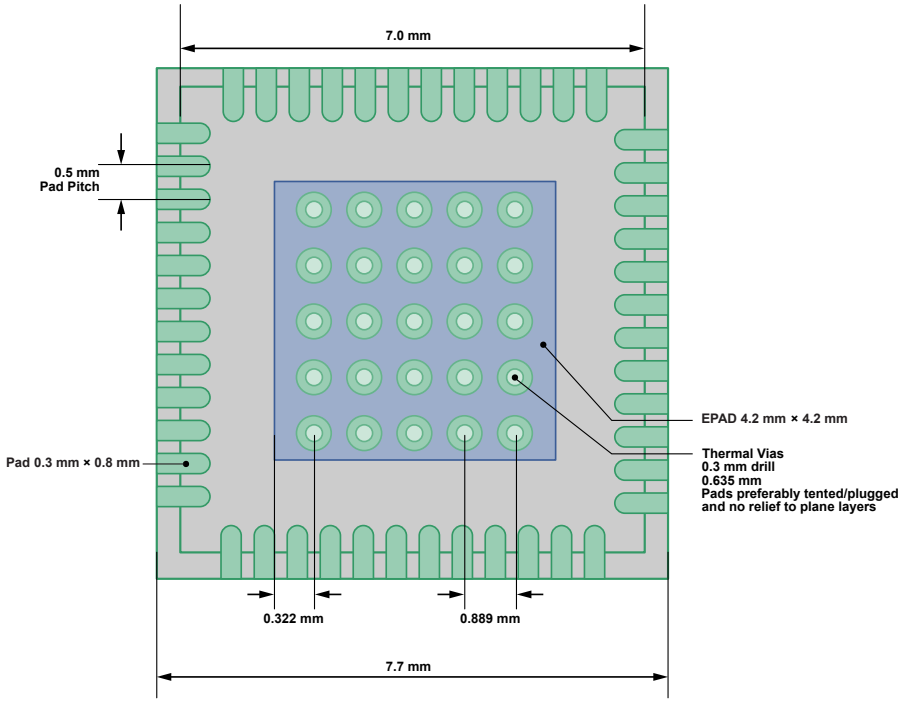

Figure 3-23: Thermal Vias

Power Supply Routing

Route the power supply signals based on the following recommendations.

1. Add power shape connecting the VOUT1 (pin 47) and PLLVDD (pin 48), DVDD (pin 2, pin 3) pins.
2. Keep the ground connection for the A^2B transceiver ground pins short.
3. Avoid other power or return-currents pass near or underneath A^2B circuit.
4. Switching signals must not pass near or underneath the A^2B circuit.

I^2S and Clock Signal Routing

Route the I^2S signals based on the following recommendations.

1. I^2S signals (clocks/data) should have continuous ground reference on adjacent layer/ immediate ground reference.
2. I^2S signals must be routed with ground guarding or provided 3x spacing for I^2S signal to any other signals.
3. Clock output (for example, BCLK for subordinate) buffered (if needed) and routed in star (routing) topology, provided more than one I^2S subordinates are connected.

Spacing

Consider the following spacing recommendations.

1. Sources of crosstalk such as other high-speed signals must be routed away from the A-port *and* B-port differential signals by 3 mm minimum.
2. Flood the design with ground pour, where possible, except under the CMC.

Data Link Layer

This section provides details for the A^{2}B transceiver data link layer specification. It describes the transmission protocols and digital interfaces in the A^{2}B bus system.

Transmission Protocol - A^{2}B Superframe

The transmission protocol consists of the A^{2}B superframe that occurs periodically. The superframe frequency must be either 48 kHz or 44.1 kHz. It starts with an SCF and includes an SRF and optional data slots. The superframe repeats every 1024 bus clock cycles. The *Superframe Structure* figure shows the structure of the A^{2}B superframe communication.

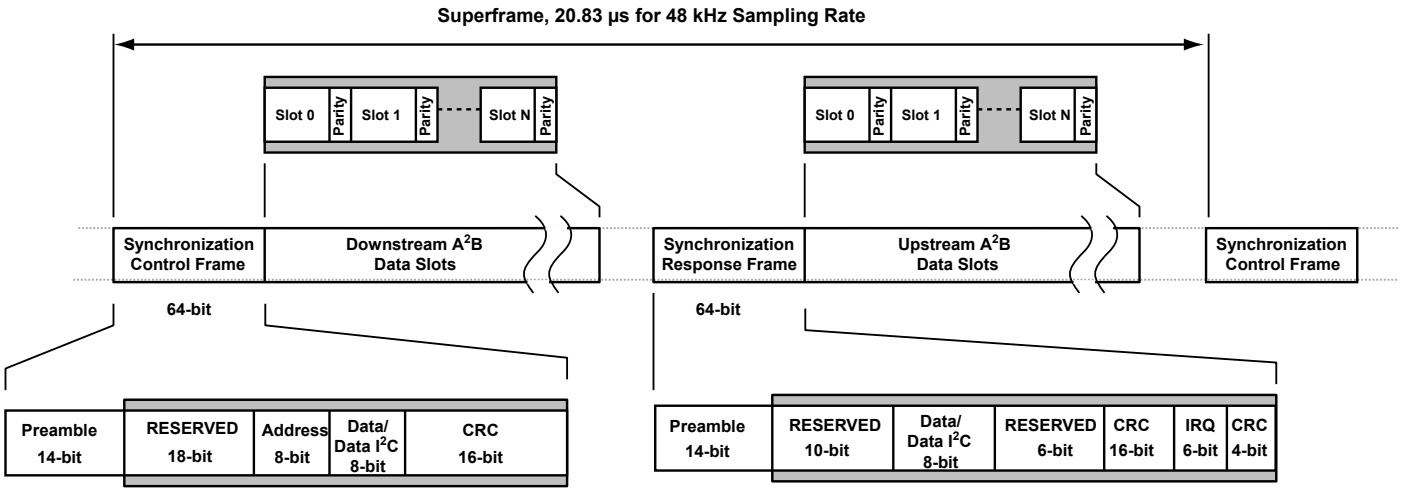

Figure 3-24: Superframe Structure

Audio Sampling Frequency

The audio sampling rate of the A^{2}B transceiver is either 44.1 kHz or 48 kHz. The A^{2}B subordinate nodes support alternate I^{2}S frame rates, which are related to the main node frame rate. All subordinate nodes support multiples and divisors of the frame rate.

I²S/TDM Data and Clock Frequency Settings

The I²S/TDM serial port operates in full-duplex mode, where both the transmitter and receiver operate simultaneously using the same critical timing bit clock (BCLK) and synchronization (SYNC) signals. The A²B subordinate transceivers generate the timing signals on the BCLK and SYNC output pins based on the I²S configuration. The A²B main transceivers use the same BCLK and SYNC pins as inputs, which are driven by the host device.

The I²S/TDM serial port supports data channel widths of 16 or 32 bits to carry data of variable word length.

Data Channel Structure of TDM Mode/Slots

I²S/TDM mode extends an I²S interface to more than stereo (2-channel). The I²S/TDM interface uses equally-sized data channels, where the word length is often smaller than the I²S /TDM data channel. The I²S /TDM interface of the transceiver supports programmable data channel lengths of 16 and 32 bits.

I²C Interface

The I²C interface is used to transmit control information over the A²B bus. This allows the locally connected host to directly access the transceiver register space.

For the A²B main transceiver, the I²C port is always a subordinate.

For A²B subordinate transceivers, the I²C port can be the main or subordinate and supports multi-main operation.

The host uses two I²C device addresses when communicating with the main transceiver:

- MSTR_ADDR to access the register space of the main transceiver
- BUS_ADDR to access the register space of any discovered subordinate transceiver or peripheral attached to a discovered subordinate

The *I²C Connection Interface* diagram shows the I²C connection between the subordinate nodes and the peripheral chip.

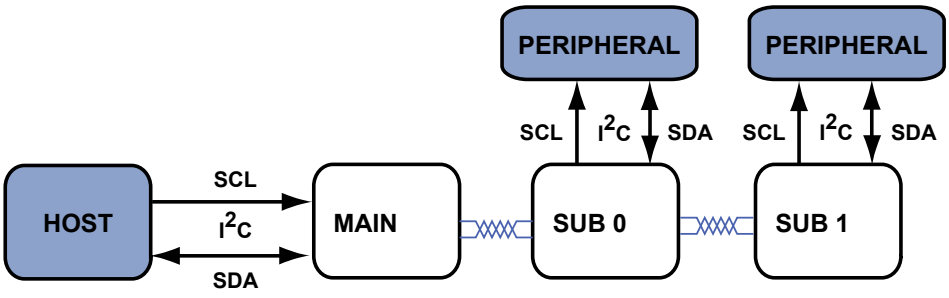

Figure 3-25: I²C Connection Interface

The transceiver uses I^2C clock stretching to ensure that I^2C accesses to peripherals attached to a subordinate have enough time to complete the I^2C transaction over the A^2B bus.

Pulse Density Modulation (PDM) Interface

The PDM block on the transceiver supports high dynamic range microphones with high signal-to-noise ratio (SNR) and extended maximum sound pressure level (SPL). The PDM block on the transceiver supports 12 kHz, 24 kHz, and 48 kHz frame rates. Even lower PDM sampling rates (for example, down to 375 Hz) are possible when the transceiver's reduced rate feature is enabled. The cutoff frequency of the high-pass filter in the transceiver PDM block is fixed to 1 Hz. Dynamic range with an A-weighted filter (rms) operates from 20 Hz to 20 kHz, –60 dB input.

For details on PDM enhancements and features, see the AD2437 programming reference manual.

Bit Error Correction

The data transmitted over the A^2B bus can be affected by signal distortion or interference. To ensure that the system is not affected by these phenomena, the A^2 B transceiver features robust error detection for control and response data. The SCF and SRF use CRC error correction, and each synchronous data slot uses a parity bit for error detection. If a bit error is detected in a data slot or in the SCF or SRF, the previous known good value is repeated. Additionally, ECC protection can be enabled on the I^2S/TDM data slots when the data width is 24- or 32-bit.

Bit errors that may occur during data communication can be classified into two categories: data errors and control and response errors.

Data errors include the following:

- Data parity error (DPERR)
- Data decoding error (DDERR)

Control and response errors include the following:

- SRF missed error (SRFERR)
- CRC error (CRCERR)
- SRF CRC error (SRFCRCERR)
- Header count error (HDCNTERR)
- Interrupt frame CRC error (ICRCERR)

Multiple bit errors affect audio data communication more than single-bit errors. The host uses the information contained in the error management registers for handling the errors. These registers help in setting a threshold to provide notification to the host.

For more information regarding types of bit error and error handling, refer to the application note *Bit Error Management in A^2B Communication (EE-406)*.

4 Fault Diagnostic Requirements

The A^{2}B transceiver supports line fault diagnostic functionality. It is intended to detect and localize the most commonly anticipated cabling faults in a typical digital audio and control distribution system using A^{2}B software. The A^{2}B stack follows a plug-in architecture for each node (main and subordinate node).

Using diagnostics during debug activities is one of the powerful features of the A^{2}B stack. The diagnostic module in the A^{2}B stack API performs power and line fault diagnostics whenever network discovery or communication fails. The diagnostics are reported back to the application through the diagnostic event handler registered with the stack.

Line Diagnostics During Discovery

The ***Line Faults*** table shows the different types of line faults and the pins affected by the faults. All faults can be detected and localized during bus discovery. When a fault is detected during discovery, the switches that enable bias current to the next-in-line node are automatically disconnected.

Table 4-1: Line Faults

Wires	Affected Pins	Detect	Localize	INTTYPE Register Value	Remarks
Partial Bus Operation May Continue for Nodes Upstream from the Fault					
Open	BP	Yes	Yes	0x0C	Open wires (BP and BN are the B-side positive and negative connector pins)
	BN				
	BN and BP				
Wrong Port	B to B' port	Yes	Yes	0x0C or 0x0D	B’ is B-side of next-in-line node
Reverse Wires	BN to AP and BP to AN	Yes	Yes	0x0D	Wrong port or reverse wires (AP is the A-side positive connector pin of the next-in-line node)
				No 0x18 timeout (no DSCDONE interrupt)	Reverse wires undetected by hardware diagnostics
Defective Node	N/A	Yes	Yes	No 0x18 timeout (no DSCDONE interrupt)	Defective node or wrong software parameter value for A2B_DISCVRY.DRESPCYC

Table 4-1: Line Faults (Continued)

Wires	Affected Pins	Detect	Localize	INTTYPE Register Value	Remarks
Short of Wires	BP with BN	Yes	Yes	0x0B	Wires shorted together
Critical Faults					
Short to Ground	BP	Yes	Yes	0x09	Positive wire shorted to ground
	BN		Yes	0x29	Software routine localizes fault
Short to V_{BAT}	BN	Yes	Yes	0x0A	Negative wire shorted to V_{BAT}
	BP		Yes	0x2A	Software routine localizes fault

NOTE: For all critical faults except BN short to GND, the fault can only be detected by the immediate local powered subordinate/main. The detecting node isolates the fault by shutting down the bus downwards. Normal A^2B bus operation must be discontinued, including removal of bus power by the main node (independent of line fault location).

For the following faults, partial A^2B bus operation can continue between the main and subordinate nodes which are upstream from the line fault location.

- Open
- Wrong port
- Reverse wires
- Defective node
- Wrong discovery parameter for next-in-line node
- Wires shorted together

The following line faults terminate communication between the main and subordinate nodes:

- BP short to GND
- BN short to V_{BAT}
- BN short to GND
- BP short to V_{BAT}

For details on line faults, refer to the A^2B System Debug section in the product-specific programming reference manual.

Line Diagnostics After Discovery

Full line diagnostics are only performed during discovery. However, certain interrupts (if enabled) after discovery indicate line faults during operation. A re-discovery detects the cause and location of any possible faults. After discovery, any of the following interrupt types indicate that there is a line fault:

- BP short to V_{BAT} – 0x0F or 0x80
- BN short to V_{BAT} – 0x80, 0x0F, or 0x05
- BP short to GND – 0x0F
- BP to BN short – 0x0F

5 System-Level Test Requirements

This section provides details on the system-level tests that must be performed to ensure reliable A^{2}B operation.

NOTE: This information is intended to enable the manufacturing and testing of A^{2}B nodes that comply with the A^{2}B specification. The information is provided on an "as is" basis and all warranties, either explicit or implied are excluded unless mandatory by law.

Eye Diagram

Eye diagrams are commonly used to analyze the signal integrity of high-speed differential transmissions. For A^{2}B transceivers, they also help to verify the complete A^{2}B link involving the A^{2}B transmitter, BIN, PCB cable and the connector.

The ***Eye Diagram Measurement*** figure shows a generic set up for an eye diagram measurement.

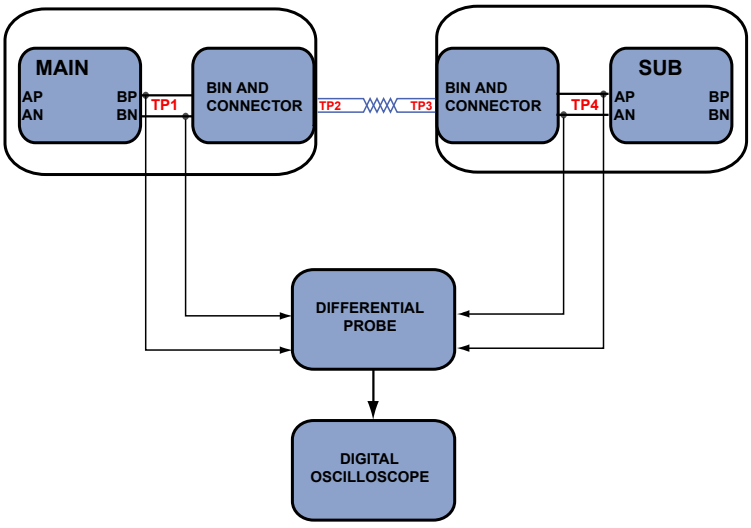

Figure 5-1: Eye Diagram Measurement

The *Eye Diagram Mask* figure shows the eye mask for A^{2}B 1.0 systems with cable lengths of 1.7m and 15m. To meet the eye mask requirements of the A^{2}B system (avoid signal distortion and achieve optimal EMC performance), ensure that the A^{2}B link complies with the A^{2}B reference schematics.

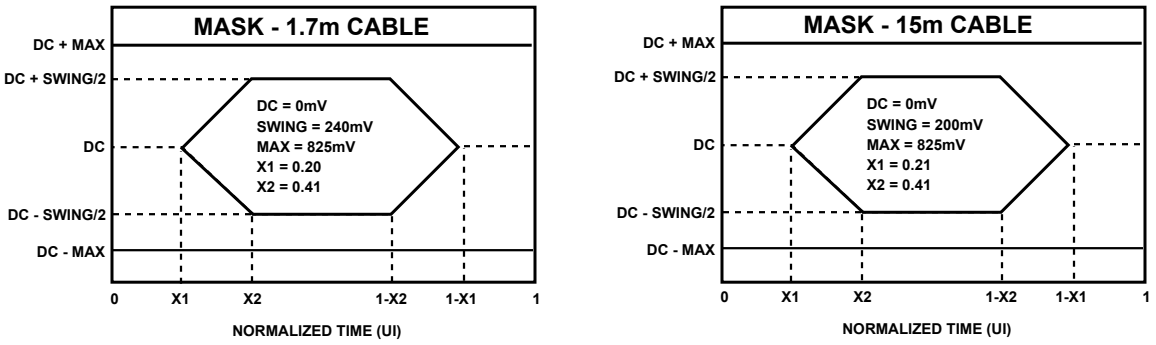

Figure 5-2: Eye Diagram Mask

For more information regarding eye diagram measurement, refer to the application note *Eye Diagram Measurement in AD242x A²B Transceiver-Based Systems (EE-369)*.

Power Spectral Density Test

Power Spectral Density (PSD) tests verify the transmitter performance of the A²B system with BIN. To meet the PSD limits outlined in the ***PSD Frequency Limits*** table and achieve optimal EMC performance, ensure that the A²B transceiver and external BIN components are used in compliance with the latest A²B reference schematics. The ***PSD Test Set Up*** figure shows a generic set up for a PSD test.

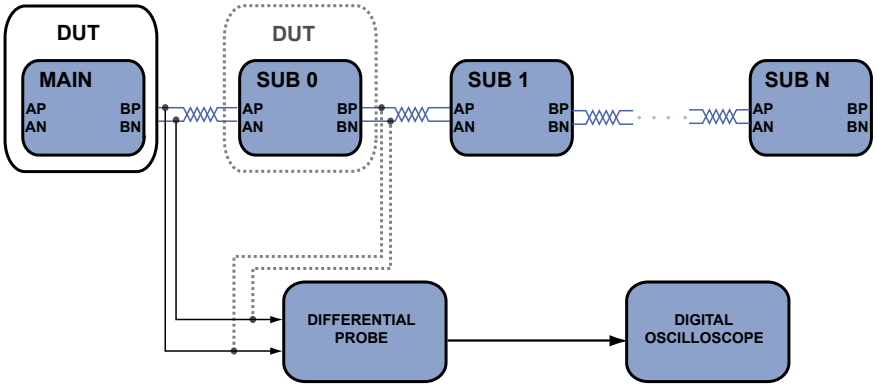

Figure 5-3: PSD Test Set Up

Table 5-1: PSD Frequency Limits

Critical Frequency (MHz)	Minimum (dBm)	Maximum (dBm)
5	-42	-22
22	-28	-10
50	-28	-10
70	-42	-19.8

Table 5-1: PSD Frequency Limits (Continued)

Critical Frequency (MHz)	Minimum (dBm)	Maximum (dBm)
100 - 180	N/A*1	-34.5
200 - 280	N/A*1	-52
300 - 500	N/A*1	-61

*1 Minimum limits apply only to the the main lobe of the PSD curve

Figure 5-4: PSD Limits Graph

For more information regarding PSD measurement, contact your ADI representative.

Bus Monitor Mode

The A^{2}B test equipment uses a bus monitor mode, which enables a transceiver to act as a passive A^{2}B bus monitor, also referred to as a "sniffer".

If the monitoring of data slots is desired, the host must enable the feature (`A2B_DATCTL.ENDSNIFF` =1) in the main transceiver after the bus monitor is attached and running. This scrambling mechanism provides a level of content protection to the synchronous data on the A^{2}B bus. Add this write to the debug mode of infotainment system to assist with A^{2}B network debugging.

A bus monitor that attaches to an A^{2}B bus after discovery and initialization can miss the broadcast; the monitoring of the synchronous data slots is disabled. The preferred method is to attach bus monitors before initialization and discovery.

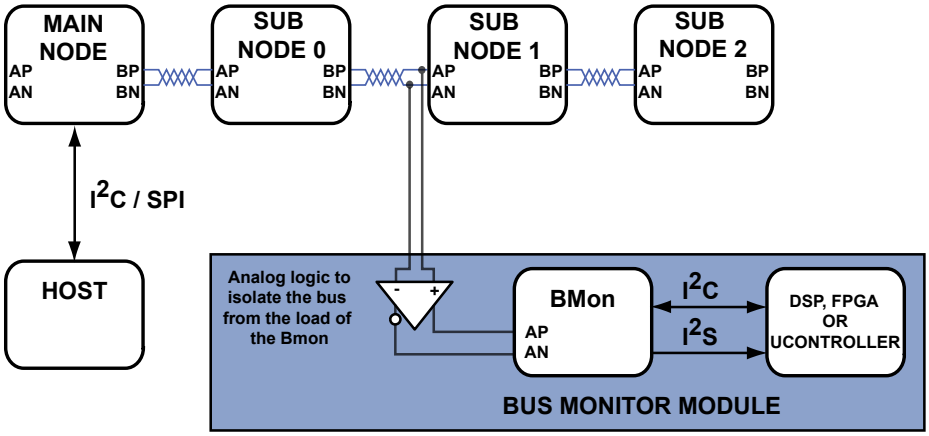

Figure 5-5: Bus Monitor Behavior

A bus monitor node behaves as follows:

- The B-Side (downstream) transceiver is disabled
- The A-Side (upstream) transceiver is enabled to receive only (not to transmit)
- SRF generation is disabled
- The I^{2}S/TDM interface is configured for 32-bit data width
  - Downstream SCFs are transmitted on the DTX0 pin
  - Upstream SRFs are transmitted on the DTX1 pin
  - Data slot bits can only stream out of the DTXn pins if the A^{2}B bus main transceiver is programmed to enable this feature
    - Downstream slots are streamed out on the DTX0 pin
    - Upstream slots are streamed out on the DTX1 pin
    - If there are more data slots on the A^{2}B bus than there are available I^{2}S/TDM channels, then a programmable offset determines which data slots are monitored on the I^{2}S/TDM channels

NOTE: When the bus monitor receiver is disabled, an external switch must be used to control the LVDS traffic going to the A-side of a transceiver in bus monitor mode.

Appendix A BOM

The *BOM* table provides a detailed list of the components required for the AD2437 transceivers.

IMPORTANT: Contact ADI for the latest A^{2}B reference schematics and a detailed BOM for each type of A^{2}B node, as well as a list of acceptable substitute components, if needed.

Table A-1: BOM

Item Number	Reference Description	Type	Value	Size	Metric	Recommended Part No.	Remarks
1	C23, C24, C30, C31, C33, C35	Capacitor	33 nF ±10%, ≥35V, X7R	0402	1005	CGA2B3X7R1H333K050BB	
2	C21, C22, C28, C29[*1]	Capacitor	10 nF ±5%, ≥35, C0G/NP0	0603	1608	GRM1885C1H103JA01J	
3	C3,[*2] C6, C9, C10	Capacitor	10 nF ±5%, ≥35, X7R	0402	1005	C1005X7R1H103K050BB	
4	C51	Capacitor	10 nF ±5%, ≥2000, X7R	1812	4532	C1812C103KGRACTU	
5	C7, C8, C11, C5, C14, C16, C18	Capacitor	0.1 µF ±10%, ≥6.3 V	0402	1005	C1005X7R1V104K050BB	
6	C2[*2], C13	Capacitor	0.1 µF ±10%, ≥35 V	0402	1005	C1005X7R1V104K050BB	
7	C25, C32	Capacitor	12 pF ±10%, ≥16 V	0402	1005	CGA2B2C0G1H120J050BA	
8	C15, C17	Capacitor	4.7 µF ±10%, ≥6.3 V	0603	1608	CGA3E1X5R0J475K080AC	
9	C1[*2], C4, C12,	Capacitor	4.7-10 µF ±10%, ≥10 V	0805	2012	GRM21BR71A106MA73K	
10	C35, C49	Capacitor	4.7 nF ±10%, ≥50 V	0402	1005	CGA2B2X7R1H472K050BA	
11	C20	Capacitor	47 µF – 1000 µF ≥35 V			Electrolytic	Must be no more than 1000 µF
12	C47, C48, C49, C50	Capacitor	27 pF ±5%, ≥16V	0402	1005	CGA2B2C0G1H270J050BA	

Table A-1: BOM (Continued)

Item Number	Reference Description	Type	Value	Size	Metric	Recommended Part No.	Remarks
15	R9, R10, R17, R18	Resistor	120 Ω ±1%, ≥1/2W	1210	3225	CRCW1210120RFKEA	≥1/2W is required to meet 200 mA BCI test level using substitution method
	R33, R34	Resistor	100 Ω ±1%, ≥1/2W	1210	3225	ERJ-P14F1000U	≥1/2W is required to meet 200 mA BCI test level using substitution method
	R7, R19	Resistor	100 Ω ±1%, ≥1/16 W	0402	1005	ERJ-2RKF1000X	
	R5, R22	Resistor	10 kΩ ±1%, ≥1/16 W	0402	1005	ERJ-2RKF1002X	
17	R1, R2, R21	Resistor	100 kΩ ±1%, ≥1/16 W	0402	1005	ERJ-2RKF1003X	
18	R6	Resistor	0.05 Ω ±1%, ≥1/8 W	0805	2012	WSL0805R0500FEA	Current sense resistor
	R8, R20, R27, R28, R35, R36, R43	Resistor	Multiple values	0402	1005		LED indication current/brightness limiting
21	L3, L4, L5, L6	Inductor	180 nH ±5%, ≥50 mA, Rdc-typ 2.88 Ω	0402	1005	MLG1005SR18JTD25	Unshielded multilayer
	L1, L2, L7, L8	Inductor	4.7 uH ±30%, ≥2 A, Rdc-typ 38mΩ	2323	5858	7440530047	Shielded power inductor
	T1	Transformer	1:1 signal transformer			74930000	T1
	P1	A^2B XLR-F connector	Neutrik Halo XLR-F			NC3FAH2-LR-DAE	B-port XLR connector
	P2	A^2B XLR-M connector	Neutrik Halo XLR-M			NC3MAH-LR	A-port XLR connector

Table A-1: BOM (Continued)

Item Number	Reference Description	Type	Value	Size	Metric	Recommended Part No.	Remarks
	P3, P4	A2B RJ45 Connector	8-pin shielded RJ45 with LED option			RJE73-188-00210, NE8FAH-LR-DAE	
22	Q1	NMOS-FET	Vds ≥ 40 V, Vgs ± 20 V, VGS(TH) 1.2-2.0 V	Power DI5060-8		DMTH8012LPSQ-13	See NMOS section for details
23	D1, D4	Diode	Schottky			PMEG6010CEH,115	
24	D2, D10	Diode	TVS 30V	SOD-123		TPSMF4L30A	ESD suppression diode
25	D3	Diode	27V Zener	SOD-123		BZT52C27-7-F	Over voltage protection
	LED1-LED4	LED	SMD LED blue	0603	1608	LB L293-L2N1-25-1-Z	Neutrik light ring XLR LED indication. Blue is standard color for A2B
26	U1	AD2437 transceiver		48-LFCSP 7 x 7		Analog Devices	See ordering guide
ADI Approved Critical (*) Components							
27	CMC1, CMC2	CM choke	ACT1210L1012P TL00 / DLW32MH101X K2L/ AMCW3225L-2-1 01T/ VFC3225-101	ACT1210 / DLW32/ AMCW3225/ VFC3225		ACT1210L1012PTL00* / DLW32MH101XK2L*/ AMCW3225L-2-101T*/ VFC3225-101	Symmetric L-type choke

Table A-1: BOM (Continued)

Item Number	Reference Description	Type	Value	Size	Metric	Recommended Part No.	Remarks
28	L9, L10, L12, L13*3 *4	Inductor	3.3uH ±8%, 500mA / 3.3uH ±5%,425mA	0805 / 1210	2012 / 3225	MLZ2012M3R3ATD69*/ LQH32NH3R3J23*	Meets CCC requirements up to ISO-7637-3:2016 level 4 (+/-110V)
			10uH ±5%, 325mA	1210	3225	LQH32NH100J23L*	Meets CCC requirements higher than ISO-7637-3:2016 level 4; tested up to the test equipment limitation of +/-200V max.

*1 Actual pulse rating depends on bus-bias voltage and components worst case tolerances. Customer need to perform WCCA analysis of their design and arrive at the required rating.

*2 Not needed when in low voltage input (LVI) mode.

*3 To maintain symmetry, use the same part number on positive (AP/BP) and negative (AN/BN) lines of A^{2}B differential pair. The parts can be different between A and B ports.

*4 Alternatives for inductors are not footprint compatible. Ensure the availability of selected inductors, or, alternatively, have PCB provision to mount both packages.

Appendix B Power Supply Design

The VOUT1, VOUT2, PLLVDD, DVDD, IOVDD, and TXVDD pins supply power to the A^{2}B transceiver. There must be adequate decoupling on these pins. The recommended capacitor value for each pin is shown in the *Capacitor Recommendations* table.

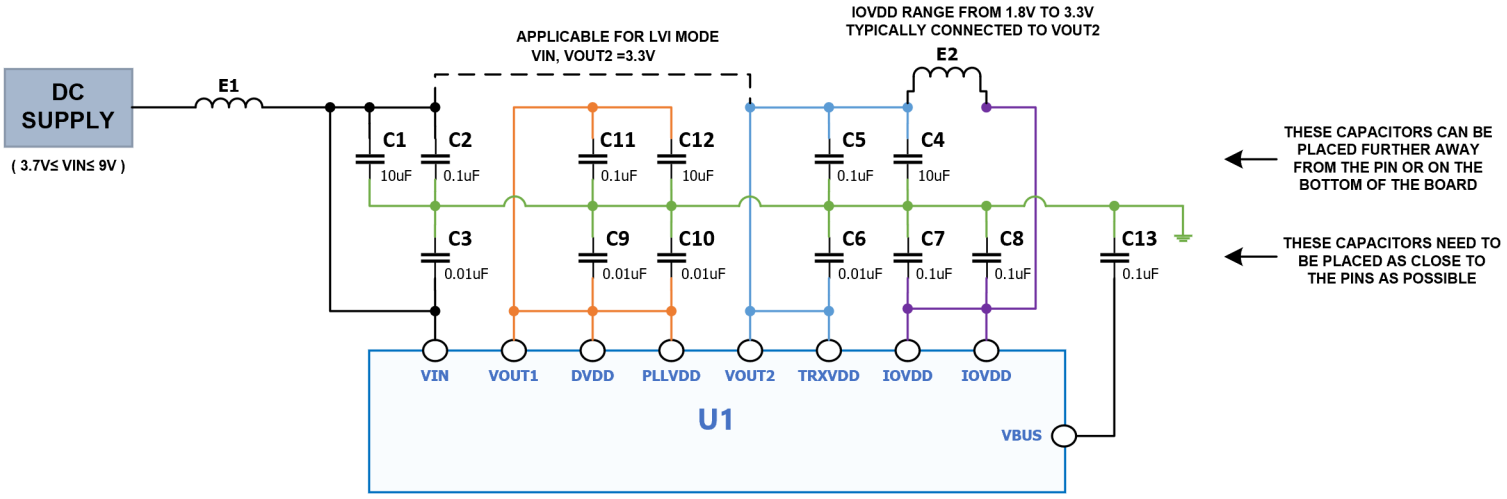

Figure B-1: Decoupling Capacitors

The *Decoupling Capacitors* figure shows the minimum number of decoupling capacitors required for the A^{2}B transceiver. More decoupling capacitors can be used than shown in the figure; however, it is mandatory to meet the minimum number to ensure proper functioning and acceptable EMC performance of the A^{2}B transceivers. The *Capacitor Recommendations* table shows the decoupling capacitor recommendations.

Table B-1: Capacitor Recommendations

Capacitor Function	Recommendation
VIN Decoupling	The VIN pin must have at least one 0.1µF (C2) capacitor close it along with a 10 µF (C1) bulk capacitor. Follow the voltage rating as mentioned in the A^{2}B circuit recommendation for these capacitors.
VOUT1 Decoupling	Use at least one 4.7 µF (C12) bulk capacitor for regulator loop stability.
PLLVDD Decoupling [*1]	Use at least one 10 nF (C10) high-frequency decoupling capacitor close to the PLLVDD pin.
DVDD Decoupling[*1]	Use at least one 10 nF (C9) high-frequency decoupling capacitor close to the DVDD pin.
VOUT2 Decoupling	Use at least one 4.7 µF (C4) bulk capacitor for regulator loop stability.

Table B-1: Capacitor Recommendations (Continued)

Capacitor Function	Recommendation
TRXVDD Decoupling	Use at least one 10 nF (C6) high-frequency decoupling capacitor and one 0.1 µF (C5) decoupling capacitor close to the TRXVDD pin, with the 10 nF being nearest to it.
IOVDD Decoupling	IOVDD can be supplied externally, and it must have at least one high-frequency 0.1 µF (C7 and C8) decoupling capacitor at each IOVDD pin and a bulk capacitor of 10 µF close to the transceiver.

*1 If PLLVDD and DVDD are supplied externally, ensure that appropriate decoupling capacitors are present. There must be a minimum load capacitor always present on VOUT1. Refer to the product-specific data sheet for the minimum load capacitor requirement.

Power supply noise created by companion peripherals such as amplifiers or a codec must be adequately filtered. The noise (from VCC or GND) can couple into A^2B signals lines and diminish EMC performance.