

## Evaluating the **ADRF6620**, a 700 MHz to 2700 MHz Rx Mixer with Integrated IF Amplifier, Fractional-N PLL, and VCO

### FEATURES

- Full-featured evaluation board for the **ADRF6620**
- On-board USB for SPI control
- Single +5 V operation
- C# software interface for serial port control

### EVALUATION KIT CONTENTS

- ADRF6620** evaluation board
- USB cable

### ADDITIONAL EQUIPMENT NEEDED

- Analog signal sources
- Power supply (6.0 V, 2.5 A)
- PC running Windows® 98 (2nd ed.), Windows 2000, Windows ME, Windows XP, or Windows 7
- USB 2.0 port, recommended

### SOFTWARE NEEDED

- ADRF6620** control software

### ONLINE RESOURCES

- ADRF6620** data sheet
- ADRF6620-EVALZ** user guide

### GENERAL DESCRIPTION

The **ADRF6620** is a highly integrated active mixer and synthesizer ideally suited for next generation communication systems. The feature rich device consists of a high linearity broadband active mixer, an integrated fractional-N phase-locked loop (PLL), a low phase noise multicore voltage controlled oscillator (VCO), and an IF digitally programmable variable gain amplifier (DGA). In addition, the **ADRF6620** also integrates a 4:1 RF switch, an on-chip tunable RF balun, programmable RF attenuator, and LDOs. This highly integrated device fits within a small 7 mm × 7 mm footprint.

This user guide describes the **ADRF6620-EVALZ** evaluation board, which provides all of the support circuitry required to operate the **ADRF6620** in its various configurations. The application software used to interface with the device is also described.

The **ADRF6620** data sheet, available at [www.analog.com](http://www.analog.com), which provides additional information, should be consulted when working with this evaluation board.

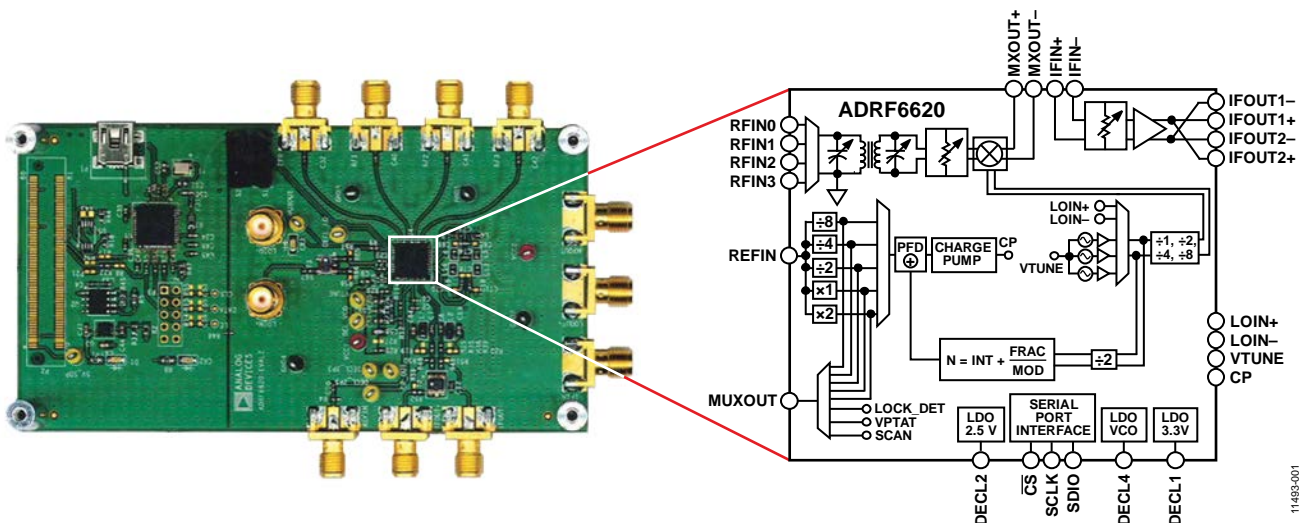


Figure 1. **ADRF6620** Evaluation Board

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**REVISION HISTORY**

7/13—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

### INTRODUCTION

The [ADRF6620](#) evaluation board provides all of the support circuitry required to operate the [ADRF6620](#) in its various modes and configurations. Figure 2 shows the typical bench setup used to evaluate the performance of the [ADRF6620](#).

### POWER SUPPLY

The [ADRF6620](#) evaluation board requires a single +5 V power supply. Connect the positive power terminal to one of the red test loops, either VCC1 or VCC2. The [ADRF6620](#) consumes less than 400 mA at power up with the default register settings.

### RF INPUTS

The high isolation 4:1 RF switch and on-chip tunable RF balun enables the [ADRF6620](#) to support four single-ended 50  $\Omega$  terminated RF inputs. The 4:1 RF switch can be controlled serially via the SPI port or parallel control using switches S1 and S2. The default configuration is parallel control using the switches. The operational frequency range of the RF inputs is from 700 MHz to 2700 MHz and the inputs should be ac-coupled.

### LO INPUT/OUTPUT

The [ADRF6620](#) offers two alternatives for generating the differential LO input signal: externally via a high frequency low phase noise LO signal or internally via the on-chip Fractional-N synthesizer. In either case, the differential LO signal can be routed off chip to the SMA connector labeled LO\_Output.

For internal LO configuration using the on-chip Fractional-N synthesizer, apply a low phase noise reference signal to the REFIN connector. The PLL reference input can support a wide frequency range since the division or multiplication blocks can be used to increase or decrease the reference frequency to the desired value before it is passed to the phase frequency detector (PFD). The integrated synthesizer enables continuous LO coverage from 350 MHz to 2850 MHz.

For optimum performance using an external LO source, the LO inputs, LOIN and LOIP, should be driven differentially. Unless an ac-coupled balun/transformer is used to generate the differential LO, the inputs must be ac-coupled. The input impedance of the differential LO signals is 50  $\Omega$ .

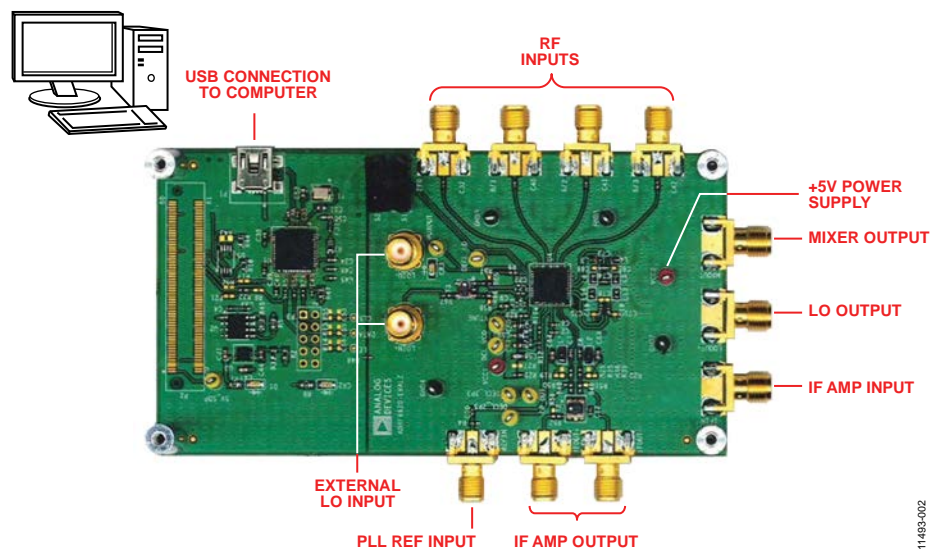


Figure 2. [ADRF6620](#) Typical Measurement Setup

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**MIXER OUTPUT**

The mixer outputs of the ADRF6620 are routed off chip for external biasing and optional low-pass filtering. The output pins, MXOP and MXON, require supply biasing to +5 V and the mixer’s differential output impedance is approximately 255 Ω. Refer to the ADRF6620 data sheet for the equivalent mixer output impedance and recommendations on the inter-stage filter design. The default configuration of the evaluation board has the mixer outputs ac-coupled to the IF VGA inputs.

The ADRF6620 evaluation board provides the option to monitor the front-end of the ADRF6620 independently from the variable gain IF amplifier by routing the differential mixer outputs to the SMA connectors. To achieve this configuration, remove L5 and L6 and populate C65 and C66 with 0.1 μF. The MXOP and MXON pins are routed to a 4:1 impedance

transformer from Mini-Circuits, TC4-1W+, to translate the 250 Ω output impedance of the mixer to 50 Ω (see Figure 3).

Attention needs to be paid to the IF frequency of the mixer output and the bandwidth of the transformer. The 1 dB bandwidth of the TC4-1W+ is limited to 100 MHz and the 3 dB band is 800 MHz. Alternatively, the 4:1 impedance transformer can be replaced with a 1:1 transformer, such as the TC1-1-13M+, and the L-resistor network (R33, R34, R32, and R10) can be used for impedance matching. The tradeoff to this approach is that the L-network is essentially a voltage divider that results in power loss.

If using a 1:1 transformer, populate R32 = R33 = 113 Ω and R34 = R10 = 28 Ω. This configuration results in a voltage loss of -19.6 dB.

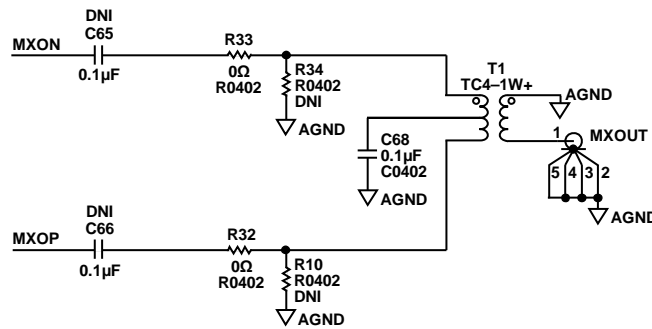


Figure 3. Mixer Output Schematic

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**IF VARIABLE GAIN AMPLIFIER**

The final IF amplifier stage amplifies the mixer outputs by 3 dB to 15 dB in 0.5 dB steps. The default configuration of the evaluation board has the mixer outputs routed to the IF amp inputs, however the evaluation board offers the flexibility of isolating the IF amp independently. To evaluate the amplifier independently of the mixer, remove C18 and C19 and populate C70 and C71 with 0.1  $\mu$ F.

By design, the IF amplifier has been optimized for OIP3 when the source and load impedance are terminated with 150  $\Omega$ . This matched condition can be achieved by using 3:1 impedance transformers at both the IF amplifier’s input and output (see Figure 4 and Figure 5). The 50  $\Omega$  source

impedance of the signal generator will reflect as 150  $\Omega$  at the IF amplifier’s input after the TCM3-1T+.

This same principle also holds true for the amplifier’s output where the spectrum analyzer’s impedance translates to 150  $\Omega$  after the transformer. If the IF amplifier is to be terminated with a source or load impedance different from what an impedance transformer can offer, a 1:1 transformer and matching network can be used.

If the load or the source resistance is not equal to 150  $\Omega$ , refer to the [ADRF6620](#) data sheet for equations which can be used to determine the resulting gain and input/output resistances.

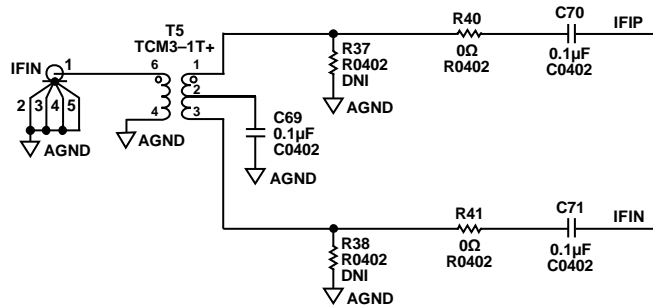


Figure 4. IF Amplifier Input Schematic

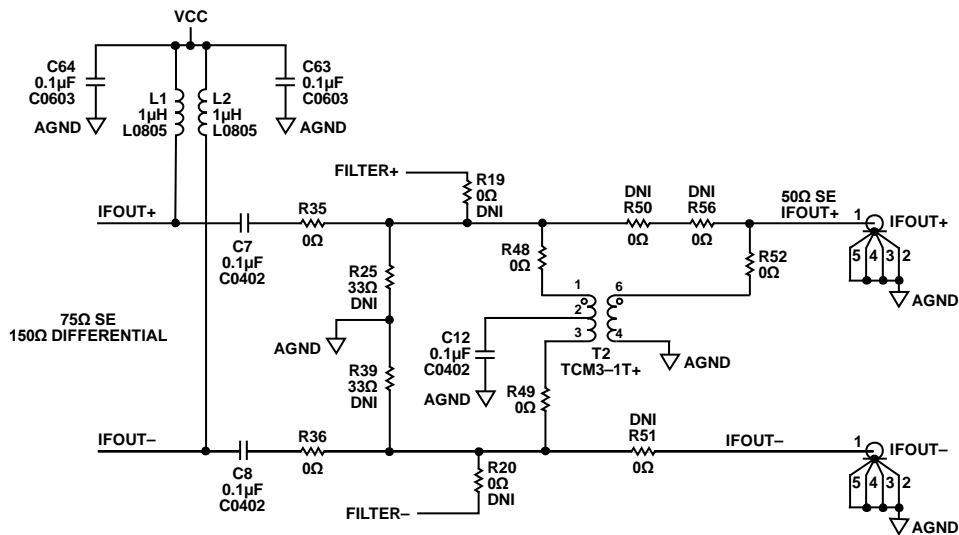


Figure 5. IF Amplifier Output Schematic

## EVALUATION BOARD CONTROL SOFTWARE

The [ADRF6620](#) evaluation board is configured with a USB-friendly interface to allow programmability of the [ADRF6620](#) registers.

### SOFTWARE REQUIREMENTS

These instructions describe how to install the [ADRF6620](#) control software, as well as the Cypress generic USB driver, onto a Windows XP, Vista, or Windows 7 computer running either a 32-bit or 64-bit operating system. Install the necessary software before plugging the USB cable to the computer.

1. In the extracted folder, **ADI\_RFG\_Drivers**, run the **ADI\_RFG\_Drivers.exe** file. Running this file allows the installation of the Cypress CyUSB.sys driver as a verified, signed driver.
2. Run the file **ADRF6620\_install.exe** from the extracted .zip file. An icon should appear on your desktop with the Analog Devices, Inc., logo, labeled [ADRF6620](#).
3. Install the USB driver once the installer is finished. Plug the RFG USB adapter into the PC using a USB cable.
4. In either Windows XP or Vista, right click on **My Computer** and select **Properties**. Next, in Vista or Windows 7, select the **Device Manager** option. In XP, select the hardware tab and then **Device Manager**.
5. In **Device Manager**, select the last category, **Universal Serial Bus Controllers**. There will be an entry with either a yellow flag (for unknown device) or **ADF4xxx USB Driver** (if you have installed the previous ADRF6x0x or Analog Devices Limerick PLL software). Right click on this device and select **update driver**. Browse to select the directory **C:\Program Files\ADRF6620\_customer\_software**.
6. Click **Next** to complete the driver installation successfully.

### ADRF6620 EVALUATION SOFTWARE

The [ADRF6620](#) evaluation software offers a block diagram view of how the registers affect the major functional blocks of the [ADRF6620](#). The main screen of the evaluation software is shown in Figure 6.

Before reading or writing to the registers, validate the USB connection by reading the USB indicators at the lower left corner of the software. The **DUT to GUI** button reads the register values from the device and updates the user interface. An automatic write to the chip is initiated every time a register value is changed from the user interface.

The PLL synthesizer blocks perform background calculations; the user need only specify the PLL reference and desired LO frequency and the software calculates and sets the INT, FRAC, and MOD values accordingly. The green boxes require user input while the yellow boxes are read only.

The Engineering tab, as shown in Figure 7, allows specific reads and writes to the individual registers. Decimal format is required when entering data to the address and data fields.

The screenshot displays the main control interface for the ADRF6620 chip. It features a central block diagram of the chip with various functional blocks and their interconnections. Key control panels include:

- RF Front-End:** Controls for RF0-3, BAL\_CIN, BAL\_COUT, and RFDSA.
- Mixer:** Controls for MIX\_BIAS (4), MIX\_RDAC (7), and MIX\_CDAC (15).
- PLL Reference:** PLL REF IN (MHz) set to 153.6, PLL REF DIVIDER (DIV4).
- Charge Pump:** Controls for CSCALE (500 uA), BLEED (up 93.75 u), ABLDLY (0 nsec), CPCTRL (PFD), and CLKEDGE (Div \, Ref \).
- VCO and LO:** VCO\_SEL (2.8 GHz - 4.1 GHz), VCO Freq (MHz) set to 4000, LO\_DIV\_A (DIV2), LO\_DRV\_LVL (-5.0 dBm).
- IF and Output:** IFIP, IFIN, IF\_ATTEN (0 dB), and output ports OIFON1, OIFOP1, OIFON2, OIFOP2.
- Control and Status:** REF\_MUX\_SEL, MUXOUT, Lock\_det, Vpstat, Scan, and a USB Connection indicator showing 'X2 USB device found, connected' and 'hex file successfully loaded'.
- Register Write Log:** A list of hexadecimal register addresses and values, with a 'Clear' button.
- Buttons:** 'Update GUI', 'Save Register File', 'Open Register File', and 'Software Reset'.

Red annotations highlight specific features:

- INPUT PLL REFERENCE:** Points to the PLL REF IN field.
- PFD FREQ AUTOMATICALLY CALCULATED:** Points to the PFD FREQ (MHz) field, which shows 38.4.
- VCO FREQ AUTOMATICALLY CALCULATED:** Points to the VCO Freq (MHz) field, which shows 4000.
- SYNTHESIZER VALUES AUTOMATICALLY CALCULATED:** Points to the N = INT + ERAC / MOD section, where INT is 52, FRAC is 128, and MOD is 1536.
- INPUT DESIRED LO FREQ:** Points to the LO Freq (MHz) field, which shows 2000.
- INCREMENT OR DECREMENT LO FREQ BY STEP SIZE:** Points to the INC and DEC buttons.

Figure 6. Main Screen of the ADRF6620 Control Software with Default Power-Up Settings

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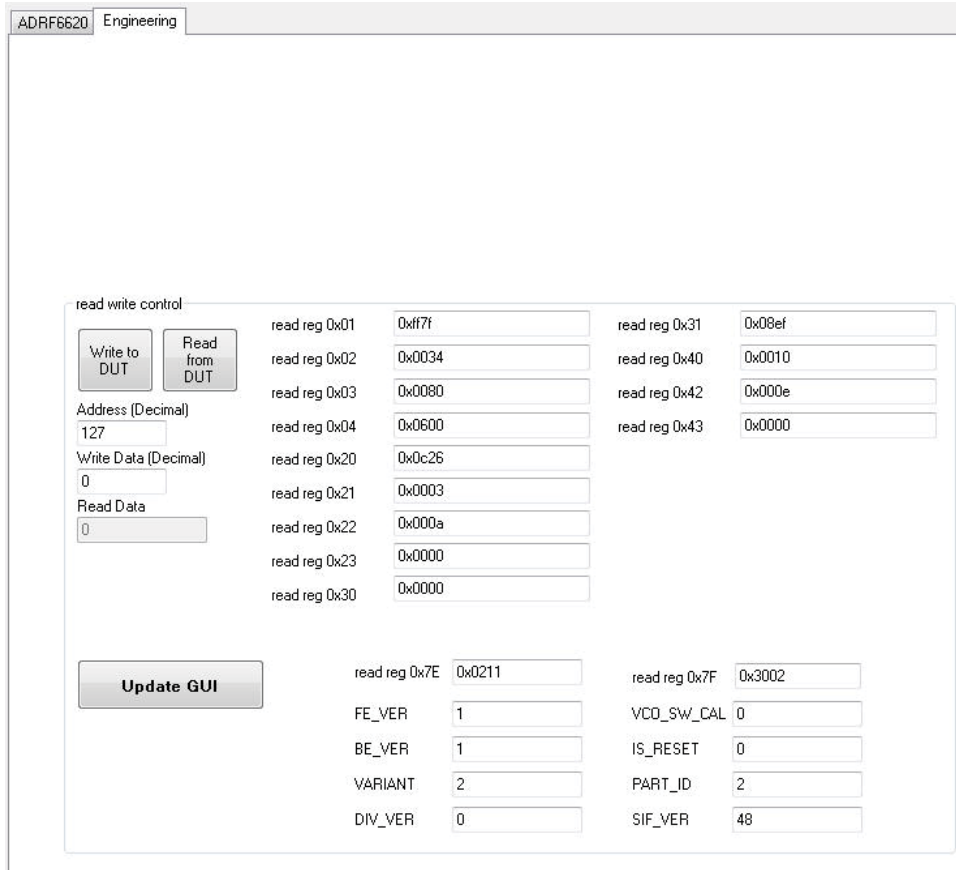


Figure 7. Engineering Tab of the ADRF6620 Control Software

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SCHEMATICS AND ARTWORK

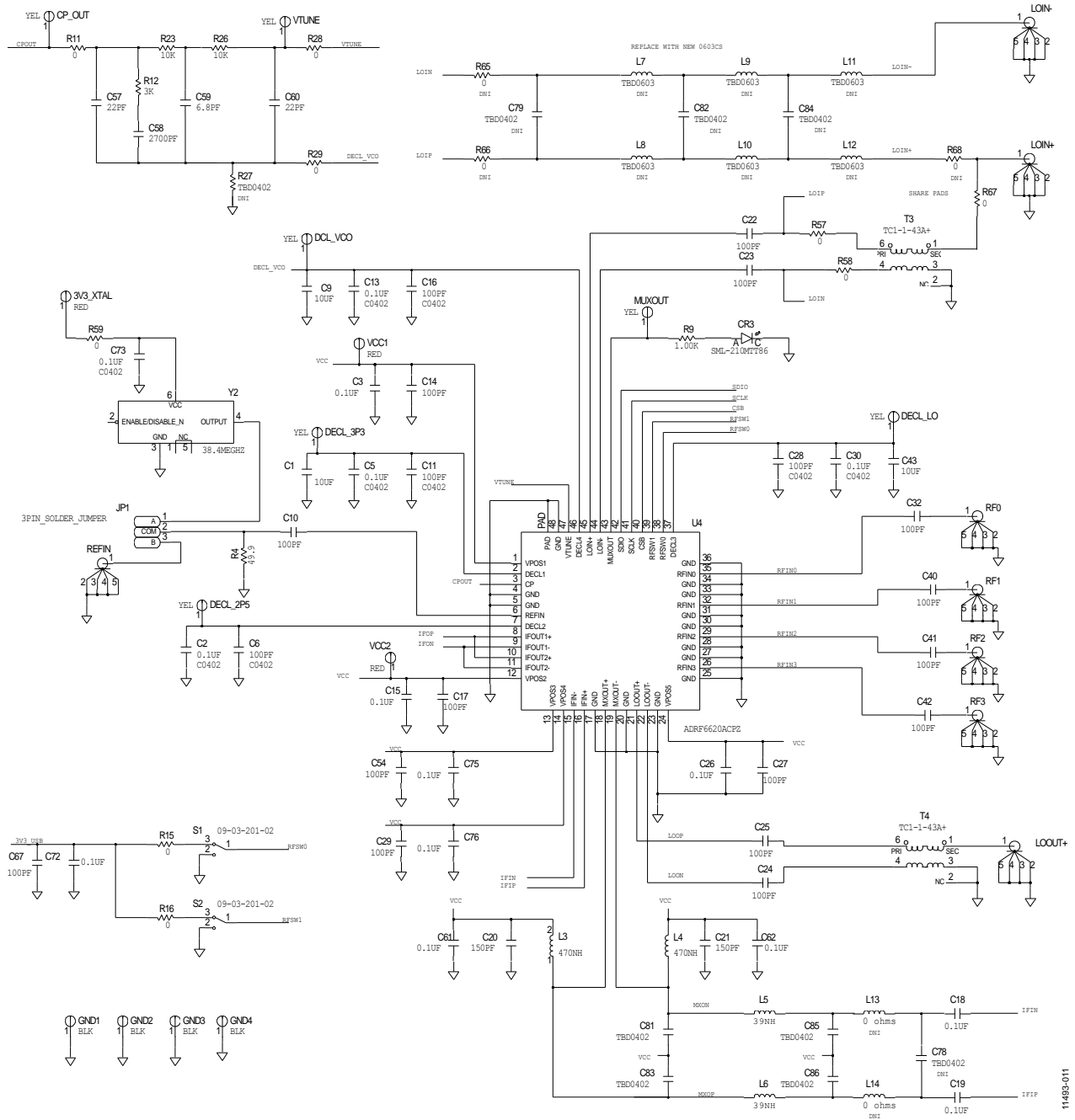
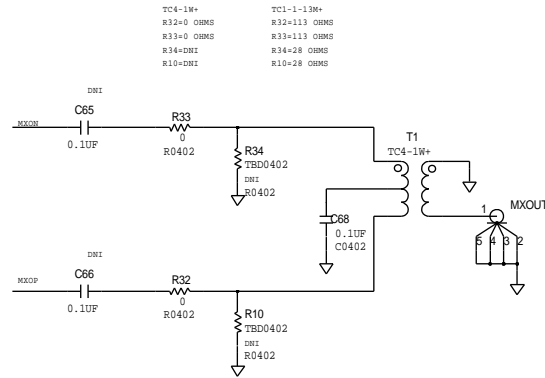
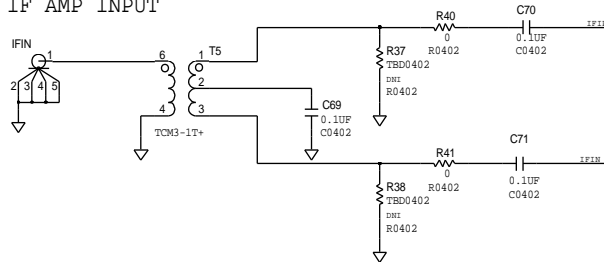


Figure 8. Schematic

MIXER OUTPUT



IF AMP INPUT



IF AMP OUTPUT

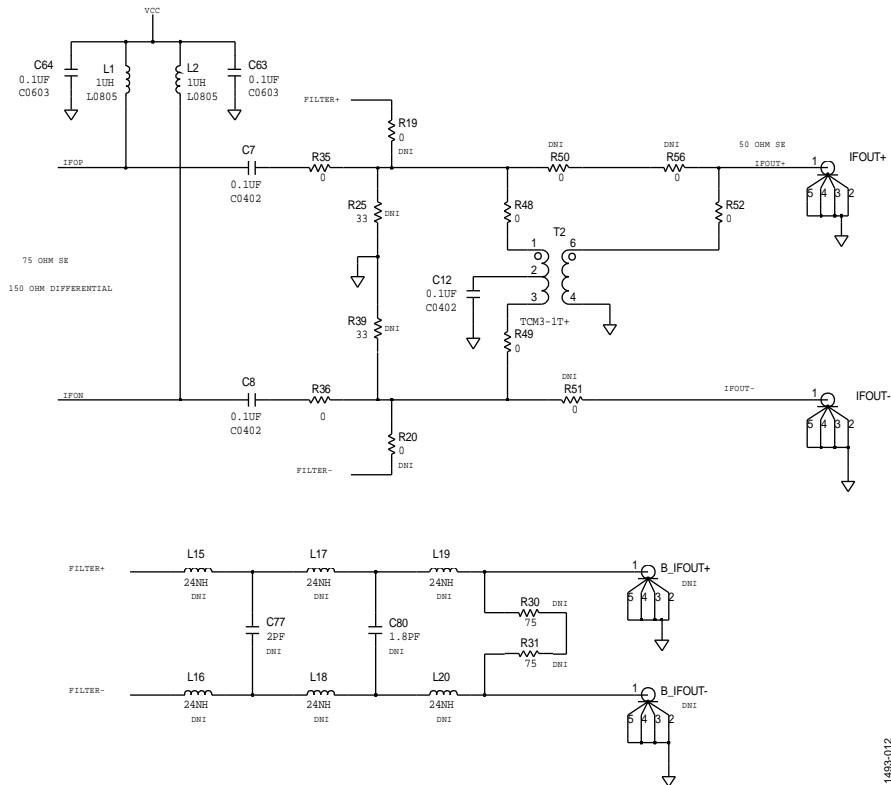


Figure 9. Mixer Output and IF Amplifier Input/Output Schematics

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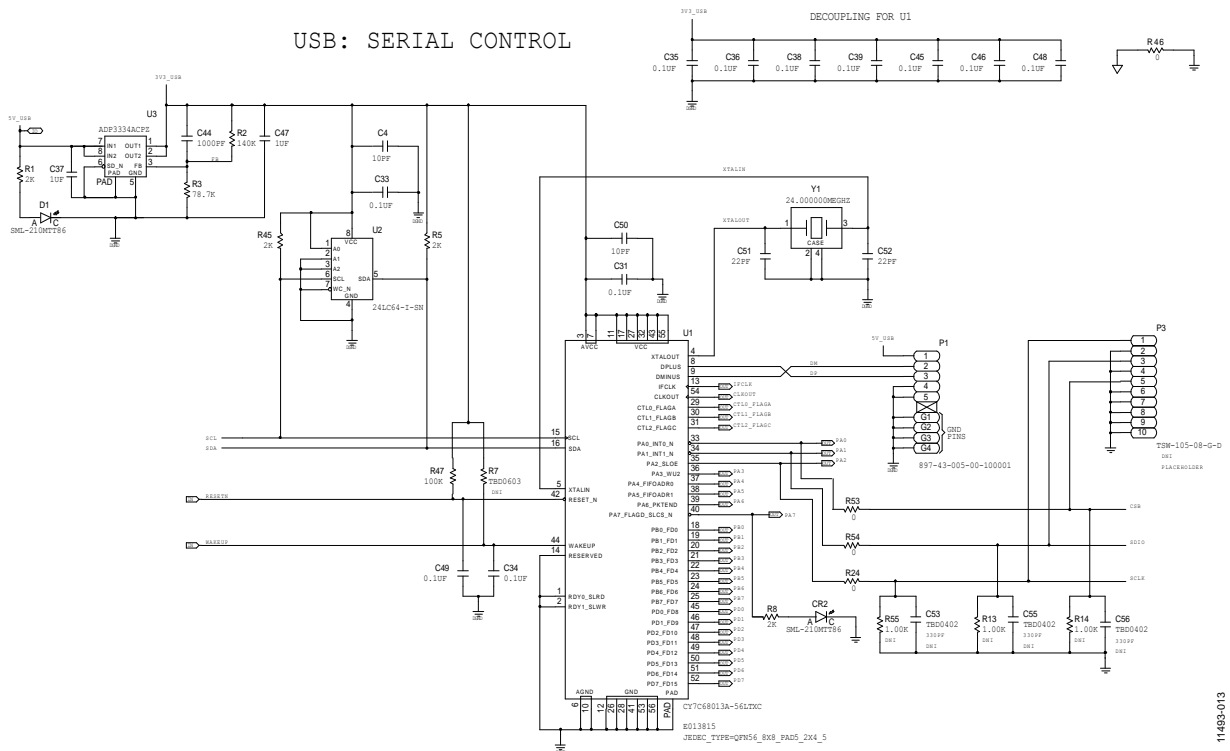


Figure 10. USB Serial Control

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L1 PRIMARY  
08-A03103-01  
REV D

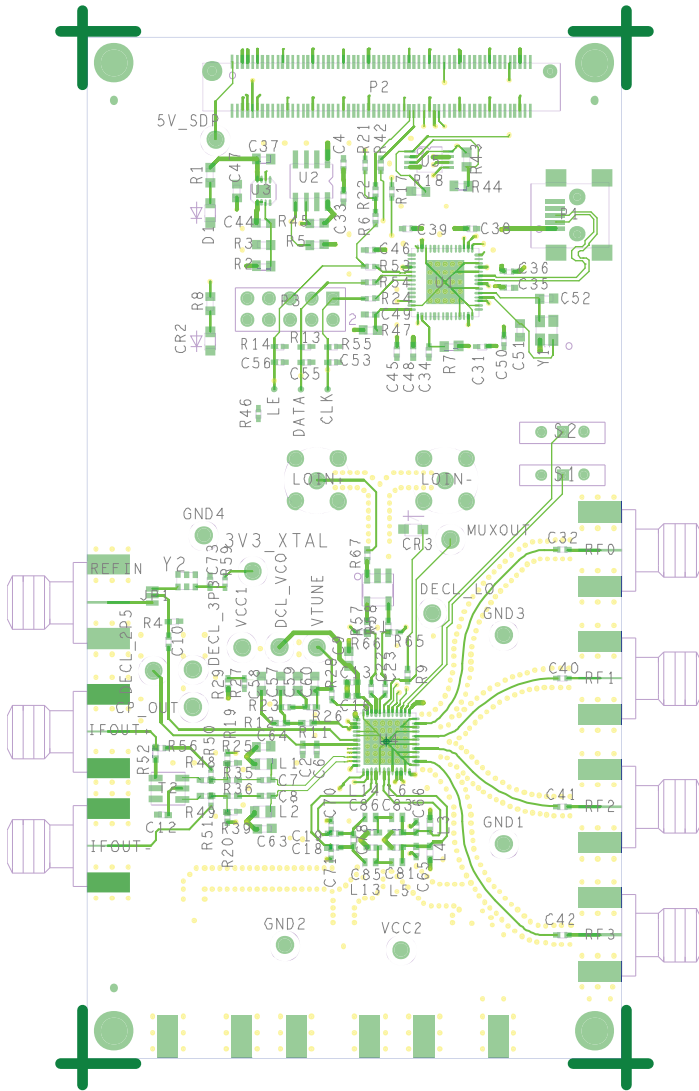


Figure 11. Primary Side Layout

L4 SECONDARY  
08-A03103-02  
REV D

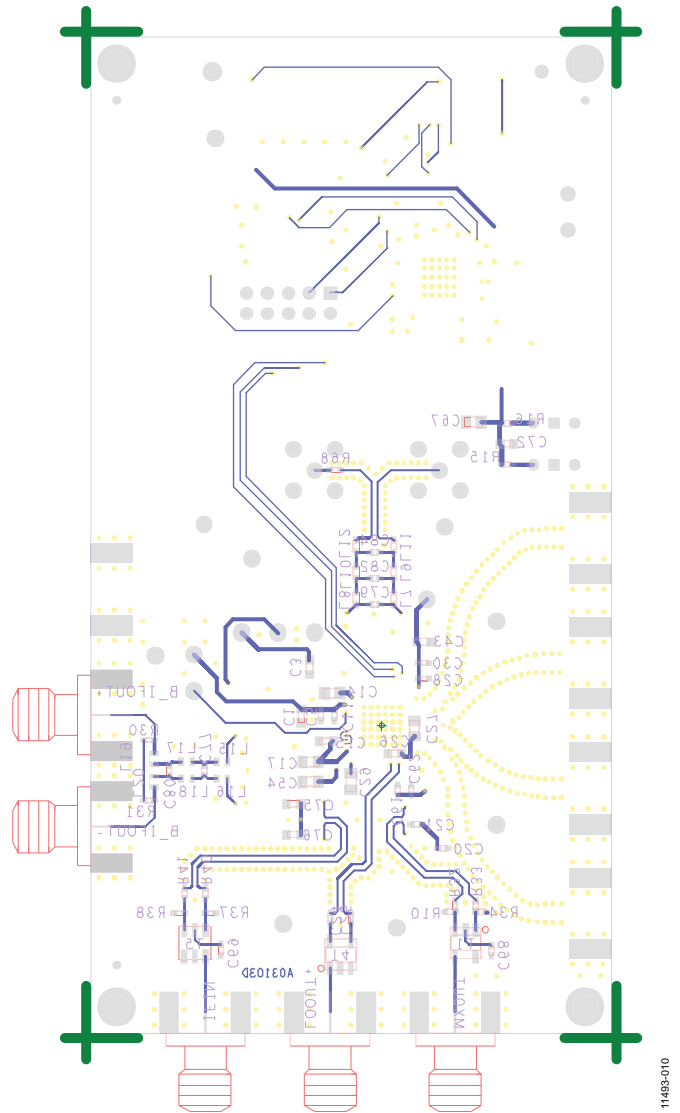


Figure 12. Secondary Side Layout

## BILL OF MATERIALS

Table 1.

Qty	Reference Designator	Description	Tolerance	Voltage	Manufacturer	Part Number
3	VCC1, VCC2, 3V3_XTAL	Conn-PCB test point, red			Components Corp	TP-104-01-02
8	VTUNE, 5V_SDP, CP_OUT, MUXOUT, DCL_VCO, DECL_LO, DECL_2P5, DECL_3P3	Conn-PCB test point, yellow			Components Corp	TP-104-01-04
3	C1, C9, C43	Cap cer, X5R 0603, 10 $\mu$ F	20	6.3 V	Murata	GRM188R60J106ME47D
13	C6, C10, C11, C16, C22 to C25, C28, C32, C40 to C42	Cap chip mono cer, COG 0402, 100 pF	5	50 V	Murata	GRM1555C1H101JD01D
27	C2, C5, C7, C8, C12, C13, C18, C19, C30, C31, C33 to C36, C38, C39, C45, C46, C48, C49, C61, C62, C68 to C71, C73	Cap cer, X7R 0402, 0.1 $\mu$ F	10	16 V	Murata	GRM155R71C104KA88D
6	C14, C17, C27, C29, C54, C67	Cap cer, NP0, 0805, 100 pF	5	100 V	AVX	08051A101JAT2A
6	C3, C15, C26, C72, C75, C76	Cap cer, X7R 0603, 0.1 $\mu$ F	10	50 V	AVX	06035C104KAT2A
2	C20, C21	Cap cer, COG 0402, 150 pF	5	50 V	Murata	GRM1555C1H151JA01D
2	C37, C47	Cap mono cer, X5R, 0603, 1 $\mu$ F	10	25 V	Murata	GRM188R61E105KA12D
2	C4, C50	Cap cer, multilayer NP0 0402, 10 pF	5	50 V	PHYCOMP (YAGEO)	CC0402JRNPO9BN100
1	C44	Cap cer, COG 0603, 1000 pF	5	100 V	TDK	C1608C0G2A102J
4	C51, C52, C57, C60	Cap cer, NP0, 0603, 22 pF	5	50 V	PHYCOMP (YAGEO)	CC0603JRNPO9BN220
1	C58	Cap cer, COG 0603, 2700 pF	5	50 V	Murata	GRM1885C1H272JA01D
1	C59	Cap cer, NP0, 0603, 6.8 pF	5	50 V	PHYCOMP (YAGEO)	2238 867 15688
2	C63, C64	Cap cer, CHIP X8R, 0603, 0.1 $\mu$ F	10	25 V	TDK	C1608X8R1E104K
2	C81, C83	Cap cer, 0402 COG, 1.6 pF	0.1 pF	50 V	Murata	GJM1555C1H1R6BB01B
2	C85, C86	Cap cer, COG SMD, 0402, 2 pF	$\pm$ 0.25 pF	50 V	Murata	GJM1555C1H2R0CB01D
3	D1, CR2, CR3	LED 570 NM WTR CLR, 0805, SMD (green)	N/A	2.2 V	Rohm	SML-210MTT86
4	GND1 to GND4	Conn-PCB test point, black			Components Corp	TP-104-01-00
10	RF0 to RF3, IFIN, MXOUT, REFIN, IFOUT+, IFOUT-, LOOUT+	Conn-PCB coax SMA end launch			Johnson	142-0701-851
2	L1, L2	Inductor SM, 0805, 1 $\mu$ H	5		Coilcraft	0805LS-102XJLB
2	L3, L4	Inductor SM, 0603, 470 nH	5		Coilcraft	0603LS-471XJLC
2	L5, L6	Inductor SM, 7144, 39 nH	5		Coilcraft	0603CS-39NXJLU
2	LOIN+, LOIN-	Conn-PCB coax SMA ST			Johnson	142-0701-201
1	P1	Conn-PCB recept mini-USB Type B SMT			Mill-Max	897-43-005-00-100001
1	P2	Conn-PCB vert type rcpt SMD			HRS	FX8-120S-SV(21)
4	R1, R5, R8, R45	Res, film SMD 0603, 2 K, 1/10 W	1		PHYCOMP (YAGEO)	9C06031A2001FKHFT
23	R11, R15, R16, R22, R24, R28, R29, R32, R33, R35, R36, R40, R41, R46, R48, R49, R52 to R54, R57 to R59, R67, L13, L14	Res, film SMD 0402, 0, 1/16 W	5		Panasonic	ERJ-2GE0R00X
1	R12	Res, thick film chip, 0402, 3 K, 1/16 W	5		Panasonic	ERJ-2GEJ302X
3	R18, R44, R47	Res, prec thick film chip, 0603, 100 K, 1/10 W	1	50 V	Panasonic	ERJ-3EKF1003V
1	R2	Res, prec thick film chip, 0603, 140 K, 1/10 W	1	50 V	Panasonic	ERJ-3EKF1403V
2	R23, R26	Res, prec thick film chip, 0402, 10 K, 1/16 W	1		Panasonic	ERJ-2RKF1002X
1	R3	Res, prec thick film chip, 0603, 78.7 K, 1/10 W	1	50 V	Panasonic	ERJ-3EKF7872V
1	R4	Res, prec thick film chip, 0402, 49.9 K, 1/16 W	1		Panasonic	ERJ-2RKF49R9X

Qty	Reference Designator	Description	Tolerance	Voltage	Manufacturer	Part Number
1	R9	Res, prec thick film chip, 0402, 100 K, 1/10 W	1		Panasonic	ERJ-2RKF1001X
2	S1, S2	SW PCB mount slide			SECMA	09-03-201-02
1	T1	XFMR RF, 0.25 W			Mini circuits	TC4-1W+
2	T2, T5	XFMR RF, 0.25 W			Mini circuits	TCM3-1T+
2	T3, T4	XFMR RF, SMT			Mini-circuits	TC1-1-43A+
1	U1	IC HS USB peripheral		3 V to 3.6 V	Cypress Semiconductor	CY7C68013A-56LTXC
1	U2	IC 64 K bit EEPROM			Microchip	24LC64-I-SN
1	U3	IC-ADI high acc. low IQ adj low drop reg			Analog Devices	<a href="#">ADP3334ACPZ</a>
1	U4	IC Rx mixer, fractional-N PLL and VCO			Analog Devices	<a href="#">ADRF6620ACPZ</a>
1	U5	IC 32 K bit serial EEPROM			Microchip	24LC32A-I/MS
1	Y1	IC crystal SMD			NDK	NX3225SA-24.000000MHZ
1	Y2	IC crystal osc, 38.4 MHz		3.3 V		

## NOTES

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Legal Terms and Conditions**

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