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Evaluation Board for SSM4321 Class-D Audio Amplifier with Voltage and Current Sense

FEATURES

Allows testing of SSM4321 features
Jumpers provided for I/V data slot assignment

EVALUATION KIT CONTENTS

EVAL-SSM4321Z evaluation board

ADDITIONAL EQUIPMENT NEEDED

External power supplies for IOVDD and PVDD
Audio signal source
Resistive loads or speakers > 4 Ω
External processor for decoding I/V data

ONLINE RESOURCES

SSM4321 data sheet
EVAL-SSM4321Z user guide

GENERAL DESCRIPTION

The SSM4321 is a fully integrated, high efficiency, Class-D audio amplifier with digitized output of output voltage, output current, and PVDD supply.

It is designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a 2.5 V to 5.5 V supply for the amplifier and a 1.42 V to 3.6 V supply for IO. It is capable of delivering 2.2 W of continuous output power with less than 1% THD + N driving an 4 Ω load from a 5.0 V supply with a 0.1Ω V/I sense resistor.

This user guide describes how to configure and use the SSM4321 evaluation board. It is recommended that this user guide be read in conjunction with the SSM4321 data sheet, which provides specifications, internal block diagrams, and application guidance for the amplifier IC.

EVALUATION BOARD OVERVIEW

The SSM4321 evaluation board carries a complete application circuit for driving a loudspeaker and obtaining voltage and current data from the output. Figure 1 shows the top view of the evaluation board and Figure 2 shows the bottom view.

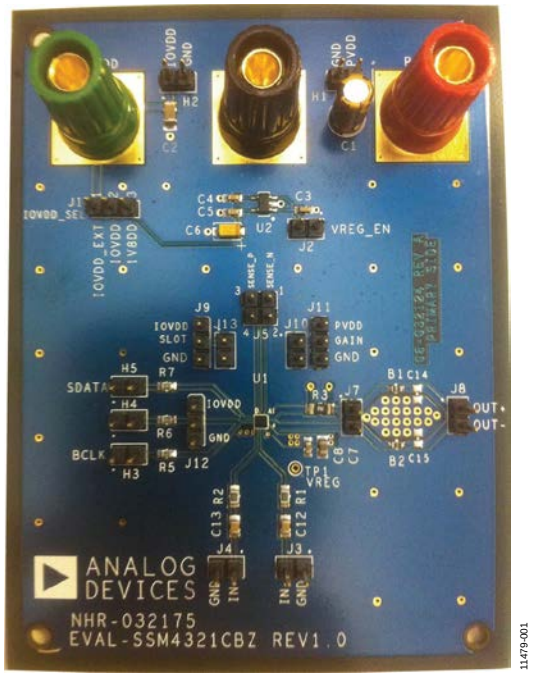

Figure 1. SSM4321 Evaluation Board Top View

Figure 2. SSM4321 Evaluation Board Bottom View

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REVISION HISTORY

4/13—Revision 0: Initial Version

SSM4321 DEVICE DESCRIPTION

The SSM4321 includes circuitry to sense output current, output voltage, and the PVDD supply voltage. Current sense is performed using an external sense resistor that is connected between an output pin and the load. Output current and voltage are sent to an ADC with 16-bit resolution and PVDD is sent to an ADC with 8-bit resolution. The outputs of these ADCs are available on the TDM or I^2S output serial port. The SLOT pin is used to determine which of four possible output slots is used on the TDM interface. A stereo I^2S interface can be selected by swapping the pin connections for BCLK and FSYNC. Alternatively, a direct PDM bit stream of voltage and current data can be selected via the SLOT pin.

Spread spectrum pulse density modulation (PDM) is used to provide lower EMI-radiated emissions compared with other Class-D architectures. The inherent randomized nature of spread spectrum PDM eliminates clock intermodulation (beating effect) of several amplifiers in close proximity.

The SSM4321 includes an optional modulation select pin that enables a low EMI mode, which significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz. With this option selected, the SSM4321 can pass FCC Class B radiated emissions testing with a 50 cm unshielded speaker cable without any external filtering.

The device also includes a flexible gain select pin that only requires one series resistor to select among 0 dB, 3 dB, 6 dB, 9 dB, or 12 dB. The benefit of this is to improve gain matching between multiple SSM4321 devices within a single application as compared to using external resistors to set gain.

SETTING UP THE EVALUATION BOARD

INPUT CONFIGURATION

A pair of 2-pin headers (J3 and J4) feeds the audio signal into the board (see Figure 1). If the input audio signal is differential, three pins of J3 and J4 are used: IN+, IN−, and GND. For a single-ended audio input, only J3 is used (IN+ and GND) and IN− is connected to ground.

SHUTDOWN MODE

The SSM4321 amplifier is enabled whenever a valid BCLK signal is connected to the chip. Any clock frequency between 512 kHz and 6.144 MHz is acceptable. When no clock is received, the amplifier enters shutdown mode and draws minimal current (< 1 μA) from the supplies.

GAIN CONFIGURATION

Two headers, J10 and J11, control the SSM4321 analog gain. By placing a jumper across two pins of J11, the amplifier's GAIN pin can be connected to GND or VDD. Three jumper settings are used: between the center pin and the top pin (IOVDD), between the center pin and the bottom pin (GND), and no jumper (open).

Placing a jumper on J10 shorts across the 47 kΩ resistor (R4) between the GAIN pin and J11. If the jumper is left open, R4 remains in the circuit.

Gain settings between 0 dB and 12 dB are available; see Table 1 for configuration details.

Table 1. Gain Configuration

Gain	J10	J11	Configuration
0 dB	Short	GND	Tie to GND
3 dB	Open	Open	Open
6 dB	Short	IOVDD	Tie to IOVDD
9 dB	Open	GND	Tie through 47 kΩ to GND
12 dB	Open	IOVDD	Tie through 47 kΩ to IOVDD

SLOT CONFIGURATION

Two headers, J13 and J9, control additional options, such as the TDM slot or I²S configuration options. By placing a jumper across two pins of J9, the amplifier's SLOT pin can be connected to GND or VDD. Three jumper settings are used: between the center pin and the left pin (HI), between the center pin and the right pin (LO), and no jumper (open).

Placing a jumper on J13 shorts across the 47 kΩ resistor (R8) between the SLOT pin and J9. If the jumper is left open, R8 remains in the circuit.

See the Digital Interface Configuration section for details of the SLOT pin options, depending on which digital interface is in use.

OUTPUT CONFIGURATION

The output connector, H4, is located on the right side of the board (see Figure 1). H4 can drive a loudspeaker whose impedance should be no less than 3 Ω.

Because the SSM4321 does not typically require any external LC output filters due to a low noise modulation scheme, no output filter is installed on the evaluation board. In this case, zero-ohm links are used in place of B1 and B2, and the capacitor pads are left unpopulated.

If the speaker length exceeds 50 cm, place Ferrite Bead B1 and Ferrite Bead B2 in the output paths, and use Capacitors C6 and C7 to couple the output terminals to ground, as shown in the schematic in Figure 6. Some recommended ferrite beads are listed in Table 9. Some users may want to use inductors for applications with specific EMI vs. audio performance constraints; see Table 10 for recommendations.

For optimal THD and SNR performance as specified in the SSM4321 data sheet, remove the entire EMI filter, short across the ferrite bead terminals, and open the capacitor terminals.

CURRENT SENSE JUMPERS

For the amplifier to operate properly, the SENSE+ and SENSE− pins must be connected to the proper sides of the current sense resistor. Jumpers between Pin 1 to Pin 2 and Pin 3 to Pin 4 of J5 must be in place; otherwise, incorrect behavior will result.

POWER SUPPLY CONFIGURATION

Two power supplies are required for the SSM4321 to operate: PVDD and IOVDD. PVDD is used for the analog input stage, modulator, and output stage. IOVDD is used for the digital logic and serial audio interface. These supplies may be connected either to the banana jacks at the top of the board or to H1 and H2, a pair of 2-pin 0.100" male headers.

Be sure to connect the dc power supplies with correct polarity and voltage. PVDD may be connected to a supply voltage in the acceptable range, between 2.5 V and 5.5 V. IOVDD must be in the range from 1.42 V to 3.6 V. Reverse polarity or overvoltage may damage the board permanently.

An on-board 1.8 V low-dropout regulator is available to provide a stable IOVDD supply without requiring multiple external power sources. To use this supply, insert a jumper into J2 (VREG_EN) and connect the center pin of J1 to 1V8DD. Alternatively, by removing these jumpers and connecting the center pin of J1 to IOVDD_EXT, an external IOVDD supply can be used.

DIGITAL INTERFACE CONFIGURATION

TDM MODE

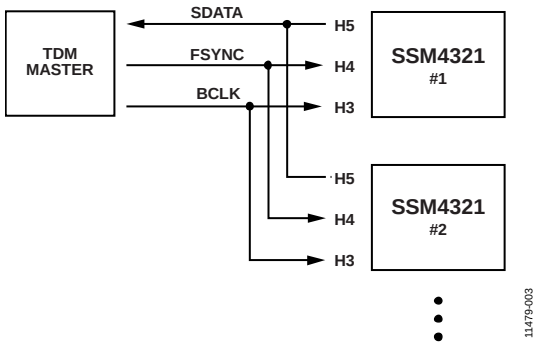

Figure 3. TDM Configuration

In TDM mode, the data stream is divided into 16-bit slots in groups of four. The start of Slot 1 is indicated by the rising edge of a one-clock-wide pulse on the FSYNC pin.

Any multiple of four slots—4, 8, 12, or 16—can be used. Each chip returns to a high-impedance mode when it is not actively driving the bus. Each SSM4321 device takes control of four conse-cutive slots, as shown in Table 2.

Table 2. TDM Slot Data Configuration

Device	V Data	I Data	PVDD Data	Hi-Z
1	Slot 1	Slot 2	Slot 3	Slot 4
2	Slot 5	Slot 6	Slot 7	Slot 8
3	Slot 9	Slot 10	Slot 11	Slot 12
4	Slot 13	Slot 14	Slot 15	Slot 16

The slots to be driven by each IC are chosen by a five-level jumper setting on the SLOT pin using J9 and J13. Each SSM4321 on the TDM bus must have a unique setting.

Table 3. SLOT Pin Configuration, TDM Mode

Slots Driven	J13	J9	Configuration
1 to 4	Short	IOVDD	Tie to IOVDD
5 to 8	Open	Open	Open
9 to 12	Short	GND	Tie to GND
13 to 16	Open	IOVDD	Tie through 47 kΩ to IOVDD
[PDM Output]	Open	GND	Tie through 47 kΩ to GND

I²S MODE

Figure 4. TDM Configuration

In I²S mode, the bit clock and LRCLK signals are reversed from the pin names. In other words, the BCLK signal is connected to the center (unlabeled) header H4, and LRCLK is connected to the BCLK header H3.

Both I²S and left-justified interface styles are available. Additionally, an 8-bit measurement of the PVDD rail can be appended to the 16-bit output voltage data. These options are chosen by a five-level jumper setting on the SLOT pin using J9 and J13.

A lower-power I²S mode is also available. In this mode, only a subset of sample rates are valid (f_S = 32 kHz to 48 kHz), and BCLK may run at 32× f_S instead of the usual 64× f_S. In all other modes, valid sample rates range from f_S = 16 kHz to 48 kHz, and BCLK must run at 64 × f_S.

Table 4. SLOT Pin Configuration, I²S Mode

Data Output	Interface Style	J13	J9
V and I Only	I²S	Short	IOVDD
V and I Only	Left justified	Open	Open
8-Bit PVDD Appended to V	I²S	Short	IOVDD
8-Bit PVDD Appended to V	Left justified	Open	IOVDD
V and I Only	I²S, low power mode (f_S = 32 kHz to 48 kHz only)	Open	GND

PDM MODE

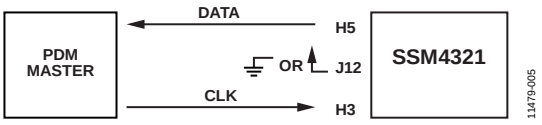

Figure 5. TDM Configuration

For PDM mode to be enabled, the SLOT pin must be tied through a 47 kΩ resistor to GND. This is done by removing the jumper from J13 and tying the center pin of J9 to GND. In addition, a 2 MHz to 6.144 MHz clock must be present on the BCLK pin.

Table 5. SLOT Pin Configuration, PDM Mode

Interface Type	J13	J9	Configuration
PDM Output	Open	GND	Tie through 47 kΩ to GND

PDM data is sent on both the rising and falling edge of the clock, so two data streams can be sampled using the PDM interface. The choice of V data or PVDD data for the falling edge is made by connecting the FSYNC pin to either GND or IOVDD. J12 is provided for this purpose; it should be left empty in all other modes.

Table 6. FSYNC Pin Configuration, PDM Mode

Output Data	FSYNC pin (J12)
I on Rising Edge, V on Falling Edge	Tie to IOVDD
I on Rising Edge, PVDD on Falling Edge	Tie to GND

PASSIVE COMPONENT SELECTION

SENSE RESISTOR SELECTION

The current-sense ADC is designed such that the full-scale output corresponds to ±150 mV across the current-sense resistor. The current-sense resistor value should therefore be calculated such that the worst-case peak current through the sense resistor will not cause a voltage drop larger than 150 mV. Table 7 provides a collection of sense resistor values for typical load impedances, and Table 8 describes some recommended components.

Any change in the sense resistor value directly affects the measured current, so a careful understanding of the sources of uncertainty and/or error in the current measurement chain is necessary to obtain the best performance.

For example, one significant consideration is the effect of changes in temperature caused by ambient temperature shifts and resistor self-heating. To minimize the change in sense resistor value, use a precision resistor with a small temperature coefficient. In addition, larger package sizes dissipate heat more efficiently, causing a smaller temperature increase and therefore a smaller resistance shift.

Table 7. Sense Resistor for Typical Loads, PVDD = 5 V

Load Impedance	Peak Current	Sense Resistor
8 Ω	750 mA	200 mΩ
4 Ω	1.5 A	100 mΩ
3 Ω	2 A	75 mΩ

INPUT GAIN RESISTORS

If the desired gain must be adjusted beyond the available gain settings (see the Gain Configuration section), a series resistor can be placed in the input signal path. This creates a voltage divider with the 80 kΩ input resistance on each input pin, allowing an arbitrary reduction of the input signal. Note that input signal attenuation directly reduces SNR performance; therefore, large values compared to the built-in input resistance should be avoided. These components are populated with 0 Ω values on the evaluation board.

INPUT COUPLING CAPACITORS

The input coupling capacitors, C1 and C2, should be large enough to couple the low frequency signal components in the incoming signal, but small enough to reject unnecessary, extremely low frequency signals. For music signals, the cutoff frequency is typically between 20 Hz and 30 Hz. The value of the input capacitor is calculated by

$$C = 1/(2\pi R_{IN} f_c)$$

where:
R_{IN} = 80 kΩ + (R1 or R2).
f_c is the desired cutoff frequency.

OUTPUT FERRITE BEADS

The output beads, B1 and B2, are necessary components for filtering out the EMI caused at the switching output nodes when the length of the speaker wire is greater than 10 cm. The penalty for using ferrite beads for EMI filtering is slightly worse noise and distortion performance at the system level due to the nonlinearity of the beads.

Ensure that these beads have enough current conducting capability while providing sufficient EMI attenuation. The current rating needed for an 8 Ω load is approximately 420 mA, and impedance at 100 MHz should be ≥120 Ω. In addition, the lower the dc resistance (DCR) of these beads, the better for minimizing their power consumption. Table 9 describes the recommended beads.

OUTPUT SHUNTING CAPACITORS

There are two output-shunting capacitors, C6 and C7, which work with the ferrite beads, B1 and B2. Use small size (0603 or 0402), multilayer ceramic capacitors made of X7R or C0G (NP0) materials. Note that the capacitors can be used in pairs: a capacitor with small capacitance (up to 100 pF) plus a capacitor with a larger capacitance (less than 1 nF). This configuration provides thorough EMI reduction for the entire frequency spectrum. If the bill of materials must be minimized, a single capacitor of approximately 470 pF can be used with acceptable performance in many cases.

OUTPUT INDUCTORS

If inductors are preferred for EMI filtering at the output nodes, choose components with an inductance of less than 2.2 µH. The higher the inductance, the lower the EMI is at the output; however, cost and power consumption are higher. Using 0.47 µH to 2.2 µH inductors is recommended, and the current rating (and saturation current) should exceed 600 mA for an 8 Ω load. Table 10 shows the recommended inductors.

Table 8. Recommended Sense Resistors

Part No.	Manufacturer	R (mΩ)	Tolerance	Tempco (ppm/°C)	Power Rating (W)	Size (mm)
WSL1206R2000FEA	Vishay-Dale	200	1%	75	0.25	3.2 × 1.6 × 0.6
WSL1206R1000FEA	Vishay-Dale	100	1%	75	0.25	3.2 × 1.6 × 0.6
WSL0805R2000FEA	Vishay-Dale	200	1%	75	0.125	2.0 × 1.2 × 0.3
WSL0805R1000FEA	Vishay-Dale	100	1%	75	0.125	2.0 × 1.2 × 0.3
ERJ-L08UF75MV	Panasonic ECG	75	1%	100	0.333	3.2 × 1.6 × 0.6

Table 9. Recommended Output Beads

Part No.	Manufacturer	Z (Ω at 100 kHz)	I_{MAX} (mA)	DCR (Ω)	Size (mm)
BLM18PG121SN1D	Murata	120	2000	0.05	1.6 × 0.8 × 0.8
MPZ1608S101A	TDK	100	3000	0.03	1.6 × 0.8 × 0.8
MPZ1608S221A	TDK	220	2000	0.05	1.6 × 0.8 × 0.8
BLM18EG221SN1D	Murata	220	2000	0.05	1.6 × 0.8 × 0.8

Table 10. Recommended Output Inductors

Part No.	Manufacturer	L (µH)	I_{MAX} (mA)	DCR (Ω)	Size (mm)
LQM31PNR47M00	Murata	0.47	1400	0.07	3.2 × 1.6 × 0.85
LQM31PN1R0M00	Murata	1.0	1200	0.12	3.2 × 1.6 × 0.85
LQM21PNR47MC0	Murata	0.47	1100	0.12	2.0 × 1.25 × 0.5
LQM21PN1R0MC0	Murata	1.0	800	0.19	2.0 × 1.25 × 0.5
LQH32CN2R2M53	Murata	2.2	790	0.13	3.2 × 2.5 × 1.55

EVALUATION BOARD SCHEMATIC AND ARTWORK

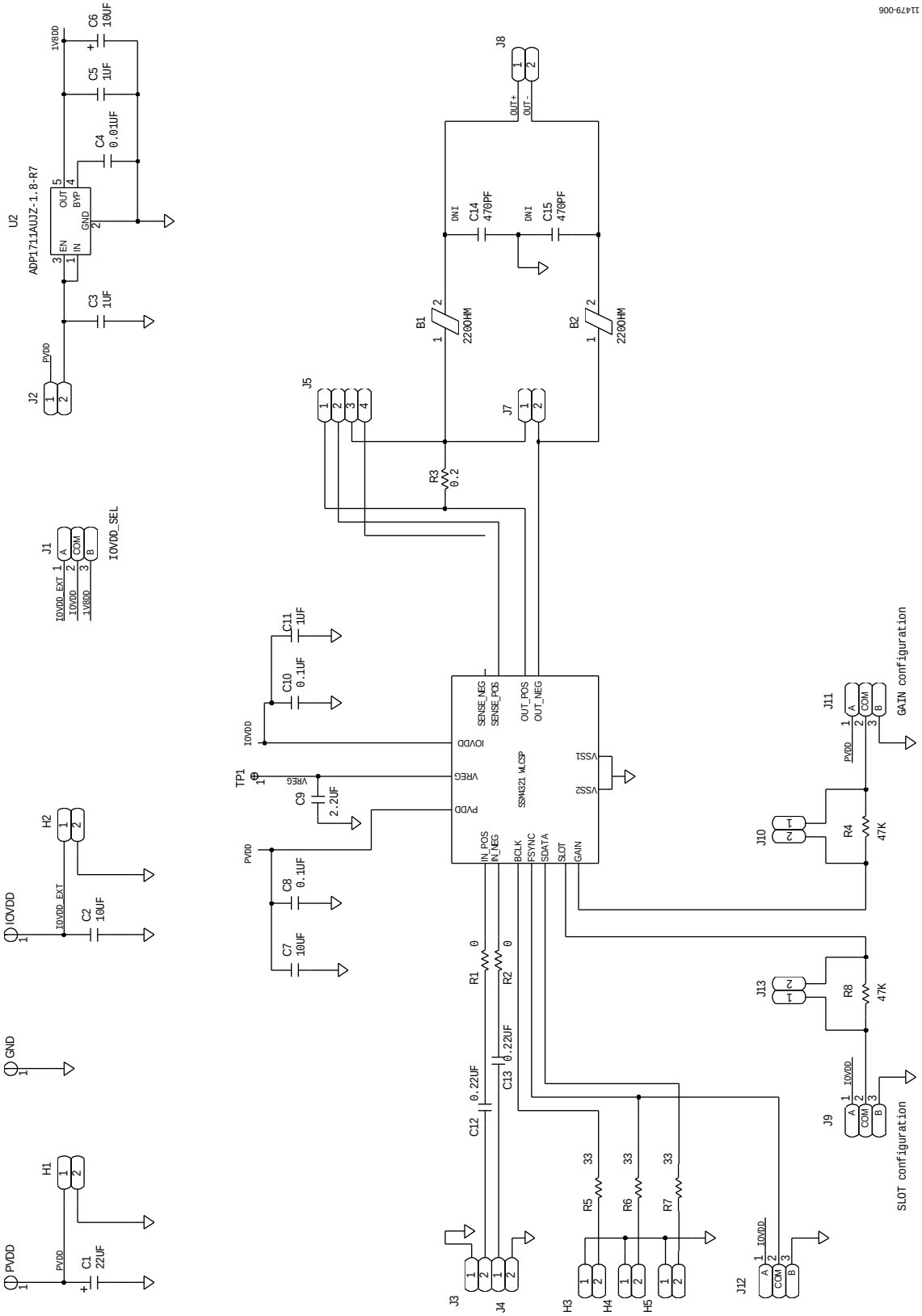

Figure 6. Schematic of the SSM4321 Evaluation Board

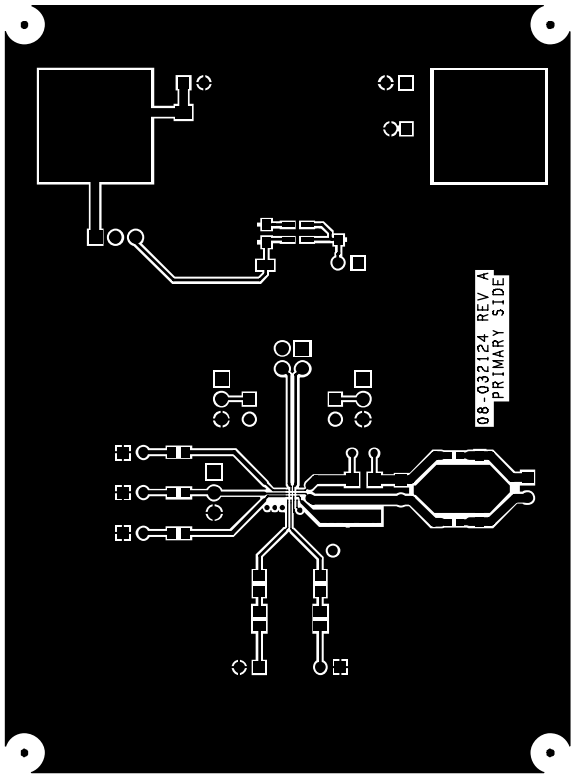

Figure 7. Top Layer Copper

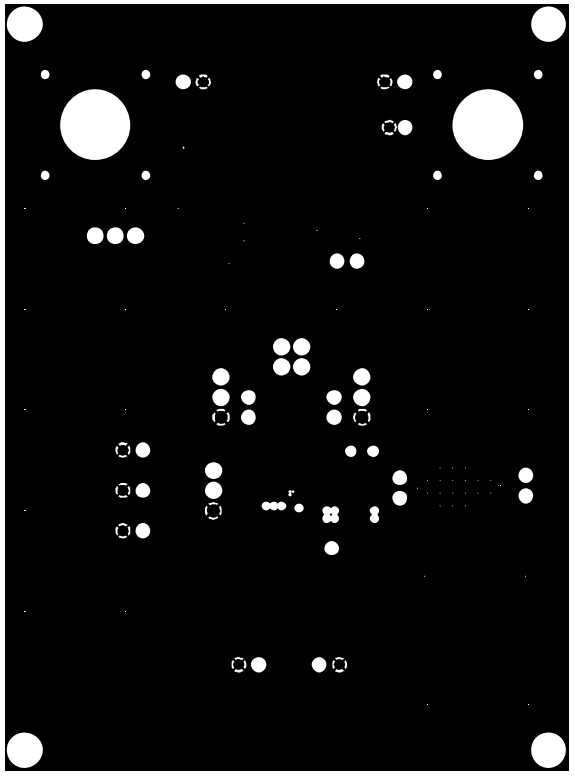

Figure 8. Second Layer Copper—GND Plane

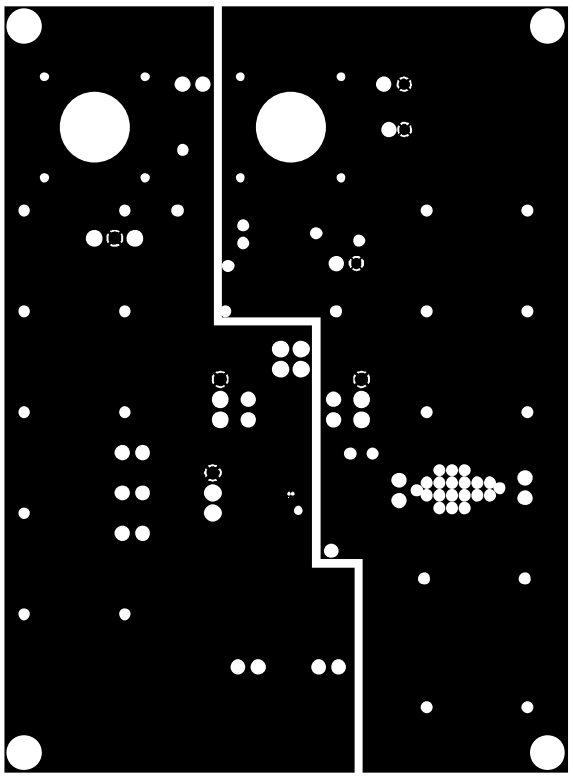

Figure 9. Third Layer Copper—VDD Plane

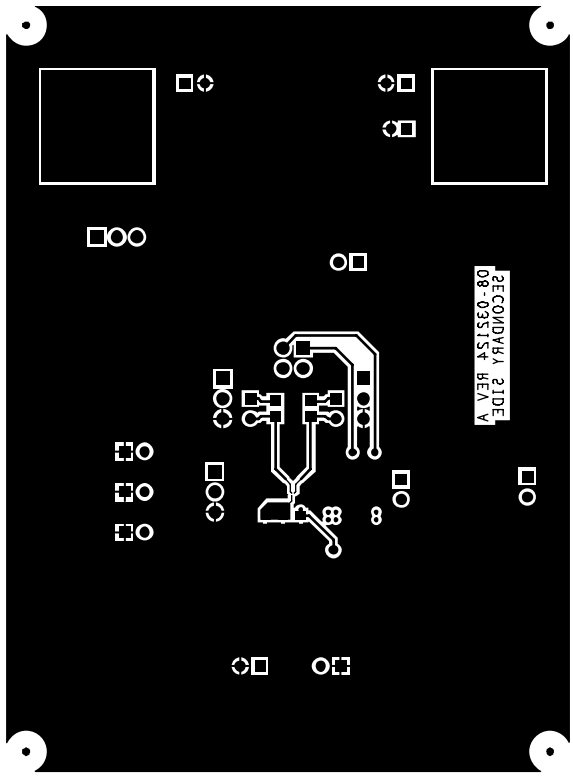

Figure 10. Bottom Layer Copper

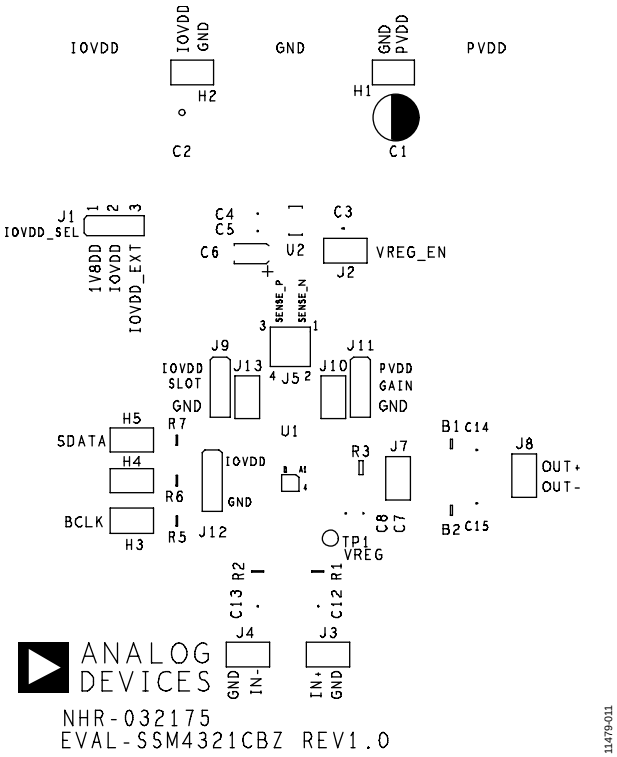

Figure 11. Top Silkscreen

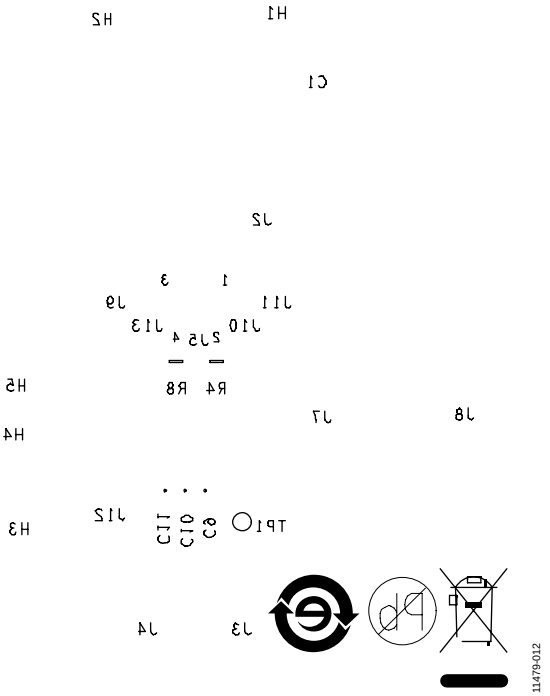

Figure 12. Bottom Silkscreen

ORDERING INFORMATION

BILL OF MATERIALS

Table 11.

Qty	Reference Designator	Description	Supplier/Part No.
1	U1	IC, SSM4321	Analog Devices/SSM4321CBZ
2	C1, C2	Capacitor, 22 nF, 25 V, 10%, X7R, 0805	Panasonic/ECJ-2YB1E224K
1	C3	Capacitor, ceramic 0.1 µF, 50 V, Y5V, 0603	Panasonic/ECJ-1VF1H104Z
1	C4	Capacitor, ceramic 10 µF, 10 V, X5R, 0805	Murata/GRM21BR61A106KE19L
1	C5	Capacitor, 47 µF, 25 V electrolytic	Nichicon/UFW1E470MDD
2	C6, C7	Capacitor, ceramic, 510 pF, 50 V, 2%, 0603	Murata/GRM1885C1H511JA01D
2	B1, B2	Wire short	N/A
2	R1, R2	Resistor, 0.0 Ω, 1/8 W, 0805	Panasonic/P0.0ATR-ND
1	R3	Resistor, 47 kΩ, 1/10 W, 1%, 0603	Panasonic/ERJ-3EKF4702V
8	H1 to H5, J1 to J3	Connector, header, 2-position, 0.100" single gold	Tyco/826629-2

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ANALOG DEVICES

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