

Evaluating the **ADAU7002** Using the **EVAL-ADAU7002Z**

FEATURES

- Supports 3.3 V or 1.8 V for PDM/I²S interface
- Supports TDM 2/4/8 operation
- Easy configuration with no software needed

EVALUATION KIT CONTENTS

- ADAU7002** evaluation board (**EVAL-ADAU7002Z**)
- UG-533** user guide

DOCUMENTS NEEDED

- ADAU7002** data sheet
- UG-533** user guide

GENERAL DESCRIPTION

This user guide explains the design and setup of the **ADAU7002** evaluation board. This evaluation board provides full access to all inputs and outputs on the **ADAU7002**. This evaluation board can be powered by a single 3.8 V to 6 V supply or by VDD of the pulse density modulation (PDM) input. The printed circuit board is a 4-layer design, with a single ground plane and a single power plane on the inner layers. The board contains connectors for external microphones and headers for PDM input and I²S output.

EVALUATION BOARD TOP SIDE AND BOTTOM SIDE

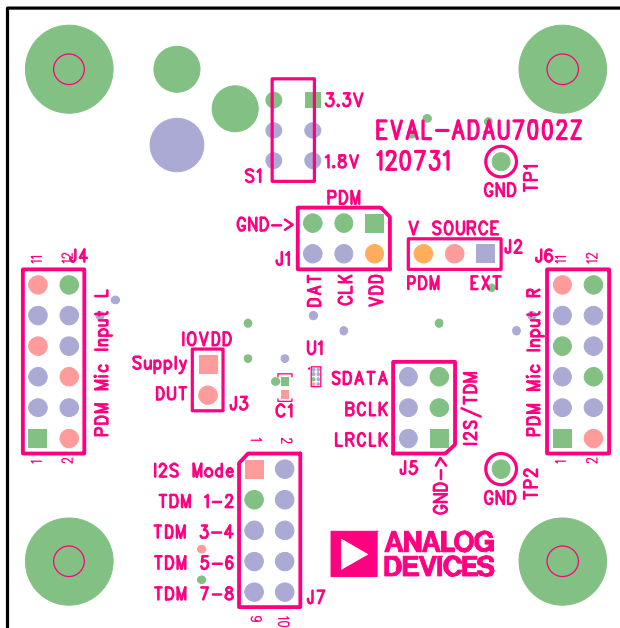


Figure 1. Evaluation Board Top Side

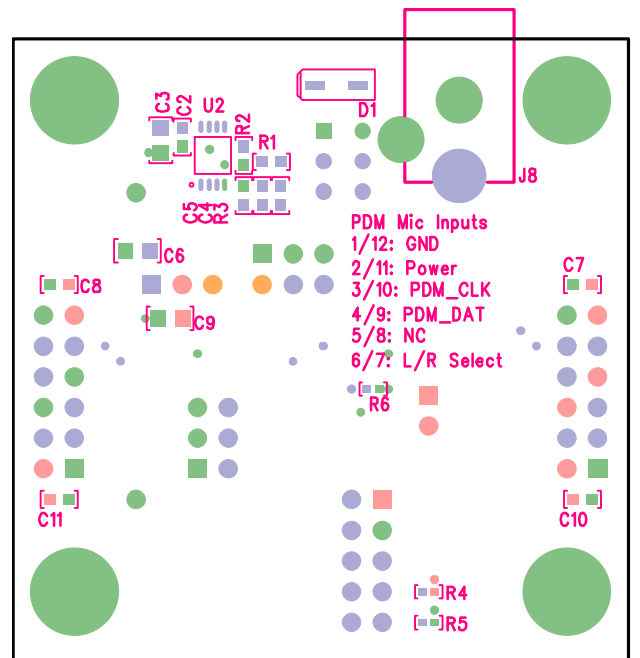


Figure 2. Evaluation Board Bottom Side

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REVISION HISTORY

8/2018—Rev. A to Rev. B

Changes to Figure 16 Caption and Figure 17 Caption 10

7/2018—Rev. 0 to Rev. A

Added Features Section 1

Changes to Evaluation Kit Contents Section and Documents
Needed Section 1

2/2013—Revision 0: Initial Version

EVALUATION BOARD BLOCK DIAGRAMS

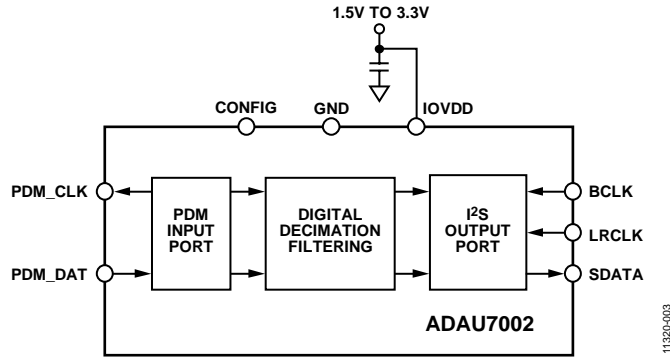


Figure 3. Functional Block Diagram

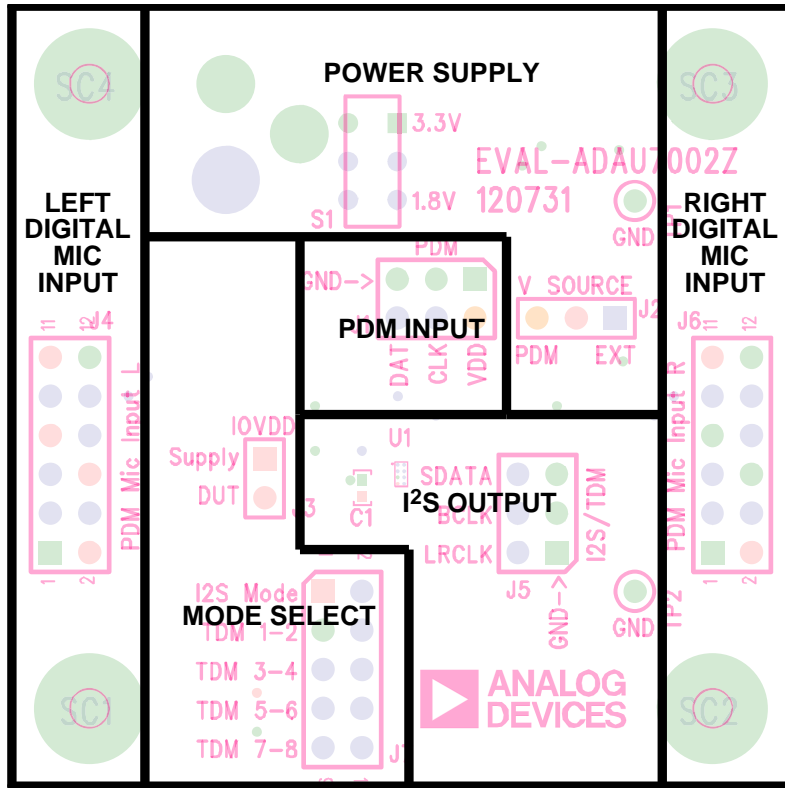


Figure 4. Board Layout Block Diagram

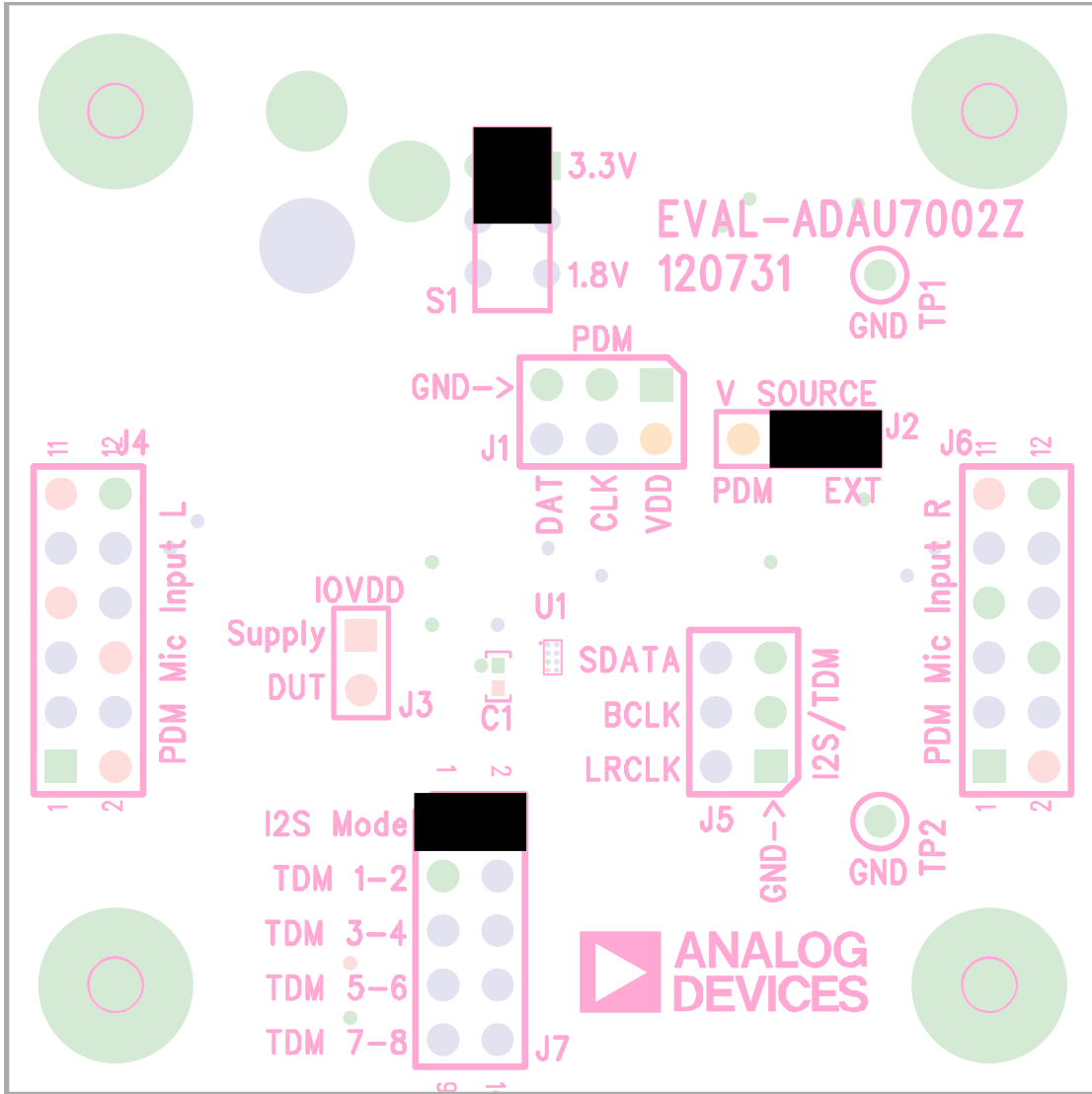


Figure 5. Default Jumpers and Switches

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SETTING UP THE EVALUATION BOARD

DEFAULT SWITCH AND JUMPER SETTINGS

Header J2 selects whether the board is to be powered by VDD of the PDM input or by an external source. The default setting for J2 is EXT—that is, to be powered from an external source (see Figure 5). Switch S1 selects whether the ADAU7002 is to be powered from 3.3 V or 1.8 V. Put the switch in the up position (the default position) to set the voltage level to 3.3 V (see Figure 5).

The default mode for the EVAL-ADAU7002Z board is I²S output. Put a jumper across the top row of Header J7 (see Figure 5).

POWERING UP THE BOARD

To power up the board, connect a tip positive 3.8 V dc to 6 V dc power supply to Connector J8 on the bottom of the board (see Figure 6).

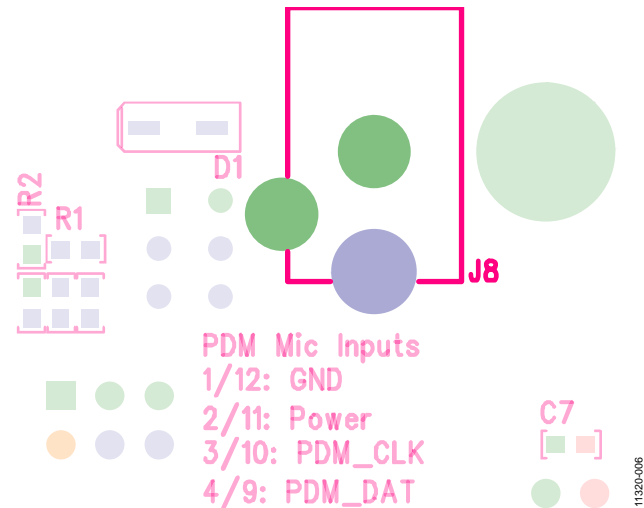


Figure 6. Power Connector J8

CONNECTING THE CABLES

Connect a PDM audio source to the board via Header J1. Because the board is being powered externally, leave the VDD jumper open (see Figure 7).

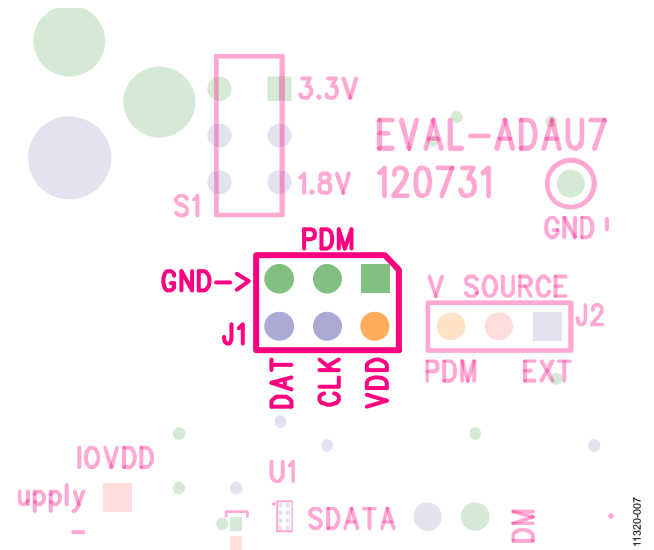


Figure 7. PDM Header

Connections for I²S/TDM output are located on Header J5. Connect SDATA, BCLK, and LRCLK accordingly (see Figure 8).

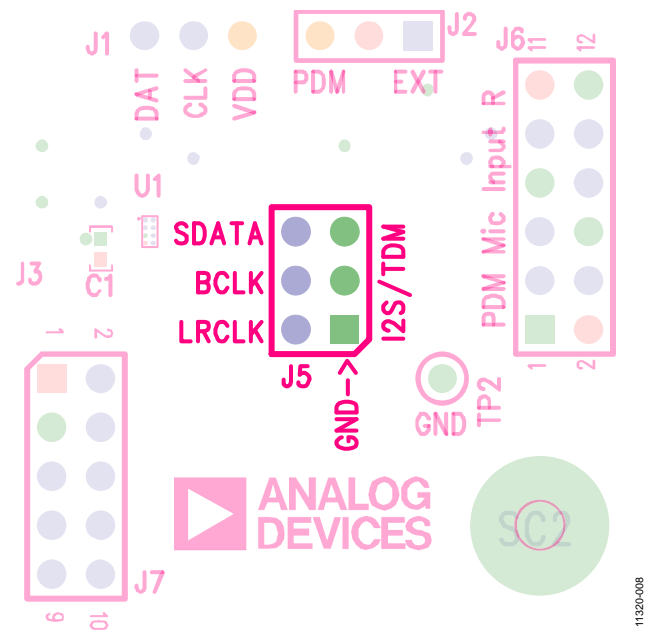


Figure 8. I²S/TDM Header

USING THE EVALUATION BOARD

POWER

Power can be supplied to the [EVAL-ADAU7002Z](#) in two ways:

- When Header J2 is in the EXT position, power can be supplied by connecting a tip positive 3.8 V dc to 6 V dc power supply to Connector J8 on the bottom of the board.
- When Header J2 is in the PDM position, power can be supplied from the VDD output of your PDM source to the VDD pins on Header J1 (see Figure 9).

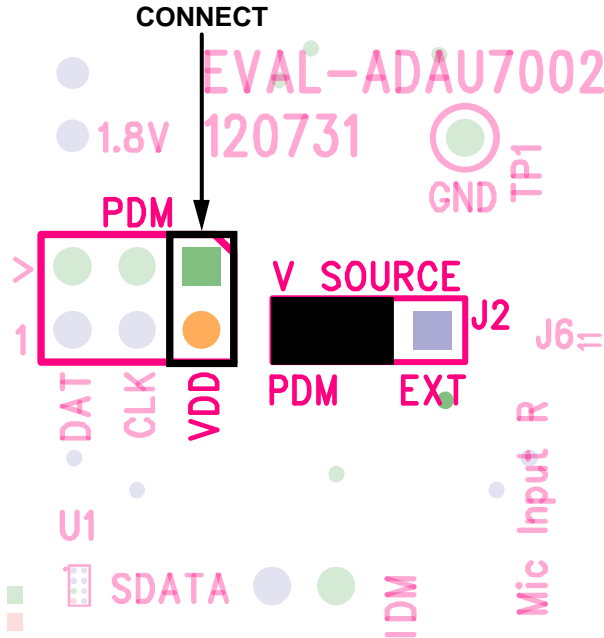


Figure 9. PDM VDD Power

INPUTS AND OUTPUTS

The board has two audio inputs and one audio output. The [ADAU7002](#) is capable of up to two channels of PDM input as well as eight channels of serial audio output in either I²S or TDM format.

Digital Microphones

PDM digital microphones connect to the J4 and J6 standard 0.100" headers (see Figure 10).

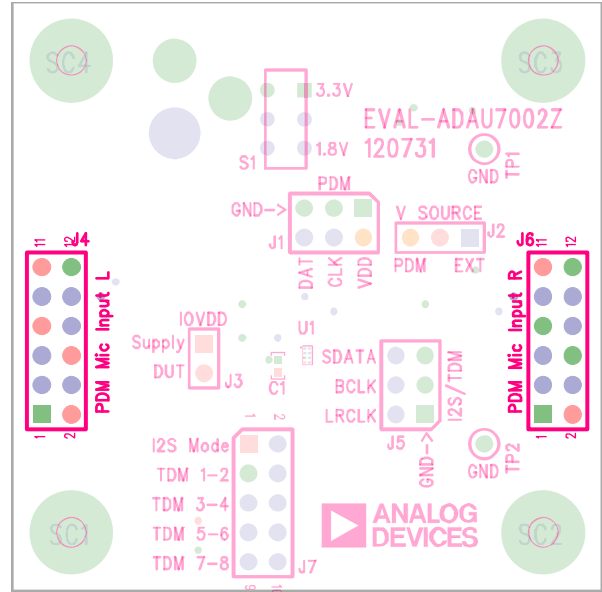


Figure 10. PDM Microphone Headers

SERIAL AUDIO INTERFACE

Serial audio signals in I²S or TDM format can be output via the serial audio interface header, J5 (see Figure 8). The [ADAU7002](#) always operates in slave mode and must be provided LRCLK and BCLK.

MODE SELECT

The mode select configuration header (J7) determines which slots of the TDM stream to output in. If the top row of the header has a jumper across it, the device is in I²S mode. The bottom four rows of Header J7 put the chip in TDM mode. The [ADAU7002](#) outputs two channels of left-justified serial PCM audio on the TDM channels specified by the silkscreen. Row 2 outputs on Slot 1 and Slot 2, Row 3 outputs on Slot 3 and Slot 4, Row 4 outputs on Slot 5 and Slot 6, and Row 5 outputs on Slot 7 and Slot 8 (see Figure 11).

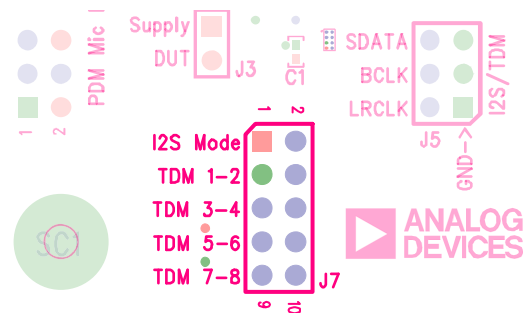


Figure 11. Mode Select Header

HARDWARE DESCRIPTION

JUMPERS

Table 1. Connector and Jack Descriptions

Reference	Functional Name	Description
J1	PDM input	Jumper used for PDM input signals and VDD source.
J2	Voltage source	Header used to choose powering the board from the PDM input or from the on-board regulator.
J3	IOVDD	Unpopulated header used for measuring IOVDD current.
J4, J6	PDM microphone inputs	Headers that allow digital microphones to be connected to the evaluation board.
J5	I ² S/TDM	Jumper used for serial audio output in either I ² S or TDM format.
J7	Mode select	Jumper used to choose between different modes of operation. See the Mode Select section.
J8	Power connector	Tip positive 3.8 V dc to 6 V dc power connector.

INTEGRATED CIRCUITS (IC)

Table 2. IC Descriptions

Reference	Functional Name	Description
U1	ADAU7002	PDM to I ² S/TDM converter.
U2	ADP3336	Adjustable output low dropout regulator.

EVALUATION BOARD SCHEMATICS AND ARTWORK

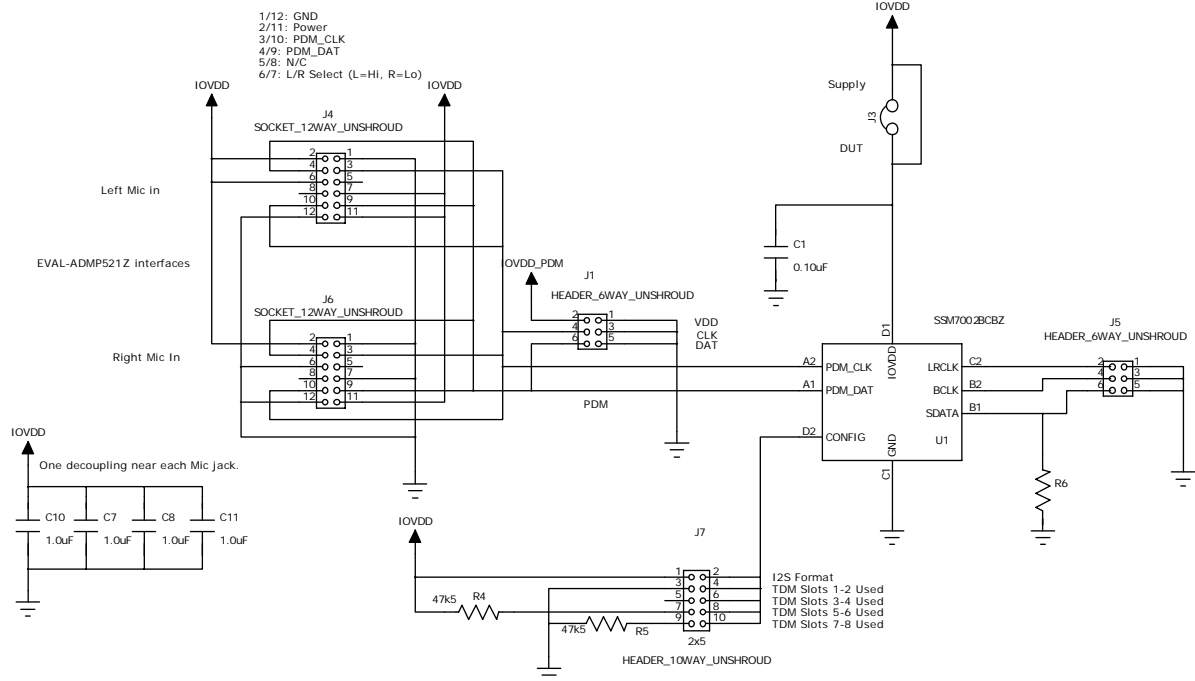


Figure 12. Evaluation Board Schematic

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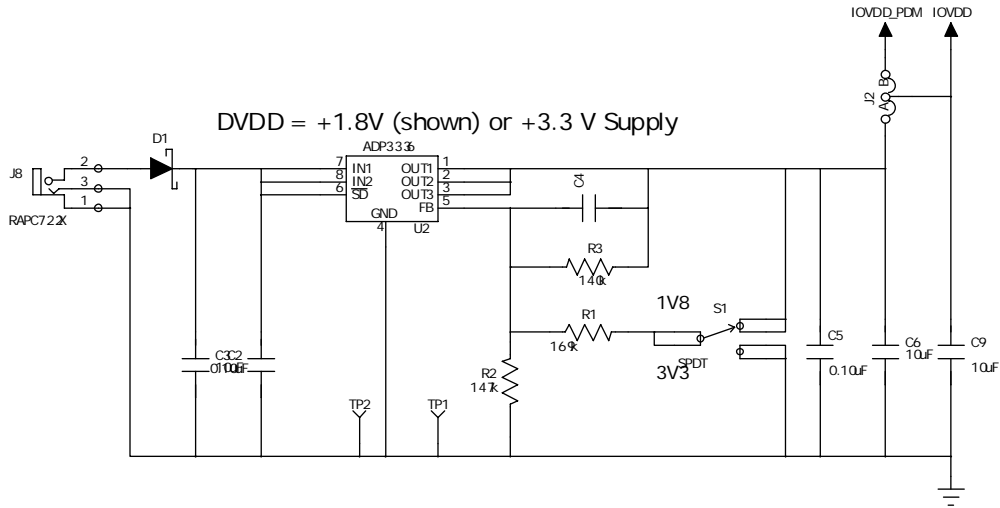


Figure 13. Evaluation Board Schematic—Power Supply

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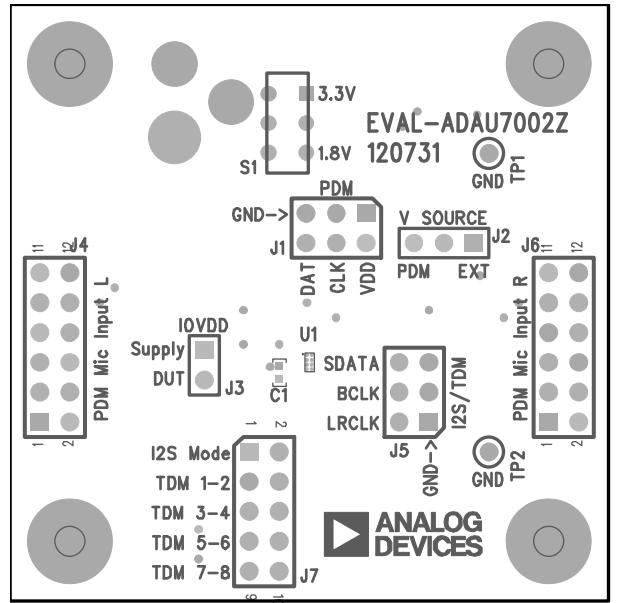


Figure 14. Evaluation Board Layout—Top Assembly

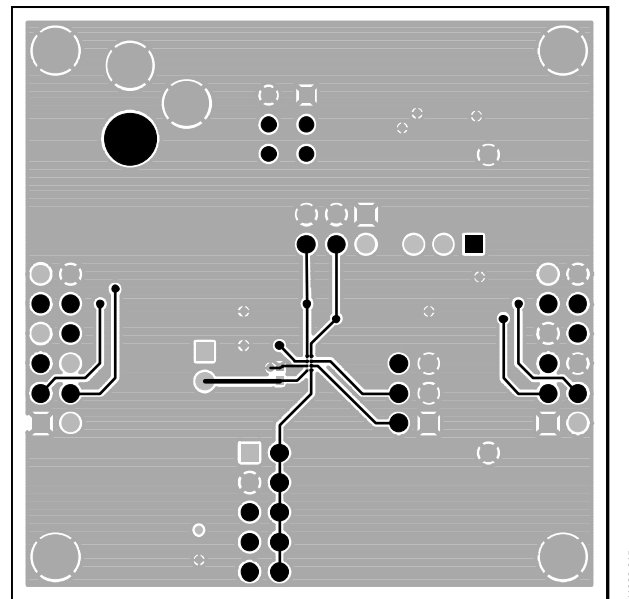
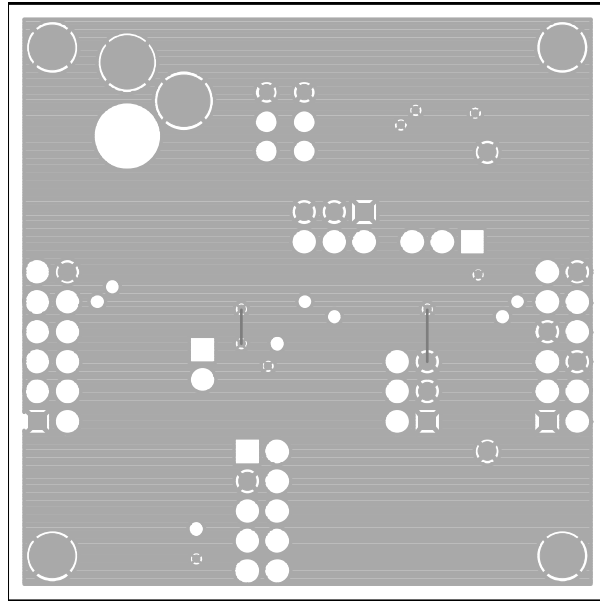
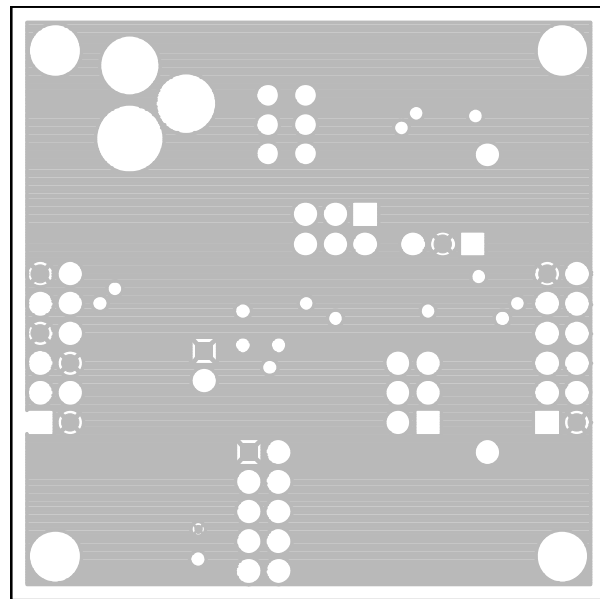


Figure 15. Evaluation Board Layout—Top Copper



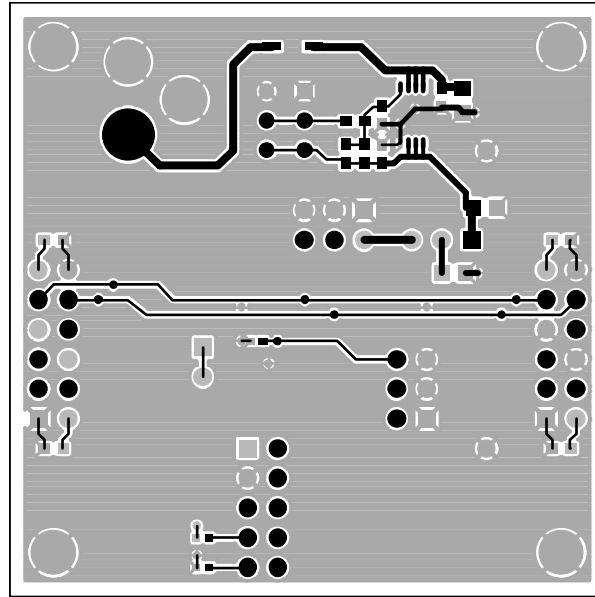
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Figure 16. Evaluation Board Layout—Ground Plane



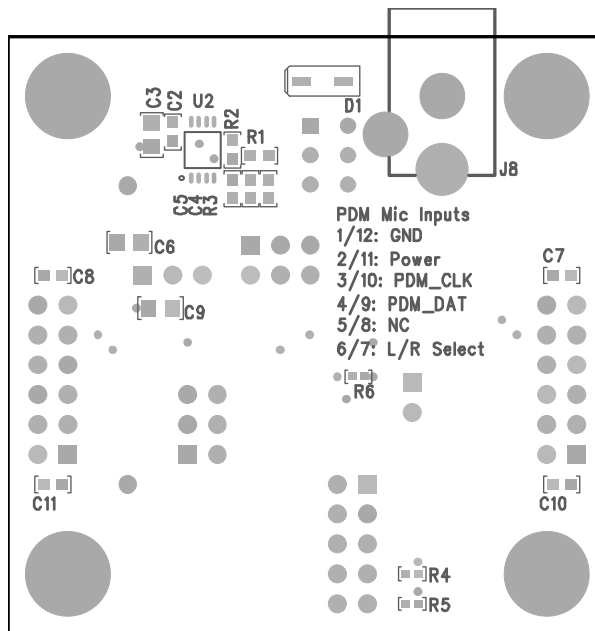
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Figure 17. Evaluation Board Layout—Power Plane



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Figure 18. Evaluation Board Layout—Bottom Copper



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Figure 19. Evaluation Board Layout—Bottom Assembly

BILL OF MATERIALS

Table 3.

Qty.	Reference	Value	Description	Part Number	Manufacturer
1	C1	0.10 μ F	Multilayer ceramic, 16 V, X7R, (0402)	GRM155R71C104KA88D	Murata ENA
2	C2, C5	0.10 μ F	Multilayer ceramic, 50 V, X7R, (0603)	ECJ-1VB1H104K	Panasonic EC
4	C7, C8, C10, C11	1.0 μ F	Multilayer ceramic, 16 V, X7R, (0603)	GRM188R71C105KA12D	Murata ENA
1	C4	10 nF	Multilayer ceramic, 25 V, NP0, (0603)	C1608C0G1E103J	TDK Corp
3	C3, C6, C9	10 μ F	Multilayer ceramic, 10 V, X7R, (0805)	GRM21BR71A106KE51L	Murata ENA
1	R3	140 k Ω	Chip resistor, 1%, 100 mW, thick film, 0603	ERJ-3EKF1403V	Panasonic EC
1	R2	147 k Ω	Chip resistor, 1%, 100 mW, thick film, 0603	ERJ-3EKF1473V	Panasonic EC
1	R1	169 k Ω	Chip resistor, 1%, 100 mW, thick film, 0603	ERJ-3EKF1693V	Panasonic EC
3	R4, R5, R6	4.75 k Ω	Chip resistor, 1%, 63 mW, thick film, 0402	RMCF0402FT4K75	Stackpole
1	U1			ADAU7002BCBZ	Analog Devices
1	U2		Adjustable low dropout voltage regulator	ADP3336ARMZ-REEL7	Analog Devices
1	J7		10-way (2 \times 5) unshrouded header	PBC05DAAN, or cut PBC36DAAN	3M
2	J1, J5		6-way (2 \times 3) unshrouded header	PBC06DAAN, or cut PBC36DAAN	3M
1	J2		3-position SIP header	PBC03SAAN, or cut PBC36SAAN	Sullins
1	D1		Schottky, 30 V, 0.5 A, SOD123 diode	MBR0530T1G	ON Semiconductor
1	J8		Mini power jack, 0.08", R/A TH	RAPC722X	Switchcraft, Inc.
2	J4, J6		12-way (2 \times 6) socket unshrouded	PPPC062LFBN-RC	3M
1	S1		SPDT slide switch PC mount	EG1271	E-Switch
2	TP1, TP2		Mini test point white, 0.1" outer diameter	5002	Keystone Electronics



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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