Evaluation Board User Guide
UG-373

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Evaluation Board for SSM2932 High Efficiency Class-G Headphone Amplifier

PACKAGE CONTENTS

EVAL-SSM2932Z evaluation board

OTHER SUPPORTING DOCUMENTATION

SSM2932 data sheet

GENERAL DESCRIPTION

The SSM2932 is a stereo headphone amplifier capable of delivering 50 mW continuous output power per channel into 16 Ω single-ended loads at the 1% THD + N threshold. The stereo headphone drivers are highly efficient, true ground-referenced Class-G technology.

The SSM2932 incorporates a gain control pin that selects between 0 dB and 6 dB. The ground-referenced output scheme eliminates the need for large dc-blocking capacitors, reducing system BOM cost and board area. The Class-G amplifier is fine-tuned to maximize battery life, a critical task in portable applications. The device maximizes battery life by modulating the amplifier power supply rail to match the output demand without consuming excessive supply current, thus reducing power dissipation during typical audio playback.

The SSM2932 is specified over the industrial temperature range (−40°C to +85°C). It has output short-circuit protection along with ESD protection to 8 kV using a human body model. It is available in 16-ball 1.6 mm × 1.6 mm wafer level chip scale package (WLCSP).

EVALUATION BOARD OVERVIEW

The SSM2932 evaluation board carries a complete application circuit for driving a headphone. Figure 1 shows the top view of the evaluation board, and Figure 2 shows the bottom view.

DIGITAL PICTURE OF THE EVALUATION BOARD

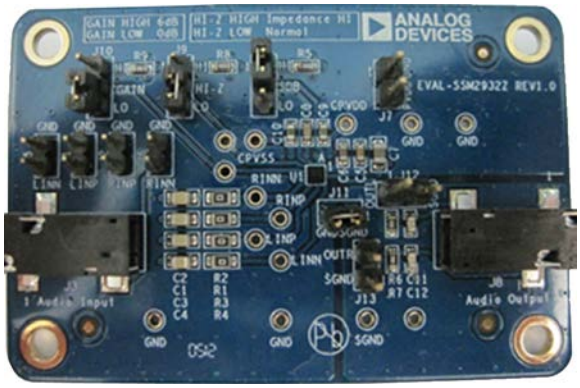

Figure 1. SSM2932 Evaluation Board Top View

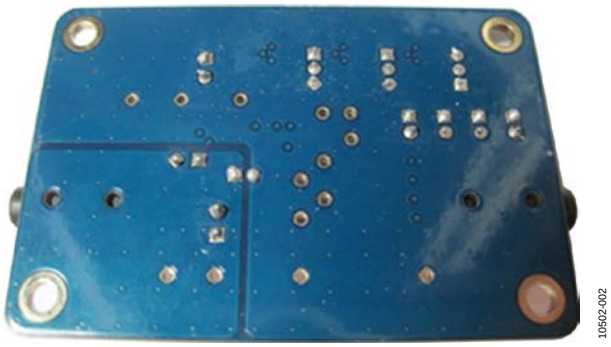

Figure 2. SSM2932 Evaluation Board Bottom View

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REVISION HISTORY

6/12—Revision 0: Initial Version

SETTING UP THE EVALUATION BOARD

INPUT CONFIGURATION

Four of the 2-pin headers (J1, J2, J5, and J6) feed the stereo differential audio signal into the board (see Figure 1). If the input audio signal is a single-ended stereo audio input, an audio jack, J3, (3.5 mm) can be used. To configure the board for single-ended stereo audio input, connect LINP and RINP to ground by inserting jumpers across J1 and J2. Audio signals are then connected to J5 (LINN) and J6 (RINN) or via a 3.5 mm jack to J3.

SHUTDOWN MODE

Shutdown of the SSM2932 amplifier is controlled by the $\overline{SD}$ (J4) pin. If a logic low is applied to the pin by inserting a jumper from the center pin of J4 to GND (low), the amplifier becomes inactive and draws only minimal current from the supply. To activate the amplifier, insert a jumper across the center pin of J4 to PVDD (high).

GAIN CONFIGURATION

The SSM2932 amplifier gain can be set to either 0 dB or 6 dB by applying a logic level to the GAIN pin, as shown in Table 1. J10 is used to configure the SSM2932 amplifier gain to 6 dB and to insert a jumper across the center pin of J10 and PVDD (high). To configure the SSM2932 amplifier gain to 0 dB, insert a jumper across the center pin of J10 and GND (low).

Table 1. Amplifier Gain

Amplifier Gain	GAIN Pin Logic Level
0 dB	Low (≤0.5 V)
6 dB	High (≥1.2 V)

HIGH OUTPUT IMPEDANCE

The SSM2932 has a HI-Z control pin that mutes the amplifier and sets the output to a high impedance. If both HI-Z and $\overline{SD}$ are set to PVDD (high), the amplifier remains in a high-impedance mode. This feature allows the headphone output jack to be shared for other functions such as video output or data transmission. J9 is used to configure the SSM2932 amplifier gain to high impedance output mode and to insert a jumper across the center pin of J9 and PVDD (high). To configure the SSM2932 amplifier output to normal operational mode, insert a jumper across the center pin of J9 and GND (low).

OUTPUT CONFIGURATION

The output connector, J8 can be connected to a set of headphones with a minimum impedance of 16 Ω. J8 is a standard 3.5 mm 3-terminal connector (left, right, and ground). Alternatively, for direct access to the outputs, the user can connect test loads to J12 (OUTL) and J13 (OUTR) for testing on an audio analyzer.

GROUND SENSE

SGND is a headphone ground sense pin and must be connected directly to the common headphone jack. When the headphone jack is connected to a device or board, there is ground difference between the headphone jack's ground pin and audio amplifier. SGND is used to detect this ground difference, which reduces audible noise due to ground loop currents. This also reduces output offset voltage and turn-on pop noise. On the board, SGND is connected to the board GND by placing a jumper across J11.

POWER SUPPLY CONFIGURATION

An external power supply connected to PVDD is required for the SSM2932 to operate. PVDD and GND must be connected by the 2-pin header, J7.

Be sure to connect the dc power supplies with correct polarity and voltage. PVDD must be connected to a supply voltage in the acceptable range, between 2.5 V and 3.6 V. Reverse polarity or overvoltage may damage the board permanently.

PASSIVE COMPONENT SELECTION

INPUT GAIN RESISTORS

If the desired gain of the amplifier is lower than the default 6 dB or 0 dB gain settings, a series resistor can be placed in the input signal path. This creates a voltage divider with the 18 kΩ input resistance on each input pin, allowing an arbitrary reduction of the input signal. Note that input signal attenuation directly reduces SNR performance; therefore, large values compared to the built-in input resistance should be avoided. These components are populated with 0 Ω values on the evaluation board (R1, R2, R3, R4).

INPUT COUPLING CAPACITORS

The input coupling capacitors, C1, C2, C3, and C4, should be large enough to couple the low frequency signal components in the incoming signal but small enough to reject unnecessary extremely low frequency signals. For music signals, the cutoff frequency is typically between 20 Hz and 30 Hz. The value of the input capacitor is calculated by

$$C = 1/(2\pi R_{IN} f_c)$$

where:
R_{IN} = 18 kΩ + (R1, R2 or R3, R4).
f_c is the desired cutoff frequency.

CHARGE PUMP FLYING CAPACITOR

The headphone amplifier uses Class-G architecture and generates the required power supplies with a built-in charge pump, using a flying capacitor connected across CF1 and CF2, C8. The value of C8 is recommended to be 1.0 µF, X7R ceramic capacitor for optimal charge pump operation.

DECOUPLING CAPACITORS FOR CPVDD AND CPVSS

The charge pump within SSM2932 generates CPVDD (positive) and CPVSS (negative) voltage rails for headphone amplifier headphone operation. C9 and C10 serve as a reservoir for the amplifier. For best audio performance, it is recommended that 2.2 µF, X7R ceramic decoupling capacitors be used for CPVDD and CPVSS.

EVALUATION BOARD SCHEMATIC AND ARTWORK

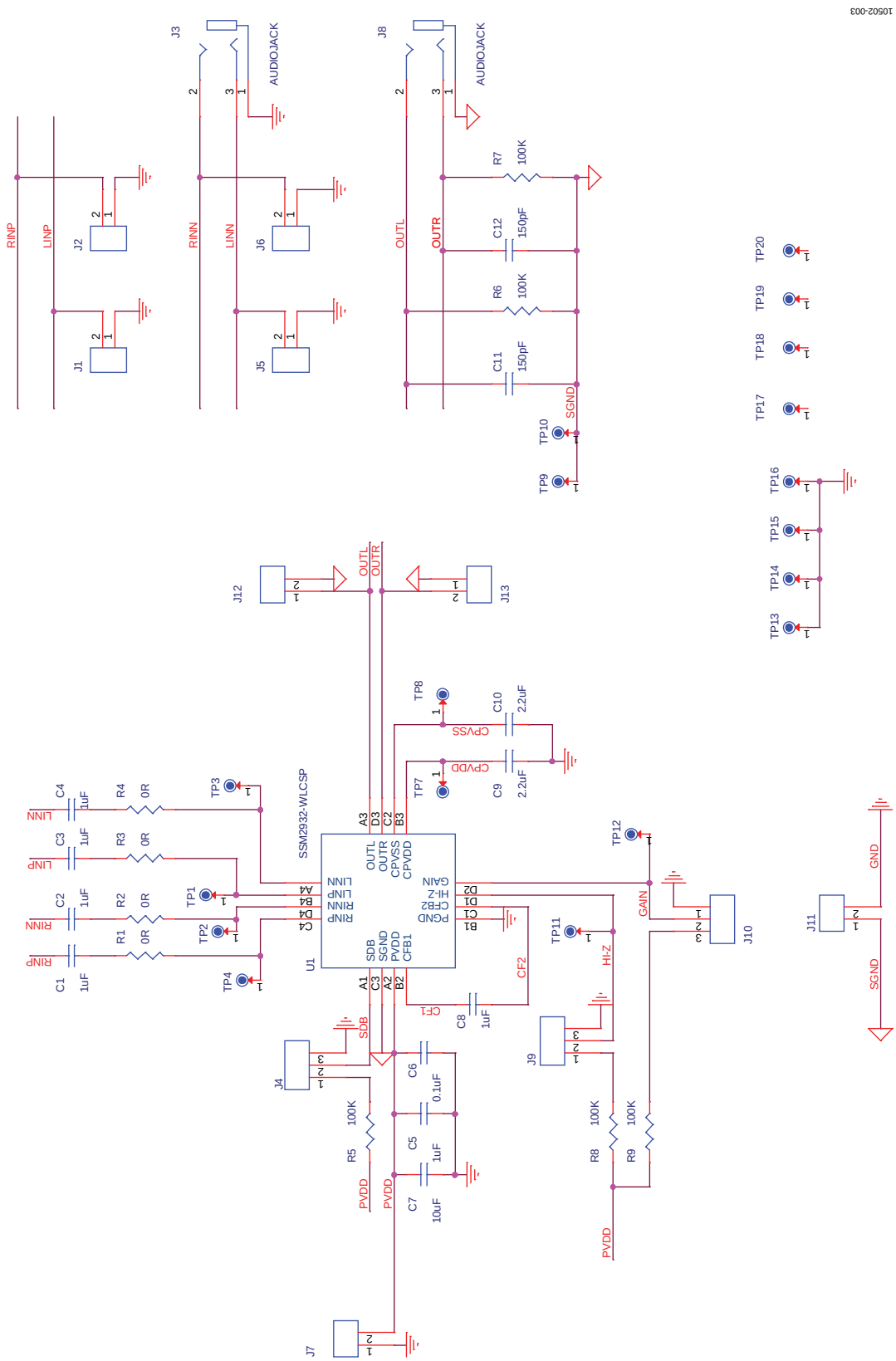

Figure 3. Schematic of the SSM2932 Evaluation Board

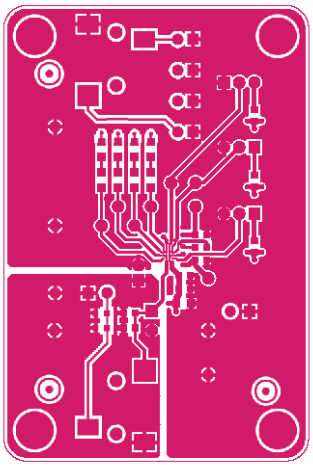

Figure 4. Top Layer Copper

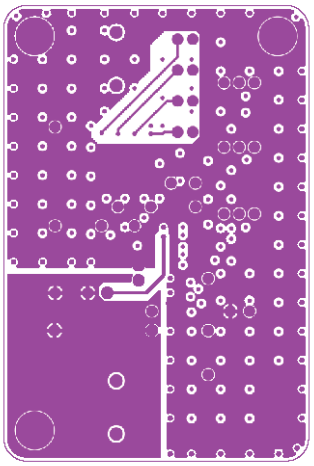

Figure 6. Third Layer Copper—VDD Plane

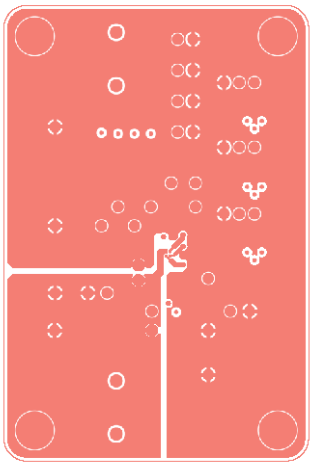

Figure 5. Second Layer Copper—GND Plane

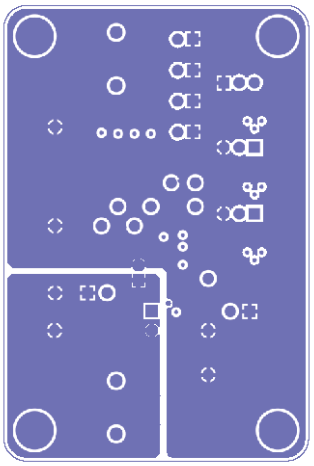

Figure 7. Bottom Layer Copper

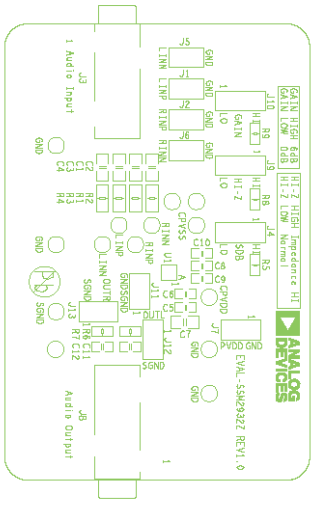

Figure 8. Top Silkscreen

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Qty	Reference Designator	Description	Supplier/Part No.
1	U1	IC, SSM2932	Analog Devices/SSM2932CBZ
4	C1, C2, C3, C4	Capacitor, ceramic 1.0 µF, 25 V, X7R, 080	Taiyo Yuden/TMK212B7105KG-T
2	C5, C8	Capacitor, ceramic 1.0 µF, 25 V, X7R, 0603	Taiyo Yuden/TMK107B7105KA-T
1	C6	Capacitor, ceramic 0.1 µF, 16 V, X7R, 0603	KEMET/C0603C104J4RACTU
1	C7	Capacitor, ceramic 10 µF, 16 V, X5R, 0805	KEMET/C0805C106K4PACTU
2	C9, C10	Capacitor, ceramic 2.2 µF, 25 V, X5R, 0603	Taiyo Yuden/TMK107ABJ225KA-T
2	C20, C23	Capacitor, ceramic, 150 pF, 25 V, X7R, 0603	AVX/06033C151KAT2A
2	J3, J10	Audio jack 3.5 mm stereo SMD	CUI Inc./SJ-3523-SMT
4	R6, R7, R8, R9	Resistor, 0.0 Ω, 1/8 W, 0805	Panasonic/ECG/ERJ-6GEY0R00V
5	R1, R2, R3, R4, R5	Resistor, 100 kΩ, 1/10 W, 1%, 0603	Vishay/CRCW0603100KFKEA
1	J8	Connector, header, 2-position, 0.100" single gold	Samtec/TSW-202
3	J4, J11, J12	Connector, header, 3-position, 2 mm single gold	Samtec/TMM-103
5	J1, J2, J5, J6, J13	Connector, header, 2-position, 2 mm single gold	Samtec/TMM-102

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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