Evaluation Board for a 20-Bit Serial Input, Voltage Output DAC with Integrated Precision Reference Buffer Amplifiers

FEATURES
Full-featured evaluation board for the AD5790
Link options
PC control in conjunction with Analog Devices, Inc., system demonstration platform
PC software for control

EVALUATION BOARD DESCRIPTION
The EVAL-AD5790SDZ is a full-featured evaluation board, designed to allow the user to easily evaluate all features of the AD5790 voltage output, 20-bit digital-to-analog converter (DAC). The AD5790 pins are accessible at on-board connectors for external connection. The board can be controlled by two means: via the on-board connector (J3), or via the system demonstration platform (SDP) connector (J4). The SDP board allows the evaluation board to be controlled through the USB port of a Windows® XP (SP2 or later) or more recent 32-bit or 64-bit (Vista, Windows 7) PC using the AD5790 evaluation software.

DEVICE DESCRIPTION
The AD5790 is a high precision, 20-bit DAC with integrated precision reference buffer amplifiers designed to meet the requirements of precision control applications. The output range of the AD5790 is configured by two reference voltage inputs. The device is specified to operate with a dual power supply of up to 33 V.

Complete specifications for the AD5790 are provided in the AD5790 data sheet, available from Analog Devices, and should be consulted in conjunction with this user guide when using the evaluation board.

FUNCTIONAL BLOCK DIAGRAM

Figure 1.
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REVISION HISTORY

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11/11—Revision 0: Initial Version
EVALUATION BOARD HARDWARE

POWER SUPPLIES

The following external supplies must be provided:

- 5 V between the VCC and DGND inputs for the digital supply of the AD5790. Alternatively, place Link 1 in Position A to power the digital circuitry from the USB port via the SDP board (default).
- 7.5 V to 16.5 V between the VDD and AGND inputs for the positive analog supply of the AD5790.
- −2.5 V to −16.5 V between the VSS and AGND inputs for the negative analog supply of the AD5790.

The analog and digital planes are connected at one location, close to the AD5790. To avoid ground loop problems, it is recommended not to connect AGND and DGND elsewhere in the system.

Each supply is decoupled to the relevant ground plane with 10 µF and 0.1 µF capacitors. Each device supply pin is again decoupled with a 10 µF and 0.1 µF capacitor pair to the relevant ground plane.

LINK OPTIONS

The link options on the evaluation board should be set for the required operating setup before using the board. The functions of the link options are described in Table 3.

Default Link Option Setup

The default link options are listed in Table 1. By default, the board is configured with \( V_{\text{REFP}} = +10 \text{ V} \) and \( V_{\text{REFN}} = -10 \text{ V} \) for a ±10 V output range.

Table 1. Default Link Options

<table>
<thead>
<tr>
<th>Link No.</th>
<th>Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>A</td>
</tr>
<tr>
<td>LK2</td>
<td>B</td>
</tr>
<tr>
<td>LK3</td>
<td>A</td>
</tr>
<tr>
<td>LK4</td>
<td>Removed</td>
</tr>
<tr>
<td>LK5</td>
<td>Removed</td>
</tr>
<tr>
<td>LK6</td>
<td>Removed</td>
</tr>
<tr>
<td>LK7</td>
<td>Removed</td>
</tr>
<tr>
<td>LK8</td>
<td>C</td>
</tr>
<tr>
<td>LK9</td>
<td>Inserted</td>
</tr>
<tr>
<td>LK11</td>
<td>Inserted</td>
</tr>
</tbody>
</table>

Connector J3 Pin Configuration

Figure 2 shows the pin configuration of Connector J3.

![Figure 2. Connector J3 Pin Configuration](image)

ON-BOARD CONNECTORS

There are nine connectors on the AD5790 evaluation board PCB as outlined in Table 2.

Table 2. On-Board Connectors

<table>
<thead>
<tr>
<th>Connector</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Digital power supply connector</td>
</tr>
<tr>
<td>J2</td>
<td>Analog power supply connector</td>
</tr>
<tr>
<td>J3</td>
<td>Digital interface pin header connector</td>
</tr>
<tr>
<td>J4</td>
<td>SDP board connector</td>
</tr>
<tr>
<td>VOUT</td>
<td>DAC output connector</td>
</tr>
<tr>
<td>VOUT_BUF</td>
<td>Buffered DAC output connector</td>
</tr>
<tr>
<td>VREF</td>
<td>5 V external reference voltage input connector(+10 \text{ V}, +5 \text{ V}, −10 \text{ V}, \text{ and } −5 \text{ V} \text{ reference voltages are generated from this 5 V input or on-board ADR4550})</td>
</tr>
<tr>
<td>VREFN</td>
<td>DAC negative reference input connector</td>
</tr>
<tr>
<td>VREFP</td>
<td>DAC positive reference input connector</td>
</tr>
<tr>
<td>Link No.</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| LK1     | This link selects the source of the digital power supply.  
Position A selects the source from the SDP board.  
Position B selects the source from Connector J1. |
| LK2     | This link selects the positive reference voltage source.  
Position A selects an on-board generated 5 V.  
Position B selects an on-board generated 10 V.  
Position C selects an external voltage applied at Connector VREFP. |
| LK3     | This link is used in conjunction with LK4 to configure the mode of operation of the output amplifier.  
Position A configures the amplifier in unity gain. LK4 should be removed.  
Position B configures the amplifier for a gain of 2. LK4 should be inserted. |
| LK4     | This link is used in conjunction with LK3 to configure the mode of operation of the output amplifier.  
When this link is inserted, LK3 should be in Position B to configure the amplifier for a gain of 2.  
When this link is removed, LK3 should be in Position A to configure the amplifier for unity gain. |
| LK5     | This link selects the state of the RESET pin.  
When this link is inserted, RESET is at logic low.  
When this link is removed, RESET is at logic high. |
| LK6     | This link selects the state of the CLR pin.  
When this link is inserted, CLR is at logic low.  
When this link is removed, CLR is at logic high. |
| LK7     | This link selects the state of the LDAC pin.  
When this link is inserted, LDAC is at logic low.  
When this link is removed, LDAC is at logic high. |
| LK8     | This link selects the negative reference voltage source.  
Position A selects an on-board generated −5 V.  
Position B selects AGND.  
Position C selects an on-board generated −10 V.  
Position D selects an external voltage applied at Connector VREFN. |
| LK9     | This link connects the output of Voltage Reference U5 to the reference scaling circuitry. |
| LK11    | This link connects the DAC output to the noninverting input of the output buffer amplifier.  
When this link is inserted, the DAC output is connected to the noninverting input of the output amplifier.  
When this link is removed, the DAC output is disconnected from the noninverting input of the output buffer amplifier and the DAC output voltage is accessible at the VOUT connector. |

1 The RBUF bit of the control register must be set to high to enable the unity-gain mode of operation.  
2 The RBUF bit of the control register must be cleared to low to enable the gain of 2 mode of operation.
EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The AD5790 evaluation kit includes self-installing software on a CD. The software is compatible with Windows XP (SP2) and Vista (32-bit or 64-bit). If the setup file does not run automatically, you can run the `setup.exe` file from the CD.

Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

1. After installation from the CD is complete, power up the AD5790 evaluation board as described in the Power Supplies section. Connect the SDP board (via either Connector A or Connector B) to the AD5790 evaluation board and then to the USB port of your PC using the supplied cable.
2. When the evaluation system is detected, proceed through any dialog boxes that appear. This completes the installation.

SOFTWARE OPERATION

To launch the software, complete the following steps:

1. From the Start menu, select Analog Devices, AD5790, then AD5790 Evaluation Software. The main window of the software then opens (see Figure 4).
2. If the evaluation system is not connected to the USB port when the software is launched, a connectivity error displays (see Figure 3). Connect the evaluation board to the USB port of the PC, wait a few seconds, click Rescan, and follow the instructions.

![Figure 3. Connectivity Error Alert](image)

![Figure 4. Main Window](image)
MAIN WINDOW

The main window is divided into three tabs: Configure, Program Voltage, and Measure DAC Output.

Configure

The Configure section allows access to the control register, clearcode register, software control register, and DAC register and allows control of the RESET, CLR, and LDAC pins.

Program Voltage

The Program Voltage section programs the DAC register with the value calculated from the entered values: the positive voltage reference (VREFP), the negative voltage reference (VREFN), and the desired output voltage (see Figure 5).

Measure DAC Output

The Measure DAC Output section allows the PC to control an Agilent 3458A multimeter to measure and log the DAC output voltage.

The multimeter is controlled over a general-purpose interface bus (GPIB). When the multimeter is connected to the PC, first configure the multimeter via its front panel before taking a measurement. Figure 7 shows the measurement options. The software runs through a sequence of steps, programming the DAC register and measuring the DAC output voltage. The sequence begins with the software programming the DAC with the Start Code value, incrementing the programmed value at each step by the Code Step value, and finishing when the programmed value reaches the Stop Code value. A delay between measurements can be inserted, if required. The GPIB address of the multimeter must be specified.

To begin the measurement, click START. The measurement can be halted at any time by clicking STOP. When the measurement is completed, a dialog box opens to allow you to save the data as a spreadsheet file with three columns of data. The first column is the DAC code, the second column is the DAC voltage in volts, and the third column is the INL error in LSBs, as shown in Figure 6. A graph of both the DAC output voltage vs. the DAC code and the INL error vs. the DAC code is displayed in the Measure DAC Output tab (see Figure 7). In the measurement example shown in Figure 7, measurements are taken in 10000 code steps beginning at Code 0 and finishing at Code 1,048,575 in a total of 100 measurements. With the number of power line cycles (NPLC) setting on the multimeter set to 1, the measurement takes ~10 sec to complete. To complete an all codes measurement requiring 1,048,575 measurement points takes ~1 day.

If an Agilent 3458A multimeter is not connected to the PC, the software steps through the codes without taking any measurements.
Figure 7. Measure DAC Output Tab
Figure 8. Schematic of the AD5790 Circuitry
Figure 9. Schematic of the Voltage Reference Circuitry
Figure 10. Schematic of the SDP Board Connector
Figure 11. Component Placement Schematic

Figure 12. Top Printed Circuit Board (PCB) Layer Schematic
Figure 13. Inner First PCB Layer Schematic

Figure 14. Inner Second PCB Layer Schematic
## ORDERING INFORMATION

### BILL OF MATERIALS

**Table 4.**

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>Part Description</th>
<th>Part Number</th>
<th>Stock Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2, C5, C6, C10, C11, C13, C17, C19, C20, C23, C24, C34 to C36, C40 to C42</td>
<td>Capacitor, 0603, 0.1 µF, 16 V</td>
<td>CM105X7R104K16AT</td>
<td>FEC 9406140</td>
</tr>
<tr>
<td>C3, C4, C8, C9, C14, C16, C18, C21, C22, C31, C32, C33, C37 to C39, C43</td>
<td>Capacitor +, 10 µF, 16 V, 10%, Case B</td>
<td>TAJB106K016R</td>
<td>FEC 498737</td>
</tr>
<tr>
<td>J1</td>
<td>2-pin terminal block (5 mm pitch) CON/POWER</td>
<td>CTB5000/2</td>
<td>FEC 151789</td>
</tr>
<tr>
<td>J2</td>
<td>3-pin terminal block (5 mm pitch) CON/POWER3</td>
<td>CTB5000/3</td>
<td>FEC 151790</td>
</tr>
<tr>
<td>J3</td>
<td>20-pin (2 × 10) header</td>
<td>Not applicable</td>
<td>FEC 1022244</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(36 + 36-pin strip)</td>
<td></td>
</tr>
<tr>
<td>J4</td>
<td>120-way connector, 0.6 mm pitch, SDP-STANDARD-CONN</td>
<td>FX8-1205-SV(21)</td>
<td>FEC 1324660</td>
</tr>
<tr>
<td>L1 to L4</td>
<td>Ferrite bead IND</td>
<td>74279204</td>
<td>FEC 1635719</td>
</tr>
<tr>
<td>LK1, LK3</td>
<td>3-pin SIL header and shorting link</td>
<td>M20-9990345 and M7567-05</td>
<td>FEC 1022448</td>
</tr>
<tr>
<td>LK2</td>
<td>6-pin (3 × 2) 0.1” header and shorting block</td>
<td>M20-9983646 and M7566-05</td>
<td>FEC 148535</td>
</tr>
<tr>
<td>LK4 to LK7, LK9, LK11</td>
<td>2-pin (0.1” pitch) header and shorting shunt</td>
<td>M20-9990246</td>
<td>FEC 1022247</td>
</tr>
<tr>
<td>LK8</td>
<td>8-pin (4 × 2) 0.1” header and shorting block</td>
<td>M20-9983646 and M7566-05</td>
<td>FEC 1022244</td>
</tr>
<tr>
<td>R1 to R12</td>
<td>SMD resistor</td>
<td>MC 0.063W 0603 10k</td>
<td>FEC 9331700</td>
</tr>
<tr>
<td>R13, R15, R17, R19, R20</td>
<td>Resistor, 1 kΩ, 0805, 5 ppm</td>
<td>PCF0805-13-1K-B-T1</td>
<td>FEC 31108863</td>
</tr>
<tr>
<td>R16</td>
<td>Resistor, 2 kΩ, 0805, 5 ppm</td>
<td>PCF0805-13-2K-B-T1</td>
<td>FEC 1108872</td>
</tr>
<tr>
<td>R18</td>
<td>Resistor, 0805, 680 Ω</td>
<td>MC 0.1W 0805 5% 680R</td>
<td>FEC 9334785</td>
</tr>
<tr>
<td>R21</td>
<td>Resistor, 0805, 510 Ω</td>
<td>MC 0.1W 0805 5% 510R</td>
<td>FEC 9334637</td>
</tr>
<tr>
<td>R22</td>
<td>Resistor, 0805, 1.5 kΩ</td>
<td>MC 0.1W 0805 5% 1K5</td>
<td>FEC 9333924</td>
</tr>
<tr>
<td>TP1 to TP7</td>
<td>Red test point</td>
<td>20-2137</td>
<td>FEC 240-333</td>
</tr>
<tr>
<td>U1</td>
<td>20-bit DAC</td>
<td>ADS790BCPZ</td>
<td>ADS790BCPZ</td>
</tr>
<tr>
<td>U2, U6</td>
<td>Single op amp</td>
<td>AD8675ARZ</td>
<td>AD8675ARZ</td>
</tr>
<tr>
<td>U8, U9</td>
<td>Dual op amp</td>
<td>AD8676BRZ</td>
<td>AD8676BRZ</td>
</tr>
<tr>
<td>U4</td>
<td>64k I2C serial EEPROM</td>
<td>24LC64-1SN</td>
<td>FEC 9758070</td>
</tr>
<tr>
<td>U5</td>
<td>5 V reference</td>
<td>ADR4550BRZ</td>
<td>ADR4550BRZ</td>
</tr>
<tr>
<td>VOUT, VOUT_BUF, VREF, VREFN, VREFP</td>
<td>Straight PCB mount SMB jack, 50 Ω</td>
<td>1-1337482-0</td>
<td>FEC 1206013</td>
</tr>
</tbody>
</table>
NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED “AS IS” AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENT, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER’S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI’S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00).

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