Evaluation Board for Dual, High Speed Op Amps
Offered in 8-Lead SOIC Packages

FEATURES
- Enables quick breadboarding/prototyping
- User-defined circuit configuration
- Edge-mounted SMA connector provisions
- Easy connection to test equipment and other circuits
- RoHS compliant

GENERAL DESCRIPTION
The Analog Devices, Inc., 8-lead SOIC package, dual, high speed evaluation board is designed to help customers quickly prototype new dual op amp circuits and reduce design time. The evaluation board can be used with almost any Analog Devices dual op amp in various configurations and applications. The evaluation board is a bare board (that is, there are no components or amplifier soldered to the board; these must be ordered separately). Figure 1 shows the component side of the evaluation board, and Figure 2 shows the circuit side of the evaluation board. This evaluation board is a 6-layer PCB, designed to provide internal, wideband, power supply bypassing without the use of external capacitors. The close spacing between the VCC supply plane (Layer 3) and the inner ground plane (Layer 4) provides the necessary capacitance to bypass the VCC supply. Similarly, the close spacing between the inner ground layer (Layer 4) and the VEE supply plane (Layer 5) provides the necessary capacitance to bypass the VEE supply.

The evaluation board components are primarily SMT 0603 case size, with the exception of the electrolytic bypass capacitors (C1, C2), which are 1206 case size.

Two options are available for supply bypassing. The first option is to use the internal interplanar capacitance. No external bypass capacitors are required. Capacitors C1 to C5 can be left off the board. If additional supply bypassing is required, C1 and C2 can accommodate 1206 tantalum or nonpolarized capacitors. C3, C4, and C5 accommodate 0603 capacitors.

Figure 3 shows the evaluation board schematic. Figure 4 and Figure 5 show the evaluation board assembly drawings.

EVALUATION BOARD COMPONENT AND CIRCUIT SIDES

Figure 1. Component Side of Evaluation Board
Figure 2. Circuit Side of Evaluation Board
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# REVISION HISTORY

8/11—Rev. A to Rev. B  
Changes to General Description Section, Figure 1, and Figure 2 ................................. 1  
Changed Evaluation Board Schematic Section to Evaluation Board Schematic and Assembly Drawings Section ................................................................. 3  
Changes to Figure 3, Figure 4, and Figure 5 ................................................................ 3  
Deleted Figure 6 and Figure 7; Renumbered Sequentially ....................................... 4  
Added Evaluation Board Layer Stackup Section ................................................... 4  
Added Figure 6; Renumbered Sequentially .............................................................. 4  
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4/11—Rev. 0 to Rev. A  
Changes to Product Title, General Description Section, Figure 1 and Figure 2 ............. 1  
Changed Evaluation Board Schematic and Artwork Section to Evaluation Board Schematic Section ............................................................... 3  
Added Evaluation Board Assembly Drawings and Layout Patterns Section .................. 4  
Changes to Figure 4 through Figure 7 ...................................................................... 4

4/10—Revision 0: Initial Version
EVALUATION BOARD SCHEMATIC AND ASSEMBLY DRAWINGS

Figure 3. Evaluation Board Schematic

Figure 4. Component Side Assembly Drawing

Figure 5. Component Side Copper
EVALUATION BOARD LAYER STACKUP

6-LAYER STACKUP

TOP SILK
TOP MASK
TOP COPPER

2 × 106  0.009" 50Ω WITH 16 mils TRACE WIDTH

INNER COPPER GND

0.37" SPACER

INNER COPPER VCC
1 × 1080  0.0032"

INNER COPPER GND
1 × 1080  0.0032"

INNER COPPER VEE
1 × 1080  0.0032"

BOTTOM COPPER GND
BOTTOM MASK
BOTTOM SILK

0.062"

Figure 6. Evaluation Board Stackup
## ORDERING INFORMATION

### BILL OF MATERIALS

Table 1.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PWR</td>
<td>Power connector</td>
<td>0.1 inch spacing</td>
</tr>
<tr>
<td>2</td>
<td>C1, C2</td>
<td>10 μF capacitor</td>
<td>C1206</td>
</tr>
<tr>
<td>3</td>
<td>C3, C4, C5</td>
<td>User-defined capacitor</td>
<td>C0603</td>
</tr>
<tr>
<td>1</td>
<td>DUT</td>
<td>Device</td>
<td>8-lead SOIC</td>
</tr>
<tr>
<td>6</td>
<td>VIN1P, VIN2P, VIN1N, VIN2N, VOUT1, VOUT2</td>
<td>SMA/SMT</td>
<td>SMA/SMT</td>
</tr>
<tr>
<td>18</td>
<td>R1 to R16, RS1, RS2</td>
<td>User-defined resistor</td>
<td>R0603</td>
</tr>
</tbody>
</table>
ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the “Evaluation Board”), you are agreeing to be bound by the terms and conditions set forth below (“Agreement”) unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement.  Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement.  Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement.

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