

## Setting Up the Evaluation Board for the ADCLK944

### PACKAGE CONTENTS

Evaluation board with ADCLK944 component installed

### GENERAL DESCRIPTION

This user guide describes how to set up and use the evaluation board for the [ADCLK944](#). The ADCLK944 data sheet should be used in conjunction with this user guide.

The data sheet contains full technical details about the specifications and operation of this device.

The ADCLK944 is a very high performance clock fanout buffer. The evaluation board is fabricated using high quality Rogers dielectric material. Transmission line paths are kept as close to 50  $\Omega$  as possible.

### DIGITAL PICTURE OF EVALUATION BOARD

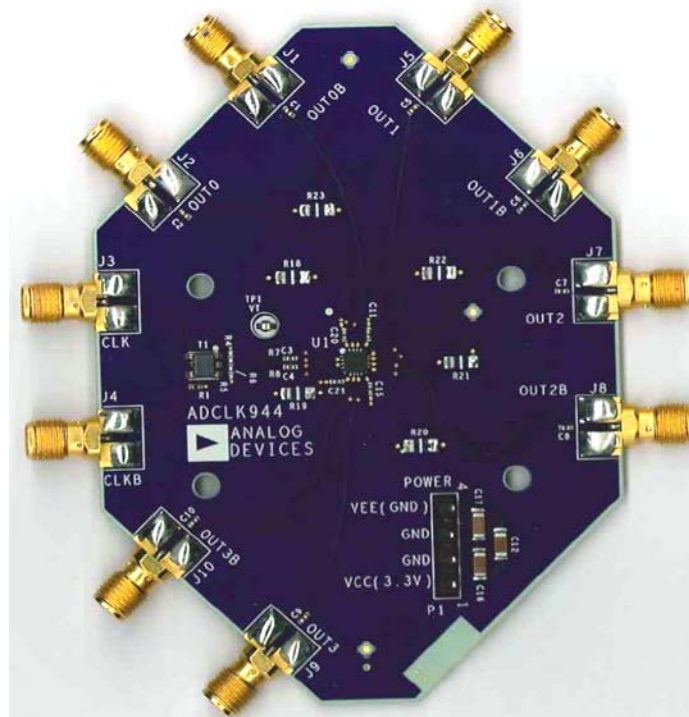


Figure 1. ADCLK944 Evaluation Board

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**REVISION HISTORY**

4/10—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

### RECOMMENDED BOARD SETUP

The recommended setup for the ADCLK944 evaluation board is shown in Figure 2.  $V_{CC}$  is set to 2.5 V to 3.3 V, and  $V_{EE}$  is set to GND.

On the evaluation board, the clock input is set up for single-ended-to-differential operation via the balun. In addition, series capacitors in the path provide ac-coupled inputs to the ADCLK944. The common-mode voltage for both inputs is provided by tying  $V_{REF}$  and  $V_T$  together. This connection is made with R13 installed at the factory.

The range of the peak-to-peak input voltage swing at CLK is 0.2 V p-p to 1.7 V p-p. Note that output jitter performance is degraded by an input slew rate, as shown in the [ADCLK944](#) data sheet.

Table 1. Basic Equipment Required

Quantity	Description
1	Single power supply
1	Signal source
1	High bandwidth oscilloscope
4	Matched high speed cables

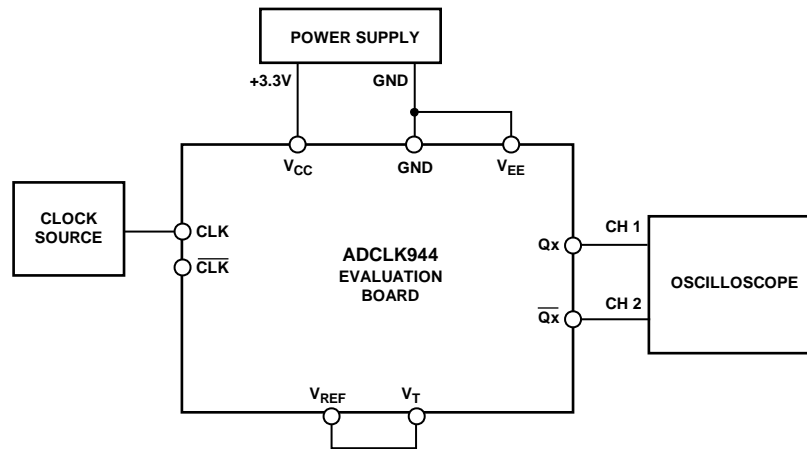


Figure 2. Recommended Setup for Device Evaluation

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**CLOCK OUTPUTS**

The ADCLK944 has four differential outputs. All differential clock outputs on the evaluation board are biased to GND via 200 Ω and ac-coupled to the SMAs. From the SMAs, use matched 50 Ω coaxial cables into the oscilloscope for evaluation. See the evaluation board schematic in Figure 4 for more details.

**Table 2. Power Connections via P1**

Label	ADCLK944
GND	Connect to GND
V <sub>CC</sub>	Connect to 3.3 V
V <sub>EE</sub>	Connect to GND

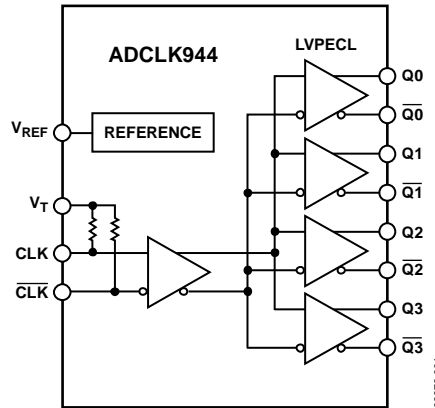


Figure 3. ADCLK944 1:4 Clock/Data Buffer Block Diagram

EVALUATION BOARD SCHEMATIC AND ARTWORK

P00-9Z-690

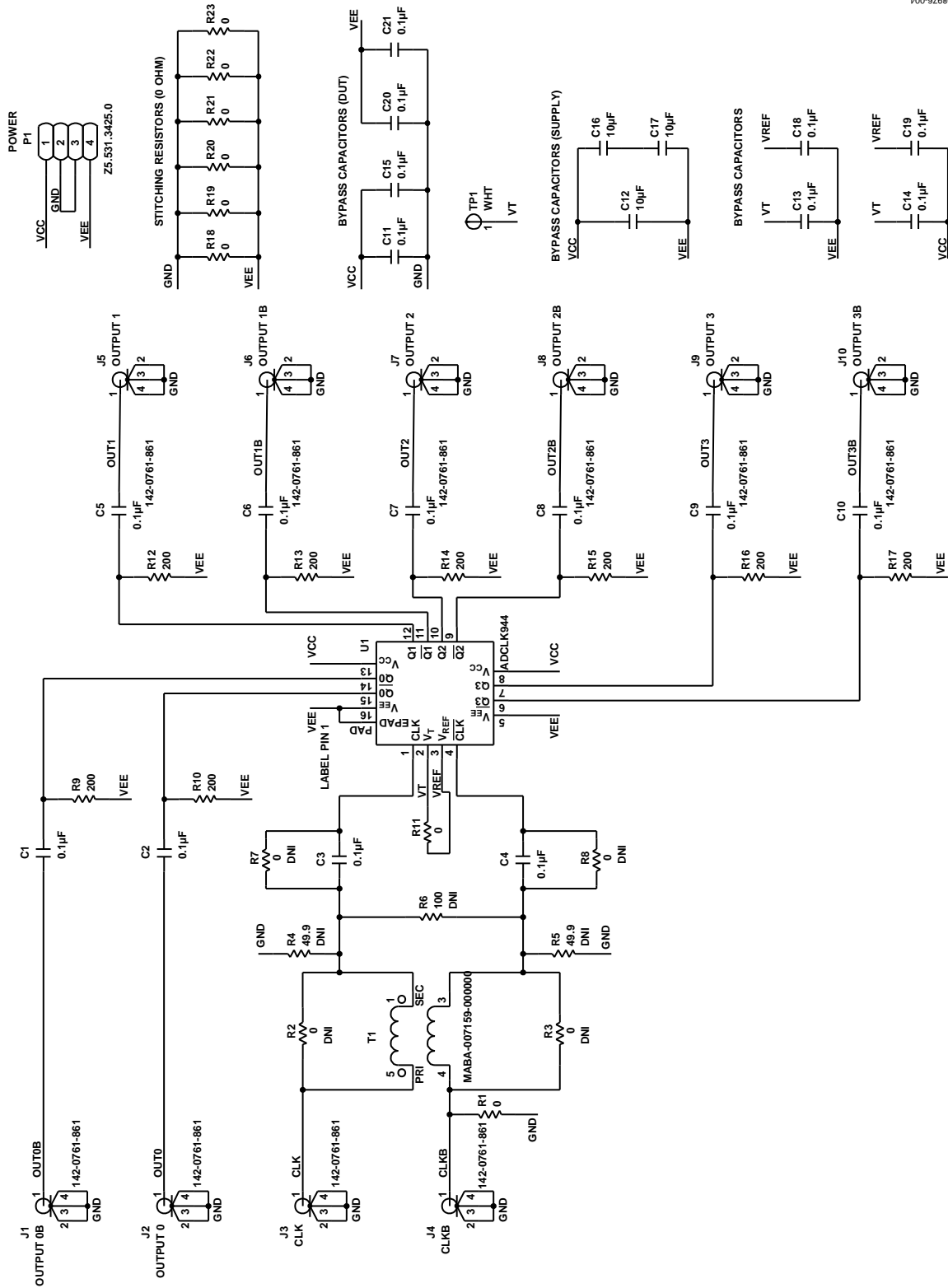
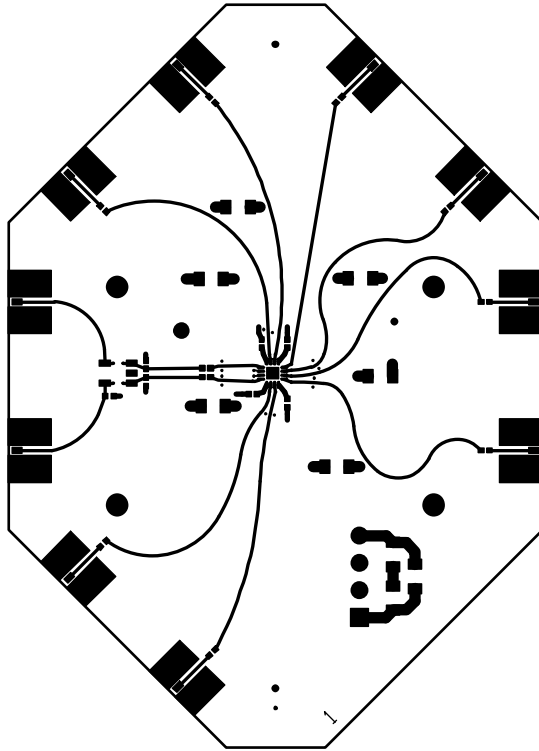
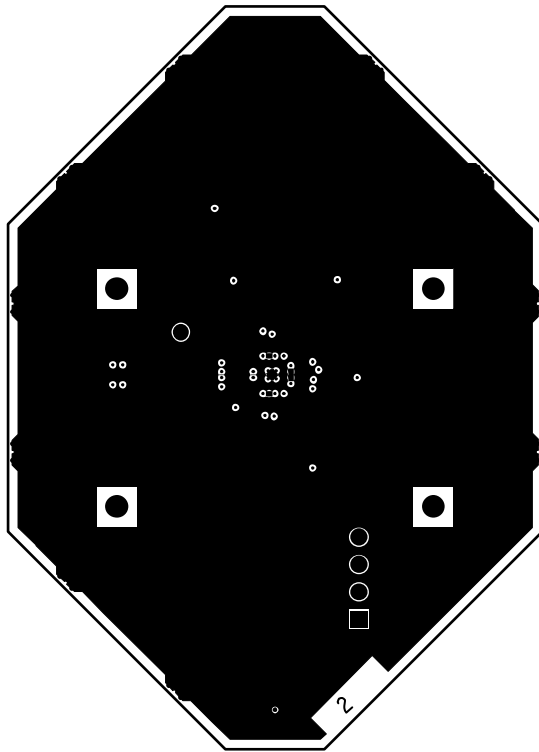


Figure 4. ADCLK944 Evaluation Board Schematic



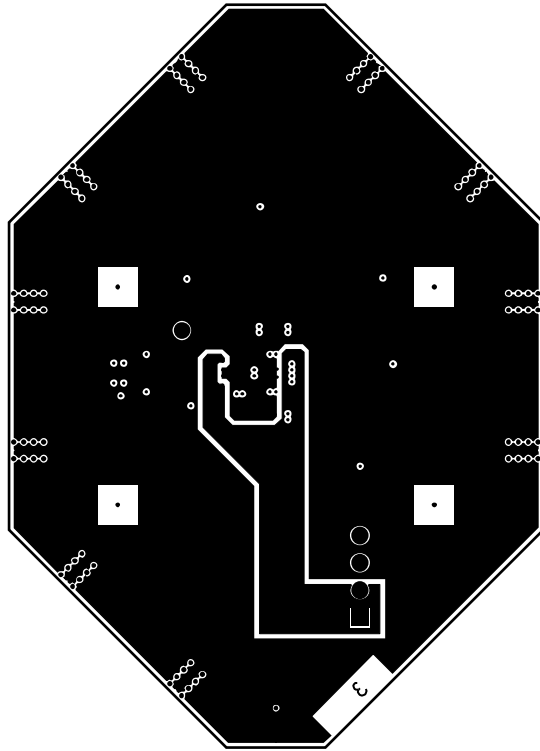
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Figure 5. Top Trace Layer



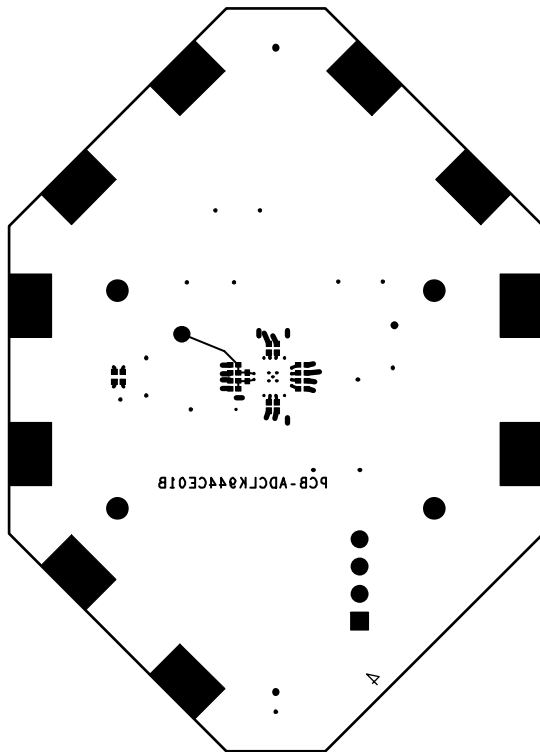
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Figure 6. Ground Plane Layer



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Figure 7.  $V_{CC}$  and  $V_{EE}$  Power Plane Layer



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Figure 8. Bottom Trace Layer

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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