Evaluation Board for Dual High Speed Op Amps
Offered in 16-Lead 3 mm × 3 mm LFCSP

FEATURES
Enables quick breadboarding/prototyping
User-defined circuit configuration
Edge-mounted SMA connector provisions
Easy connection to test equipment and other circuits
RoHS compliant

GENERAL DESCRIPTION
The Analog Devices, Inc., 16-lead LFCSP evaluation board is designed to help users evaluate dual high speed op amps offered in 16-lead, 3 mm × 3 mm LFCSP packages. The evaluation board is a bare board (that is, there are no components or amplifier soldered to the board; these must be ordered separately) that enables users to quickly prototype a variety of dual op amp circuits, which minimizes risk and reduces time to market. Figure 1 and Figure 2 show the bare evaluation board component and circuit sides.

The evaluation board is a 2-layer PCB that accepts SMA edge mounted connectors on the inputs and outputs for efficient connection to test equipment or other circuitry. The ground plane, component placement, and supply bypassing are designed to minimize parasitic inductances and capacitances. The evaluation board components are primarily SMT 0805 case size, with the exception of the electrolytic bypass capacitors (C1 and C2), which are 3528 case size.

Figure 3 shows the evaluation board schematic. The evaluation board assembly drawings and layout patterns are shown in Figure 4 through Figure 7.
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REVISION HISTORY
6/11—Rev. 0 to Rev. A
Changes to Features and General Descriptions Sections .......... 1
Changes to Figure 1 ..................................................................................... 1
Added Figure 2 ............................................................................................ 1
Changes to Evaluation Board Schematic, Assembly Drawings,
and Layout Patterns .................................................................................... 3
Added Ordering Information Section ....................................................... 6
2/10—Revision 0: Initial Version
Figure 3. Evaluation Board Schematic
Figure 4. Assembly Drawing, Component Side

Figure 5. Assembly Drawing, Circuit Side
Figure 6. Layout Pattern, Component Side

Figure 7. Layout Pattern, Circuit Side
### ORDERING INFORMATION

#### BILL OF MATERIALS

Table 1.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>+VS, −VS, GND1, GND2, GND3, GND4, PD1, PD2</td>
<td>Test point</td>
<td>TP</td>
</tr>
<tr>
<td>2</td>
<td>C1, C2</td>
<td>10 µF capacitor</td>
<td>3528</td>
</tr>
<tr>
<td>4</td>
<td>C3, C4, C5, C6</td>
<td>Capacitor, user defined</td>
<td>C0805</td>
</tr>
<tr>
<td>1</td>
<td>DUT</td>
<td>DEV, QFN16_3x3</td>
<td>16-lead LFCSP</td>
</tr>
<tr>
<td>6</td>
<td>+IN1, +IN2, −IN1, −IN2, OUT1, OUT2</td>
<td>SMA/SMT</td>
<td>SMA/SMT</td>
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<tr>
<td>21</td>
<td>R1 to R21</td>
<td>Resistor, user defined</td>
<td>R0805</td>
</tr>
</tbody>
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NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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