EVAL-ADGM1304EBZ User Guide

UG-644

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Evaluating the ADGM1304 0 Hz/DC to 14 GHz, Single-Pole, Four-Throw MEMS Switch with Integrated Driver

FEATURES

Supply voltage: single 3.3 V
Wide frequency range
High power handling capability: 36 dBm
SMA connectors for RF signals
SMB connectors for switch control signals
On-board CALIBRATION THRU transmission line for analyzer calibration

GENERAL DESCRIPTION

This user guide describes the EVAL-ADGM1304EBZ evaluation board for the ADGM1304, a dual-chip, radio frequency (RF) switching solution containing a single-pole, four-throw (SP4T), microelectromechanical systems (MEMS) switch and a control chip copackaged in a compact, 5 mm × 4 mm, LFCSP package. The SP4T switch uses Analog Devices, Inc., MEMS switch technology, providing optimum performance in terms of bandwidth, power handling capability, and linearity for RF applications. The control chip generates the high voltage signals needed for the MEMS switch and allows the user to control its operation through a simple and flexible complementary metal-oxide semiconductor(CMOS)-/low voltage transistor-transistor logic (LVTTL)-compliant parallel interface.

The EVAL-ADGM1304EBZ comes fitted with connectors for RF and control signals as well as links to allow the user to control the operation of the switch and evaluate its performance.

For full details on the ADGM1304, see the ADGM1304 data sheet, which should be consulted in conjunction with this user guide when using these evaluation boards.

EVAL-ADGM1304EBZ CONNECTION DIAGRAM

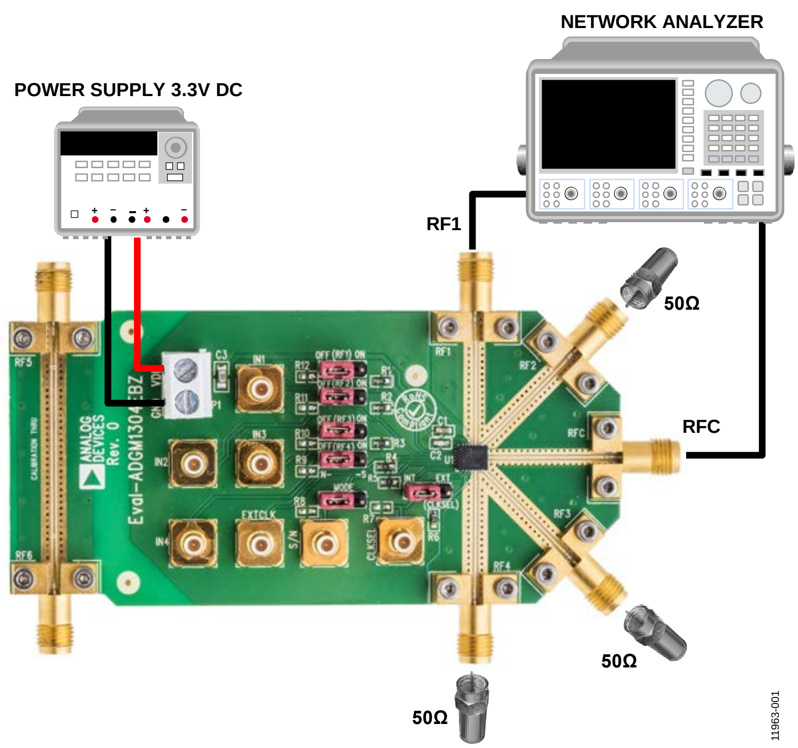

Figure 1.

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REVISION HISTORY

10/2016—Revision A: Initial Version

EVALUATION BOARD HARDWARE

The ADGM1304 evaluation kit contains a fully fitted, printed circuit board (PCB).

The EVAL-ADGM1304EBZ evaluation board allows the user to connect RF signals to the MEMS switch. The user controls the switch operation using the on-board links, or by applying the correct control signals to the appropriate connectors.

The EVAL-ADGM1304EBZ provides an additional transmission line to facilitate the calibration of the network analyzer to minimize the effects of the PCB tracks that connect the RF signals to the MEMS switch. This user guide describes the calibration process in the Network Analyzer Calibration Procedure section.

POWER SUPPLY

To operate the EVAL-ADGM1304EBZ, the user must provide an external power supply connected to the power block, P1. The supply voltage is 3.3 V and must be positive with respect to the ground of the PCB. The ground of the PCB is marked with GND on the silkscreen near P1 (see Figure 11).

RF CONNECTORS

The SMA edge connectors on the EVAL-ADGM1304EBZ (RF1 to RF4 and RFC) connect to each switch in the ADGM1304 for performance evaluation purposes. The RF5 and RF6 connectors connect to a transmission line to estimate the loss associated with the PCB (see the Measurement section). Table 1 describes the RF connectors to the ADGM1304.

Table 1. RF Connectors Connection to the ADGM1304

Connector	Description
RF1	Port RF1 of the ADGM1304
RF2	Port RF2 of the ADGM1304
RF3	Port RF3 of the ADGM1304
RF4	Port RF4 of the ADGM1304
RFC	Common RF port of the ADGM1304
RF5, RF6	CALIBRATION THRU transmission lines used for calibration

SWITCH CONTROL CONNECTORS

The control IC packaged with the MEMS switch internally generates the voltage signal required to drive the switch. To operate, the internal control IC contains a reference clock signal at a nominal 11 MHz. The ADGM1304 chip provides the user with the option to choose between using an internal oscillator operating at a nominal frequency of 11 MHz and an external clock signal supplied by the user with a frequency range from 20 MHz to 23 MHz using the CLKSEL and EXTCLK pins. See the CLKSEL and EXTCLK section for information on configuring the device to use an external clock signal.

The ADGM1304 comes with a standard LVTTL parallel interface consisting of five inputs: IN1 to IN4 and SLEEP. The logic level applied to the IN1 through IN4 inputs controls the state of the MEMS switches, and the logic level applied to the SLEEP input sets the operation mode of the ADGM1304. When SLEEP is set to high, the ADGM1304 enters sleep mode, a low power state that reduces the current drawn by the device to only 1 µA. To set the ADGM1304 to normal operation mode, set the SLEEP pin to low.

CLKSEL and EXTCLK

The CLKSEL pin controls the reference clock signal used by the ADGM1304. The logic level to this pin can be set by using the CLKSEL link or by applying an external signal to the CLKSEL SMB connector (see Table 2).

Table 2. CLKSEL Link and CLKSEL SMB Connector Settings

Position	Reference Clock Setting
EXT	External reference clock (supplied by user)
Removed	Controlled via CLKSEL SMB
	High equals external
	Low equals the internal 11 MHz clock
	No signal equals the internal 11 MHz clock
INT (Default Setting)	Internal reference clock

When the ADGM1304 is set to use an external reference clock (see Table 2), apply a clock signal to the EXTCLK SMB connector.

RF1, RF2, RF3, and RF4 Mode

The IN1 to IN4 and SLEEP input pins control the switch state and operation mode of the ADGM1304. The EVAL-ADGM1304EBZ allows the user to control these pins using the RF1 to RF4 links or by applying external signals to the SMB connectors, IN1 to IN4 and S/N, respectively (see Table 3 and Table 4).

Table 3. Link Mode and S/N SMB Connector Settings

Position	ADGM1304 Operation Mode
S	Sleep mode
Removed	Controlled via S/N SMB
	High equals sleep mode
	Low equals normal mode
N (Default Setting)	Normal mode

Table 4. (RF1) to (RF4) Links and IN1 to IN4 SMB Connector Settings

Link Name	Controlled RF Switch	Link Position	RF Switch Status[1]
(RF1)	RF1 to RFC	Removed	Controlled via IN1 SMB High equals on Low equals off
		On	On
		Off (default setting)	Off
(RF2)	RF2 to RFC	Removed	Controlled via IN2 SMB High equals on Low equals off On Off
(RF3)	RF3 to RFC	Removed (default setting)	Controlled via IN3 SMB High equals on Low equals off
		On	On
		Off (default setting)	Off
(RF4)	RF4 to RFC	Removed (default setting)	Controlled via IN4 SMB High equals on Low equals off
		On	On
		Off (default setting)	Off

[1] The RFx switch status is valid only when the ADGM1304 is in normal operation mode. When the device is in sleep mode, all RFx switches are off.

MEASUREMENT

Figure 1 shows the EVAL-ADGM1304EBZ evaluation board of the ADGM1304. Apply a V_{DD} to the board to measure the performance of the switch. The links are set according to the switch under test (see Table 4). After selecting the desired channel and its state, a network analyzer can collect the switch performance data. Terminate the RF edge connectors of unused switch channels into 50 Ω loads to achieve the full performance of the channel under test.

The EVAL-ADGM1304EBZ shown in Figure 1 comes with a calibration transmission line (CALIBRATION THRU) on the PCB. The purpose of this calibration line is to remove the insertion loss and phase offset of the PCB transmission lines connecting to the switch from the measurement. Figure 2 shows the calibration line and its insertion loss and return loss up to 16 GHz. The calibration line is exactly the same length as the distance from any one RFx connector to the switch pin, plus the distance from the RFC connector to the switch pin. Figure 3 illustrates the definition of the calibration line length. All RF traces connecting to the ADGM1304 are of equal length.

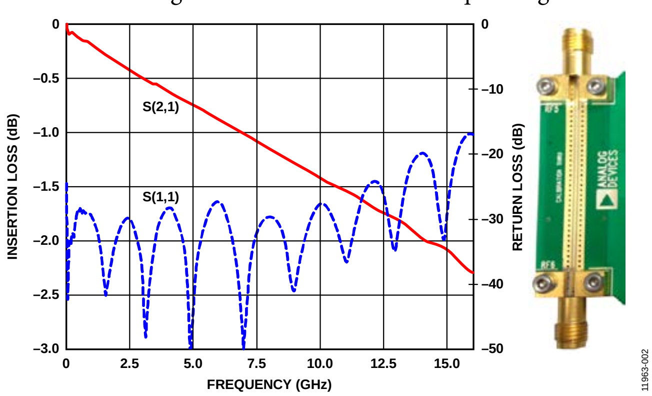

Figure 2. EVAL-ADGM1304EBZ Evaluation Board Calibration Transmission Line Used for PCB Insertion Loss and Phase Offset Correction

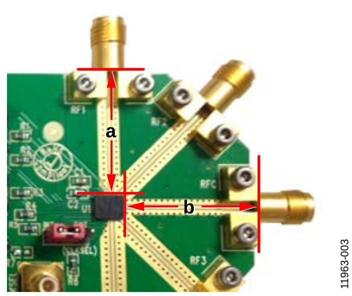

Figure 3. Calibration Transmission Line Length Equal to a + b

To deembed the PCB transmission line insertion loss from the entire switch insertion loss board measurement (RF1 to RFC path), the measurement S(2,1) data must be divided by the |S(2,1)| of the CALIBRATION THRU. Perform this deembedding by using the network analyzer at the time of the measurement or after the measurement using individual measurement data files. Refer to the Network Analyzer Calibration Procedure section for more information.

Use the network analyzer port extension function to deembed the phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct for phase. Enter the time delays into the port extension menu on the network analyzer that correspond to the phase offset introduced from an RF edge connector to the switch pin. Figure 3 shows an example of these phase offsets on a typical switch measurement, labeled as a and b. Both a and b are identical in length and can be calculated by measuring the time delay of the calibration line and dividing it by two.

Figure 4 shows the ADGM1304 switch insertion loss (network analyzer two-port S(2,1) measurement) measurement results that were deembedded with respect to the PCB transmission line losses. The blue trace is the RF2 to RFC switch channel, and the red trace is the RF1 to RFC switch channel. The dashed traces are the respective return loss traces. The performance of the RF2 switch is identical to RF3, and the RF1 switch is identical to RF4.

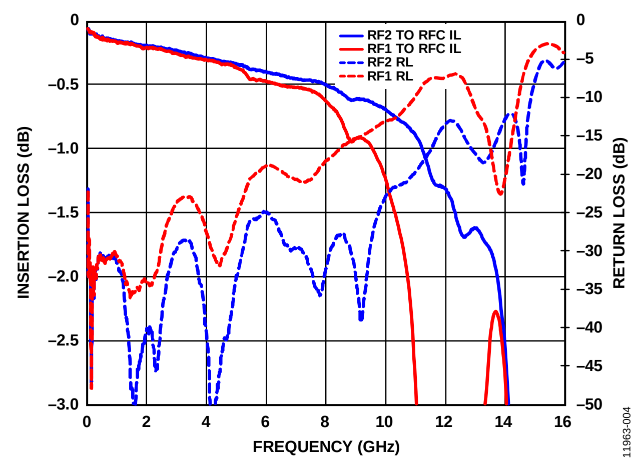

Figure 4. PCB Deembedded ADGM1304 Insertion Loss Performance (Blue = RF2 to RFC Channel, Red = RF1 to RFC Channel)

Figure 5 shows the ADGM1304 switch off-isolation performance measurement results for two channels. The blue trace is the RF2 to RFC switch channel, and the red trace is the RF1 to RFC switch channel. As with insertion loss, the performance of the RF2 switch is identical to RF3, and the RF1 switch is identical to RF4.

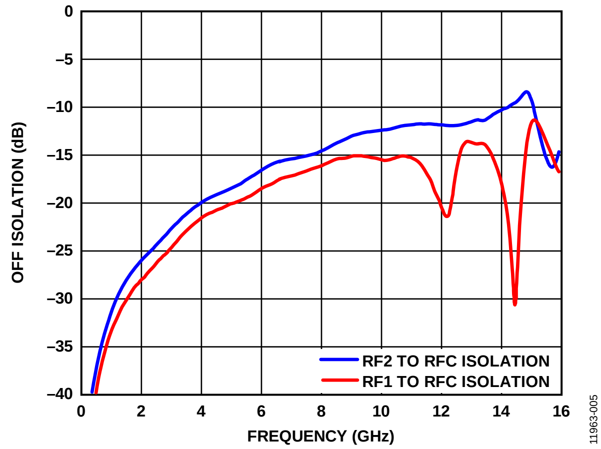

Figure 5. ADGM1304 Off-Isolation Performance (Blue = RF2 to RFC Channel, and Red = RF1 to RFC Channel)

NETWORK ANALYZER CALIBRATION PROCEDURE

Use the following procedure in conjunction with the EVAL-ADGM1304EBZ evaluation board for two-port measurements; assuming that the user has a set of manual calibration standards or an electric calibration (ECal) type unit to perform a SLOT calibration of the network analyzer. The maximum value for the network analyzer frequency sweep for the EVAL-ADGM1304EBZ PCB can be up to 16 GHz.

1. Perform a full, two-port standard short, load, open, through (SLOT) calibration of the network analyzer.
2. Connect the CALIBRATION THRU calibration line (Connector RF5 and Connector RF6) to the analyzer and measure its insertion loss S(2, 1).
3. Save the measured data to the network analyzer memory to later use.
4. Configure the EVAL-ADGM1304EBZ links and power up the EVAL-ADGM1304EBZ with a 3.3 V dc power supply.
5. Connect the network analyzer to the desired MEMS switch RF connectors and apply the external control signals, if needed.
6. Measure the complete insertion loss of the EVAL-ADGM1304EBZ. Include the insertion loss of the MEMS switch and test fixture (PCB transmission lines and RF connectors).
7. Deembed the PCB losses from the complete evaluation board measurement using the data saved at Step 3 and the measured data at Step 6. Because the extraction method is dependent on the network analyzer used, consult the network analyzer user manual before performing the extraction. Typically, the divide function is used to divide the complete S(2, 1) measurement data by the CALIBRATION THRU line S(2, 1) data stored in memory.
8. Use the network analyzer port extension function to deembed the phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct for phase. Enter the time delay values into the port extension menu on the network analyzer for each RF edged connector to switch the pin path equal to the electrical length of the calibration line divided by two.

EVALUATION BOARD SCHEMATIC AND ARTWORK

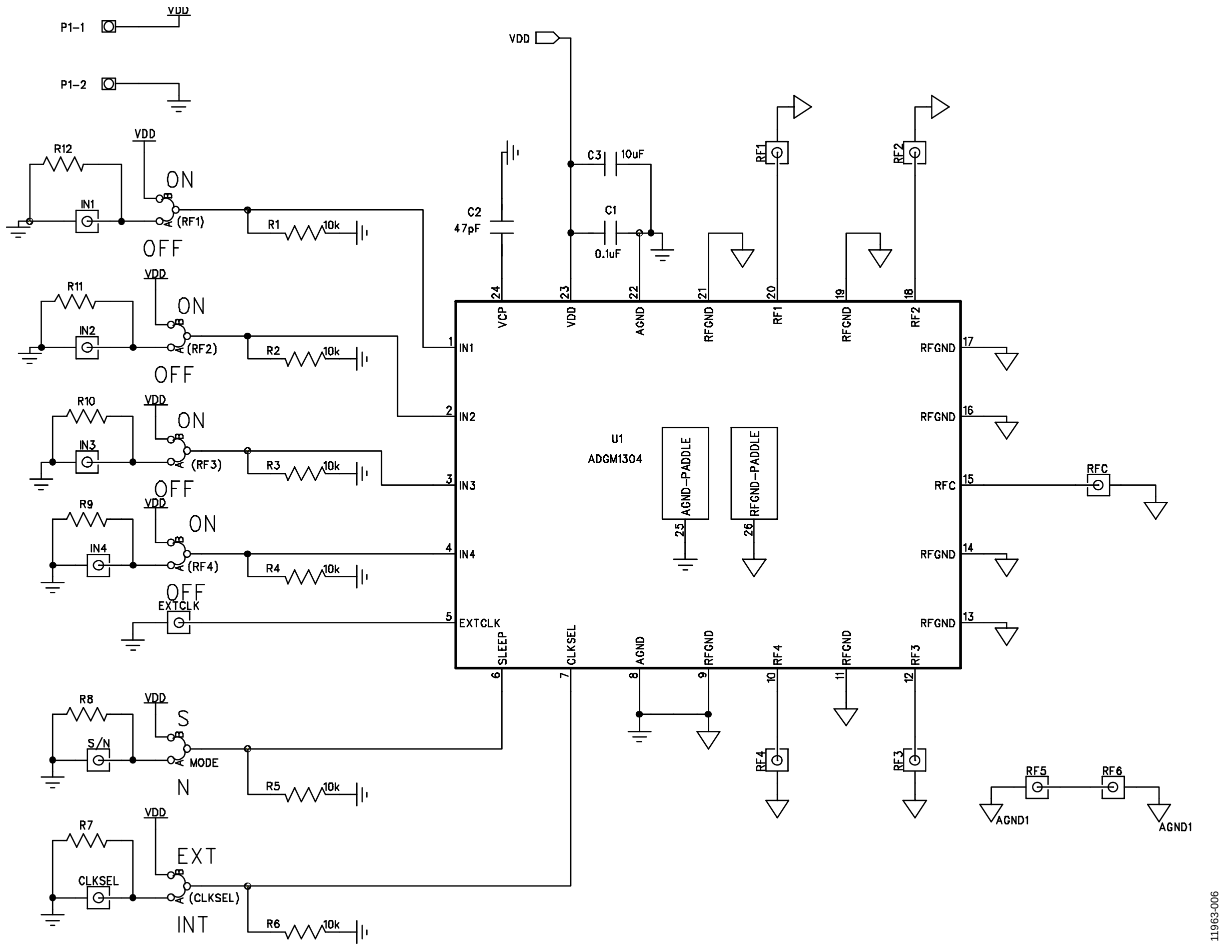

Figure 6. Schematic of the EVAL-ADGM1304EBZ

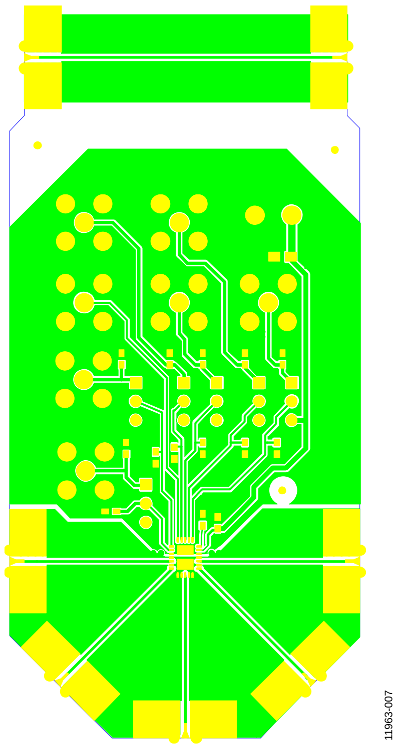

Figure 7. EVAL-ADGM1304EBZ Component Side PCB Drawing (Layer 1)

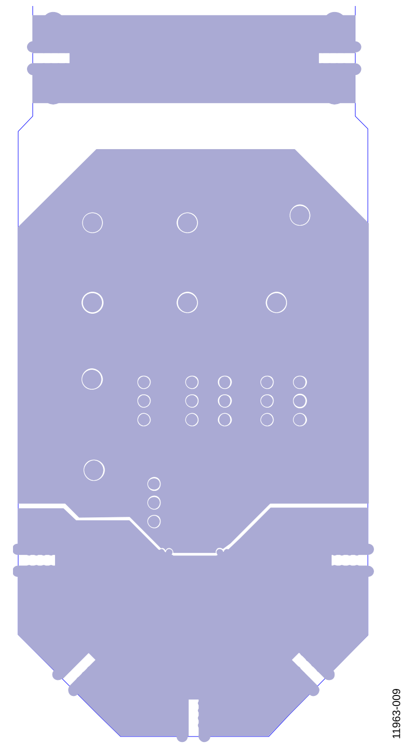

Figure 9. EVAL-ADGM1304EBZ Component Side Ground Plane PCB Drawing (Layer 3)

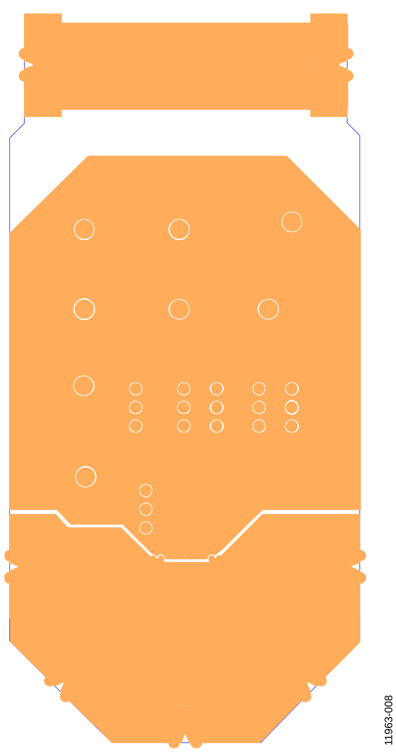

Figure 8. EVAL-ADGM1304EBZ Component Side Ground Plane PCB Drawing (Layer 2)

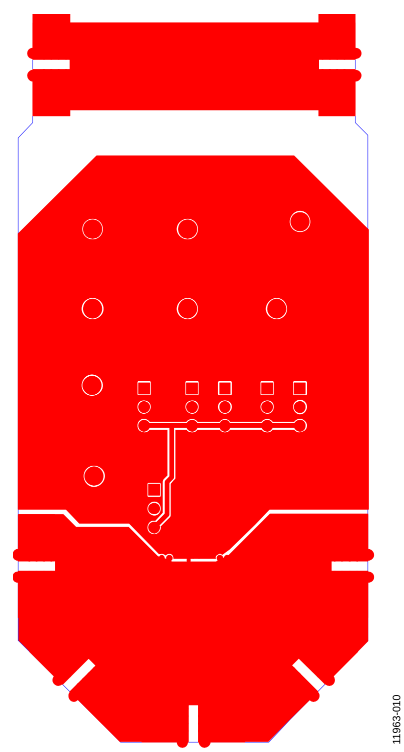

Figure 10. EVAL-ADGM1304EBZ Component Side, Bottom Side PCB Drawing (Layer 4)

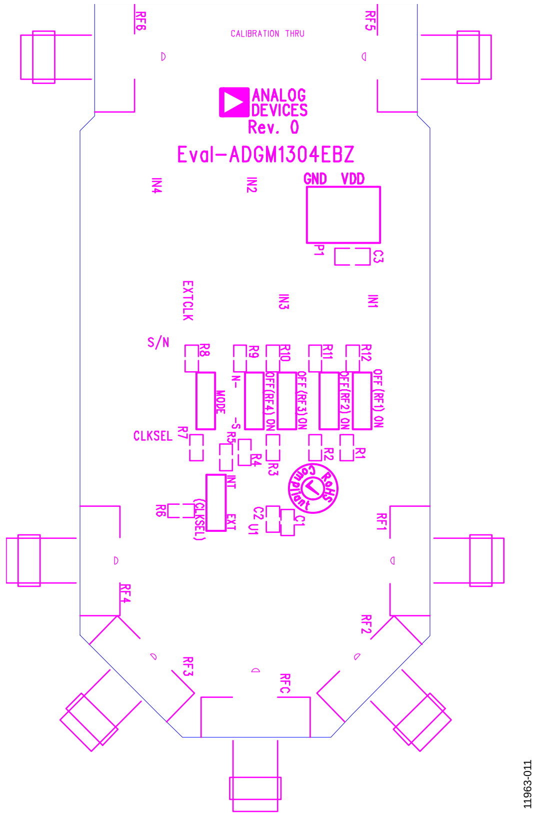

Figure 11. EVAL-ADGM1304EBZ Component Side Silkscreen PCB Drawing (Top)

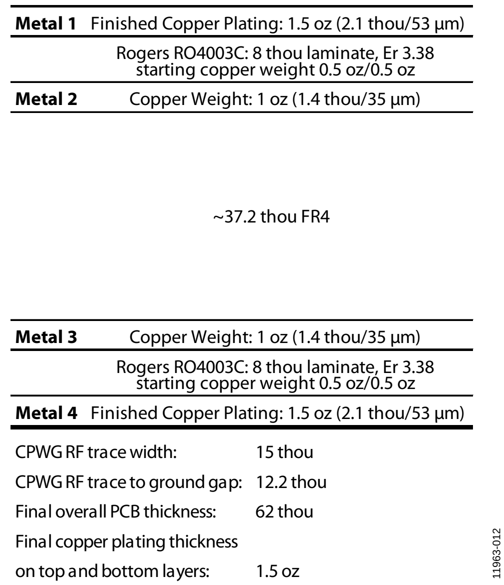

Figure 12. EVAL-ADGM1304EBZ PCB Stack Up with Coplanar Waveguide with Ground (CPWG) Dimensions

ORDERING INFORMATION

Table 5. Bill of Materials

Quantity	Reference Designator	Description	Supplier/Number
1	C1	0.1 µF, 0603 package, 16 V, X7R, SMD ceramic capacitor	FEC 940-6140
1	C2	47 pF, 0603 package, 100 V, C0G/NP0 capacitor	Digi-Key 478-1144-1-ND
1	C3	10 µF, 0805 package, 10 V, X5R, SMD ceramic capacitor	FEC 940-2136
7	CLKSEL, EXTCLK, IN1 to IN4, S/N	50 Ω SMB connector through holes	FEC 111-1349
6	(RF1) to (RF4), MODE, (CLKSEL)	3-pin SIL headers and shorting links	FEC 102-2248 and FEC 150-411
1	P1	2-pin terminal block (5 mm pitch)	FEC 151-785
6	R1 to R6	10 kΩ (0603 package) SMD resistors	FEC 933-0399
6	R7 to R12	Not populated	
9	RF1 to RF6, RFC	50 Ω side launch SMA connectors	Rosenberger 32K243-40ML5
1	U1	ADGM1304, 0 Hz/dc to 14 GHz, single-pole, four-throw MEMS switch with integrated driver	Analog Devices
3	Not applicable[1]	Wideband 50 Ω termination SMA loads	Pasternack PE6081

[1] Screwed on at measurement time (see Figure 1).

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