ANALOG DEVICES

EVAL-ADG5436FEBZ User Guide
UG-871

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Evaluation Board for the ADG5436F, Overvoltage Protected Dual SPDT Switch

FEATURES

- Supply voltages
  - Dual supply: ±5 V to ±22 V
  - Single supply: 8 V to 44 V
- Protected against overvoltage on source pins
  - Signal voltages up to −55 V and +55 V
- LED for visual overvoltage indication
- Parallel interface compatible with 3 V logic
- On-board LDO regulator for digital supply and control, if required

EVALUATION KIT CONTENTS

EVAL-ADG5436FEBZ evaluation board

DOCUMENTS NEEDED

ADG5436F data sheet
EVAL-ADG5436FEBZ user guide

EQUIPMENT NEEDED

- DC voltage source
  - ±22 V for dual supply
  - 44 V for single supply
- Optional digital voltage source: 3 V to 5 V
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION

The EVAL-ADG5436FEBZ is the evaluation board for the ADG5436F, which features two independently controlled single-pole/double-throw (SPDT) switches. The ADG5436F has overvoltage detection and protection circuitry on the source pins and is protected against signals up to −55 V and +55 V in both the powered and unpowered states.

Figure 1 shows the EVAL-ADG5436FEBZ in a typical evaluation setup. The ADG5436F is soldered to the center of the evaluation board and screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device with a fourth terminal that provides a user defined digital voltage if required. Alternatively, a low dropout (LDO) regulator is provided for 5 V digital voltage control and to supply the LED, which is mounted to provide visual indication of the fault status of the switch.

Full specifications on the ADG5436F are available in the product data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

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REVISION HISTORY

9/15—Revision 0: Initial Version

EVALUATION BOARD CONNECTION DIAGRAM

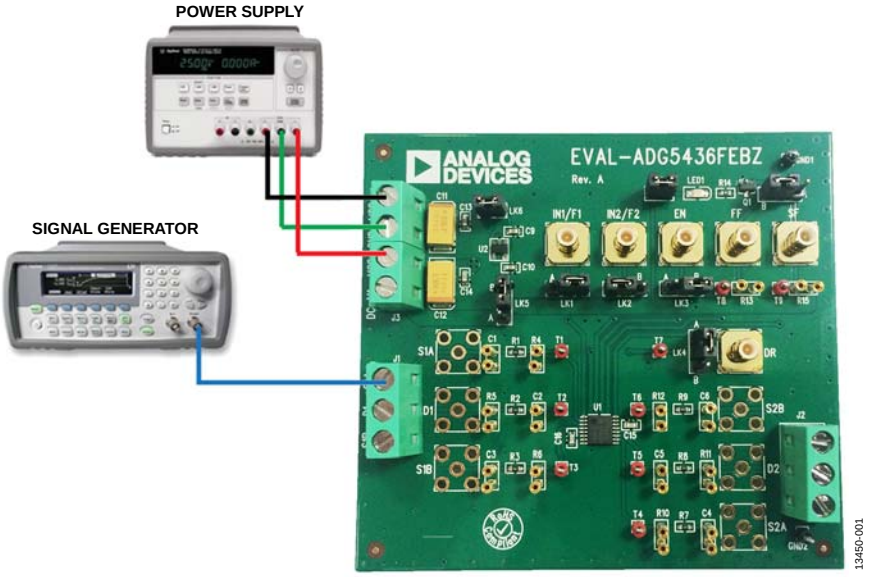

Figure 1. EVAL-ADG5436FEBZ (on the Right), Power Supply, and Signal Generator

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG5436FEBZ board is designed to operate independently and does not require any additional evaluation boards or software. An on-board LDO regulator is provided for digital control and supply voltage.

Supply the evaluation board with a dual supply power source of up to ±22 V or a single supply power source of up to 44 V. For single supply operation, connect V_{SS} to GND using Connector J3.

Set up a simple functionality test as follows:

1. Connect a power supply to Connector J3. For single supply operation, connect V_{SS} to GND using Connector J3.
2. Insert the header for LK6 to use the on-board LDO regulator and place the header for LK5 to Position B.
3. LK1 to LK3 control the digital signals for each switch on the ADG5436F.
4. In Position A, the switch is open (off).
5. In Position B, the switches SxA are closed (on) and has a resistance of approximately 10 Ω. The switches SxB are open (off).

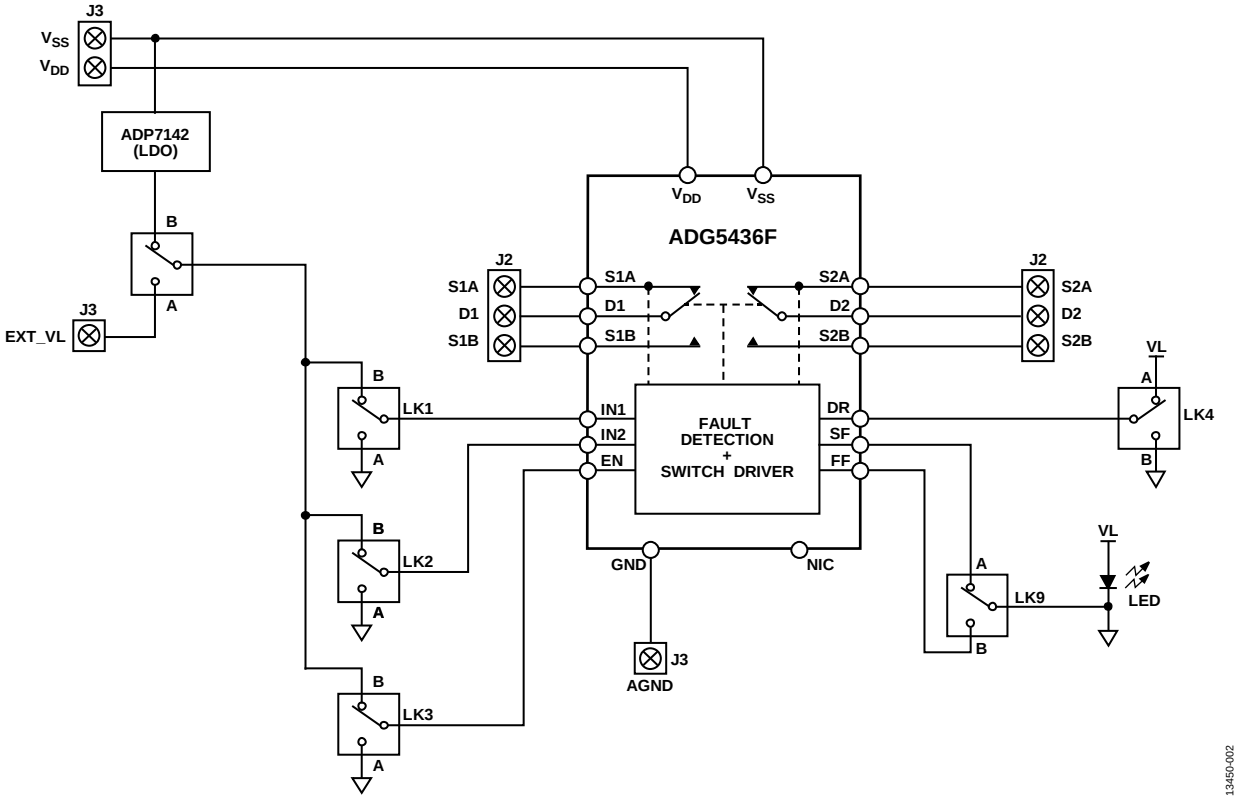

Figure 2. EVAL-ADG5436FEBZ Block Diagram

EVALUATION BOARD HARDWARE

The operation of the ADG5436F is evaluated using the EVAL-ADG5436FEBZ. Figure 1 shows a typical setup where only a power supply and signal generator are required. Figure 2 shows a block diagram of the main components of the evaluation board.

The connectors on the board pass signals through the ADG5436F switch. The source pins have fault detection circuitry that reacts to an overvoltage. During an overvoltage event, the switch turns off and the FF pin pulls low. When an overvoltage event occurs on the selected source of A0/F0, A1/F1, or EN/F2, the SF pin pulls low. See the ADG5436F data sheet for further details.

POWER SUPPLY

Connector J3 provides access to the supply pins of the ADG5436F. VDD, GND, and VSS link to the appropriate pins of the ADG5436F. For dual supply voltages, power the evaluation boards from ±5 V to ±22 V. For single supply voltages, connect the GND and VSS terminals and power the evaluation board with 8 V to 44 V. Additionally, an on-board LDO regulator is provided for digital control voltage. If necessary, connect a secondary voltage source to DC_V1 and use it as the digital control voltage. To use DC_V1, place the header of LK5 into Position A.

INPUT SIGNALS

Two screw connectors are provided to connect both the source and drain pins of the ADG5436F. Additional subminiature Version V (SMB) connector pads are provided if extra connections are required.

The ADG5436F is overvoltage protected on the source side and the maximum voltage that can be applied to SxA and SxB is −55 V or +55 V. See the ADG5436F data sheet for more details.

Each trace on the source and drain side includes two sets of gold pin connectors that place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. Use the resistor combined with the gold pin connectors to create a simple resistor/capacitor (RC) filter.

The ADG5436F uses parallel interface channels (IN1/F1 and IN2/F2) to control the operation of the switches. Use the headers on LK1 to LK3 to manually control the operation of the switches, or connect an external controller directly to the control pins by using the SMB connectors, IN1/F1, IN2/F2, and EN, and remove the link headers on LK1 to LK3.

OUTPUT SIGNALS

There are two outputs on the ADG5436F. The FF pin indicates when the device is operating normally or whether there is an overvoltage fault on one of the source pins. The SF pin also indicates when an overvoltage fault occurs on one of the source pins and transitions low only when an overvoltage occurs on the channels selected by the IN1/F1 and IN2/F2 inputs. For visual indication, an LED is mounted on the evaluation board.

Use LK8 to connect the LED circuit. When the device is operating normally, the FF pin remains high and the LED turns on. If an overvoltage occurs at any of the source pins, the FF pin pulls low and the LED turns off.

The LK9 selector allows the user to choose which output controls the LED. Putting the header in Position A allows the FF pin to control the LED. In Position B, the SF pin controls the LED.

SMB connectors are provided to interface the evaluation board with external controllers, and two gold pin connectors are provided to connect a pull-up resistor between the FF and SF signals and the digital supply.

The DR pin allows the user to choose the state of the drain pin when the device is deactivated during an overvoltage event. The LK4 selector allows the user to choose between open circuit and pulling to rails.

JUMPER SETTINGS

LINK HEADERS

Use the link headers to control the ADG5436F manually, to configure the digital control voltage, and to isolate the LED from the system. Table 2 shows a summary of the link headers and how they are used on the evaluation board.

Use LK1 and LK2 to control the switches of the ADG5436F. Use LK3 to enable or disable the device.

Position A is tied to GND and sets the logic low, whereas Position B is tied to DC_V1 and sets the logic high.

Table 1. ADG5436F Truth Table

LK3 (EN)	LK1 (IN1/F1)	LK2 (IN2/F2)	ADG5436F Switch States
A	X[1]	X[1]	All switches off
B	B	B	S1A, S2A (on); S1B, S2B (off)
B	B	A	S1A, S2B (on); S1B, S2A (off)
B	A	B	S1B, S2A (on); S1BA, S2B (off)
B	A	A	S1B, S2B (on); S1A, S2A (off)

[1] X means don't care.

LK4 allows the user to configure the state of the drain during an overvoltage condition.

LK6 connects the on-board LDO regular to the V_{DD} supply. Remove the header to protect the LDO regulator from voltages higher than 28 V or to use an alternative digital control voltage. Change the header on LK5 to Position A to connect to DC_V1.

LK8 connects the LED to the digital power supply and LK9 connects the FF or SF pin of the ADG5436F to the LED.

SMB CONNECTORS

Control the parallel interface of the ADG5436F manually using the link headers of LK1 to LK3, or access the parallel interface using the SMB connectors IN1/F1, IN2/F2, and EN. To use the SMB connectors, remove the link headers of LK1 to LK3. Use the FF/SF SMB connectors to access the FF/SF digital outputs from the ADG5436F.

Table 2. Switch and 0 Ω Resistor Descriptions

Link Header	Position	Description
LK1	A	Logic 0 on IN1/F1 pin
	B	Logic 1 on IN1/F1 pin
LK2	A	Logic 0 on IN2/F2 pin
	B	Logic 1 on IN2/F2 pin
LK3	A	All switches off (disabled)
	B	Device enabled (EN pin), switch function set by the IN1/F1 and IN2/F2 pins
LK4	A	V_{DD} or V_{SS} during an overvoltage
	B	Open circuit during an overvoltage
LK5	A	DC_V1 digital voltage
	B	On-board LDO regulator digital voltage
LK6	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
LK8	Inserted	LED powered up
	Removed	LED unpowered
LK9	A	SF pin controls the LED
	B	FF pin controls the LED

EVALUATION BOARD SCHEMATICS AND ARTWORK

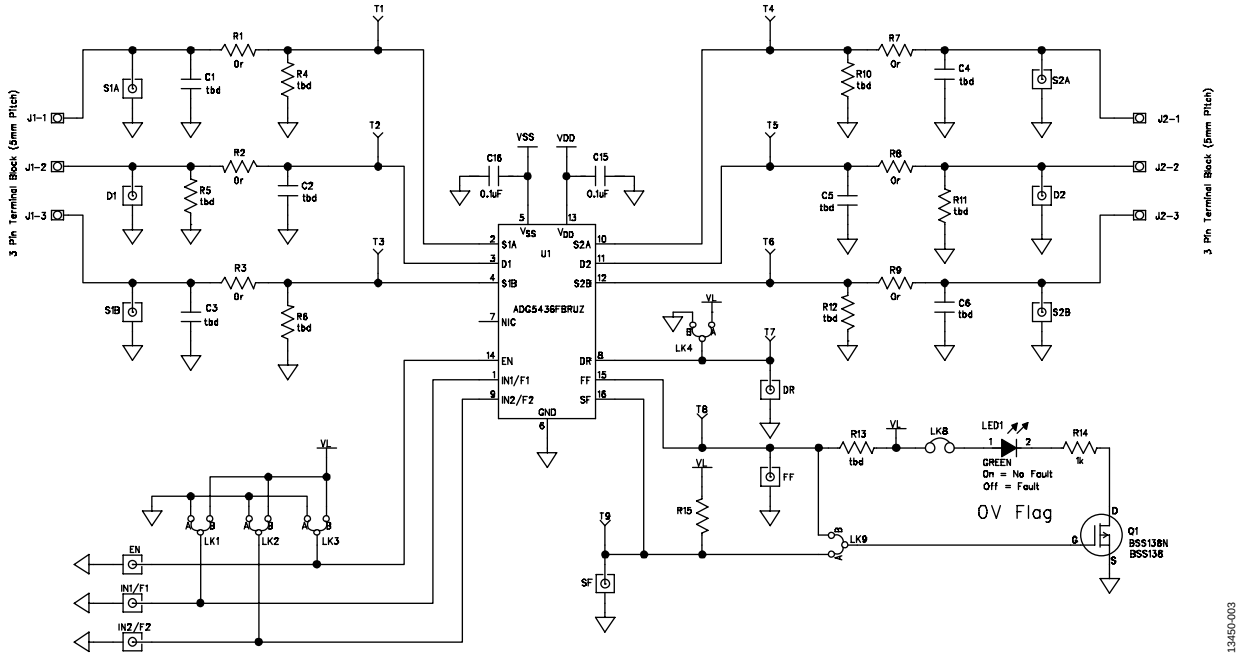

Figure 3. ADG5436F Evaluation Board Schematic (Part 1)

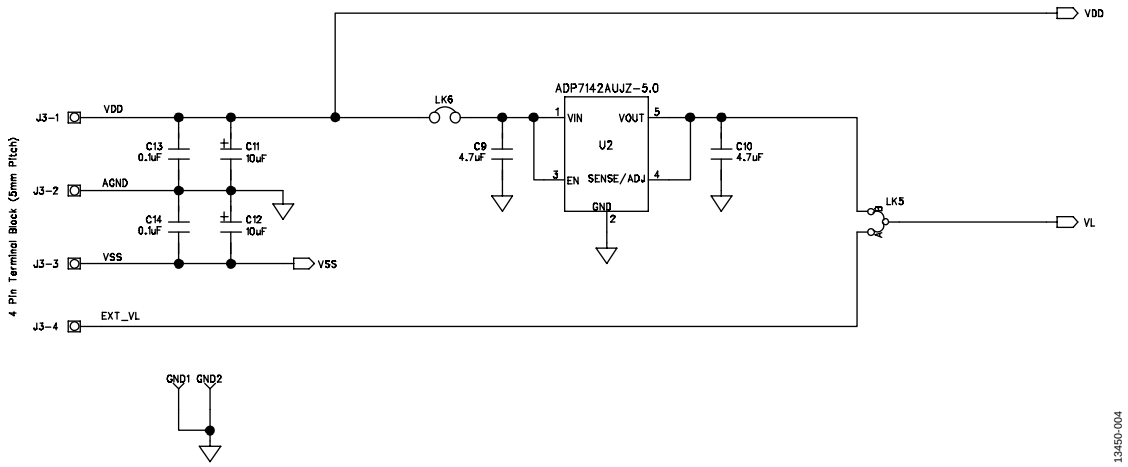

Figure 4. ADG5436F Evaluation Board Schematic (Part 2)

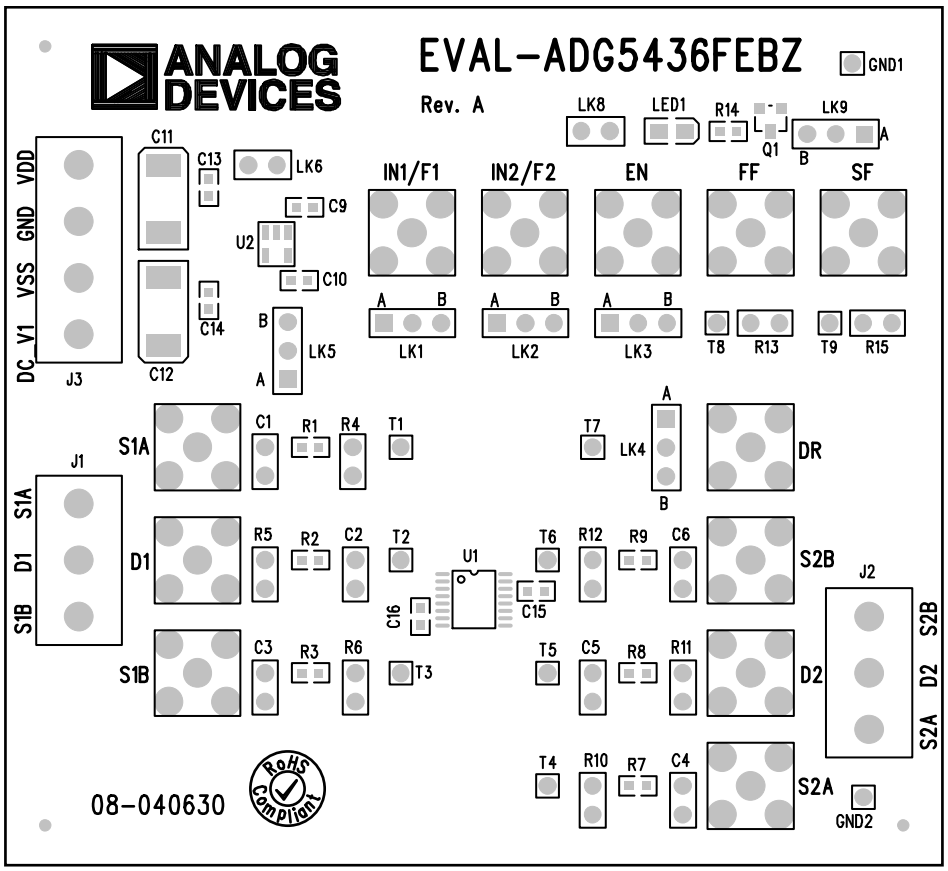

Figure 5. EVAL-ADG5436FEBZ Silk Screen

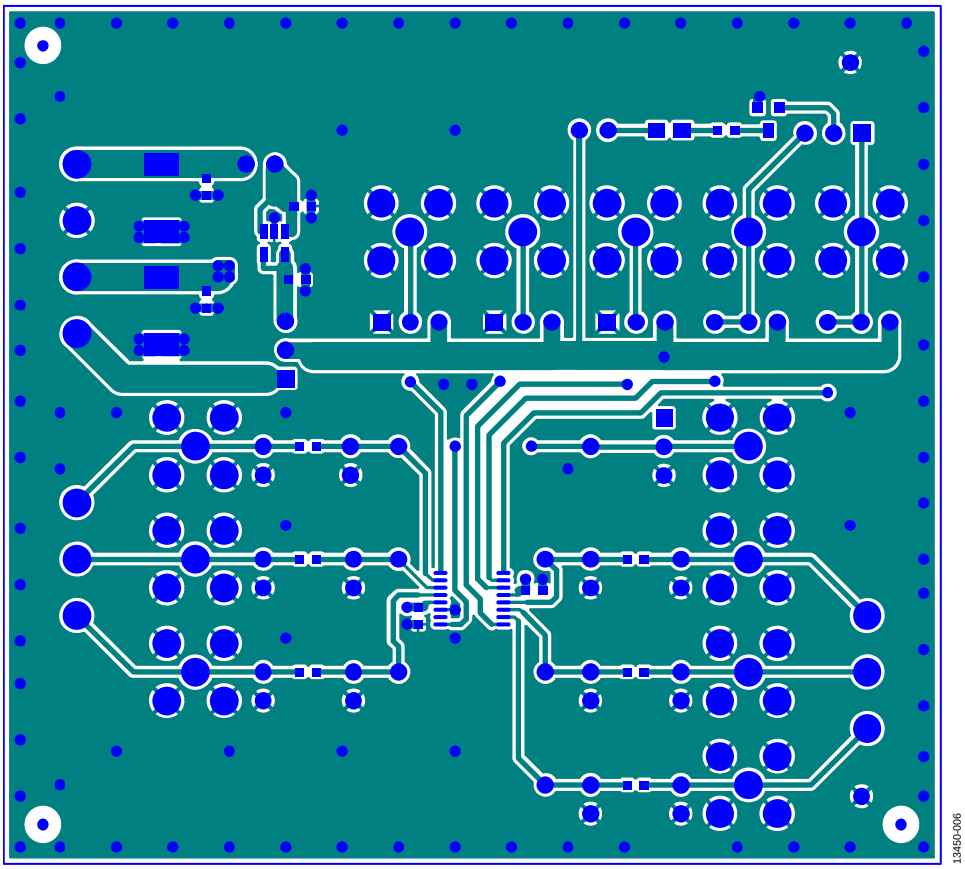

Figure 6. EVAL-ADG5436FEBZ Top Layer

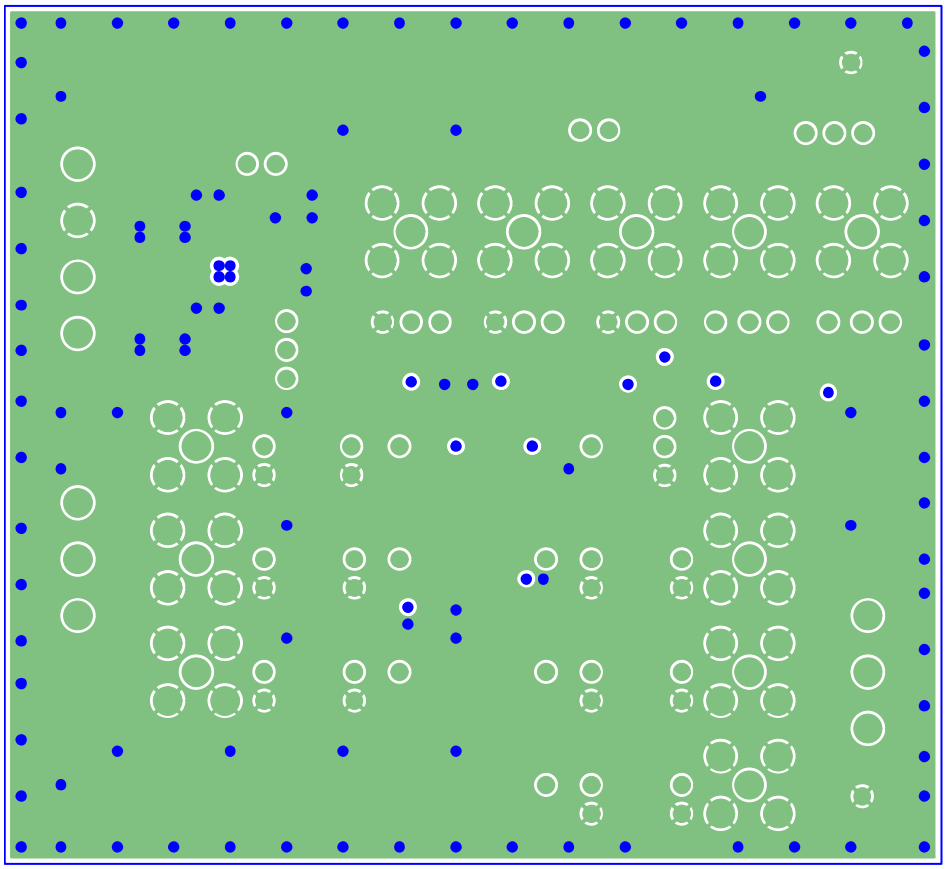

Figure 7. EVAL-ADG5436FEBZ Layer 2

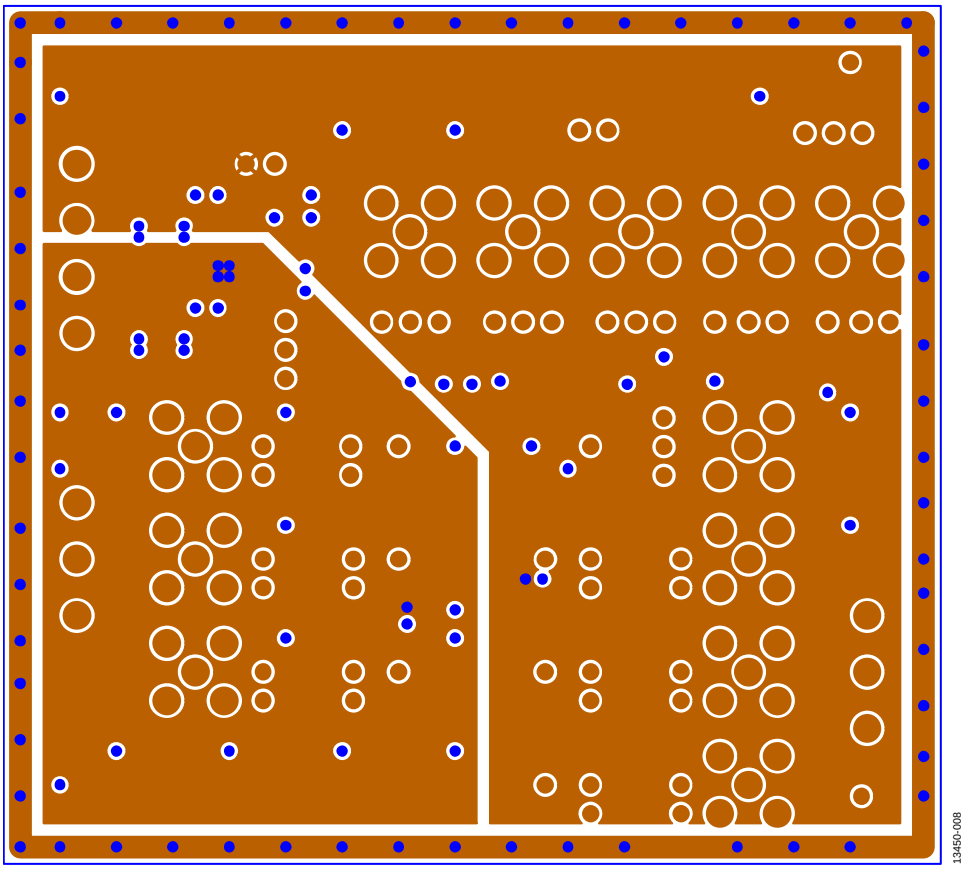

Figure 8. EVAL-ADG5436FEBZ Layer 3

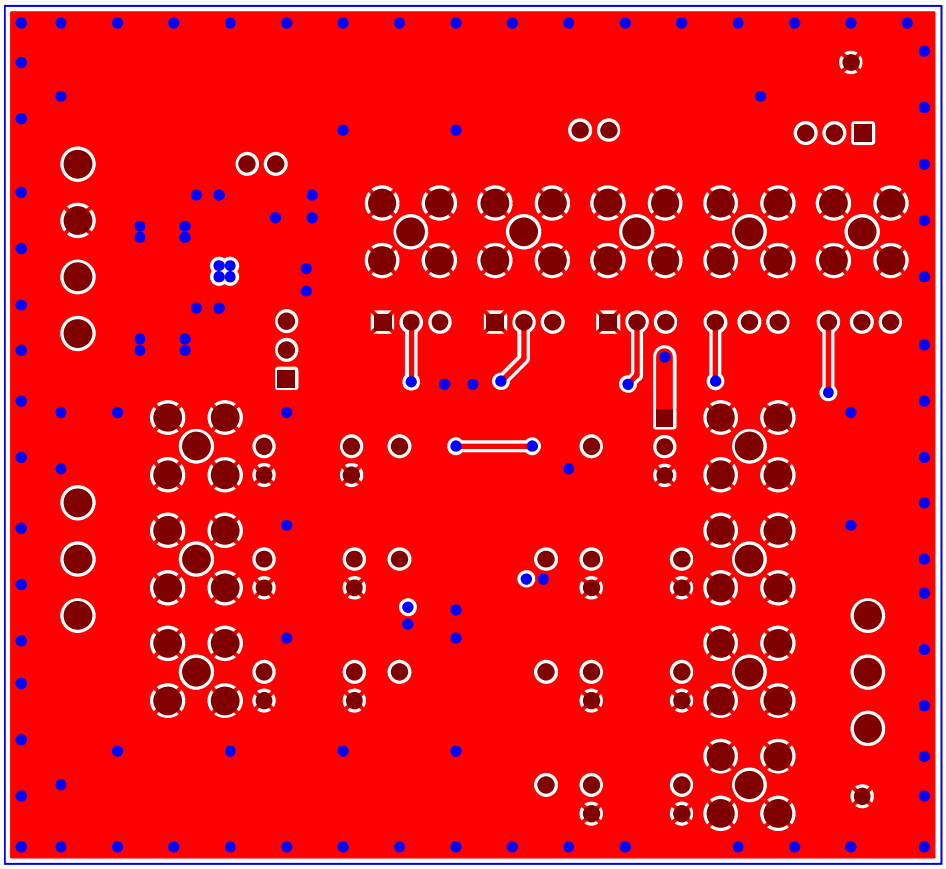

Figure 9. EVAL-ADG5436FEBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Reference Designator	Description	Part Number	Stock Code
C1 to C6	Socket pins, PCB, 2-pin only	66-3472	FEC 329563
C9, C10	Multilayer ceramic capacitors, X5R, 35 V, 0603, 4.7 µF	GRM188R6YA475KE15D	FEC 2426960
C11, C12	50 V, tantalum capacitors, D, 10 µF	TAJD106K050RNJ	FEC 143-2387
C13 to C16	50 V, X7R, multilayer ceramic capacitors, 0603, 0.1 µF	GRM188R71H104KA93D	FEC 882-0023
D1, D2, S1A, S1B, S2A, S2B	50 Ω, straight SMB sockets	SMB1251B1-3GT30G-50	Do not insert
DR, EN, FF, IN1/F1, IN2/F2, SF	50 Ω, straight SMB sockets	SMB1251B1-3GT30G-50	FEC 1111349
GND1, GND2	Black test points	20-2137	FEC 873-1128
J1, J2	3-pin terminal blocks (5 mm pitch)	CTB5000/3	FEC 151790
J3	4-pin terminal block (5 mm pitch)	CTB5000/4	FEC 151791
LED1	LED, SMD green, 0805	KP-2012SGC	FEC 1318243
LK1 to LK5, LK9	3-pin, single in line header and shorting links	M20-9990345 and M7567-05	FEC 1022248 and 150410
LK6, LK8	2-pin, 0.1" pitch, header and shorting shunts	M20-9990246	FEC 1022247 and 150-411
Q1	Transistor, N-MOSFET, 60 V, 0.23 A, SOT-23	BSS138N	FEC 115-6434
R1 to R3, R7 to R9	Resistors, 0603, 1%, 0 Ω	MC0063W06030R	FEC 9331662
R4 to R6, R10 to R13, R15	Socket pins, PCB, 2-pin only	66-3472	FEC 329563
R14	Resistor, 1 kΩ, 0.063 W, 1%, 0603	MC0063W060311K	FEC 9330380
T1 to T9	Red test points	20-313137	FEC 873-1144
U1	High voltage, latch-up, proof dual SPDT switches	ADG5436FBRUZ	ADG5436FBRUZ
U2	5 V linear regulator, LDO	ADP7142AUJZ-5.0	ADP7142AUJZ-5.0-R7