Evaluating the **ADA4350**, a FET Input Analog Front End With ADC Driver
Offered in a 28-Lead 9.8 mm × 6.4 mm TSSOP

**FEATURES**
- Enables quick breadboarding/prototyping
- User defined circuit configuration
- Edge mounted SMA connector provisions
- Easy connection to test equipment and other circuits
- Guard ring to minimize leakage currents

**GENERAL DESCRIPTION**
The EVAL-ADA4350RUZ-P evaluation board is designed to help users evaluate the ADA4350 offered in a 28-lead, 9.8 mm × 6.4 mm thin shrink small outline package (TSSOP). The evaluation board is a populated board that enables users to quickly prototype the best configuration of the analog front end for their systems. Figure 1 shows the component side of the bare evaluation board, and Figure 2 shows the solder side of the bare evaluation board.

The evaluation board is a 6-layer printed circuit board (PCB) designed to minimize leakage currents with its guard ring features. It accepts SMA edge mounted connectors on the inputs and outputs for efficient connection to test equipment or other circuitry.

The evaluation board components are primarily SMT 0603 case size, with the exception of the electrolytic bypass capacitors (C9, C10, and C13), which are 1206 case size.

Figure 10 shows the ADA4350 configured as a transimpedance amplifier with multiple gains when a dual supply is used.

Figure 3 and Figure 4 show the signal gain/noise gain of the board when configured as Figure 10. Figure 7 to Figure 9 show the guard ring details. Figure 11 shows the assembly drawing and Figure 12 shows the 6-layer stackup along with the dimensions for each layer. The bill of materials is listed in Table 2.

**DIGITAL PICTURES OF THE EVALUATION BOARD**

![Figure 1. ADA4350 Evaluation Board Component Side](image1)

![Figure 2. ADA4350 Evaluation Board Solder Side](image2)
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REVISION HISTORY
5/15—Revision 0: Initial Version
EVALUATION BOARD HARDWARE

POWER SUPPLIES

The ADA4350 has two supplies. The analog supply is used to power up all the analog circuitries while the digital supply is used to power up all the digital controls. The two supplies have separate grounds inside the chip. Table 1 shows the supply range of the analog and digital supply, the voltages to be applied to the supply pins in different configurations, and their limitations.

GUARD RING FEATURES

The ADA4350 evaluation board employs a two layer electrostatic guarding to minimize leakage currents from entering the TIA node.

Five mil wide guard rings encircle the inverting and noninverting input components on the top copper layer (see Figure 7 and Figure 9). The guard rings connect to the internal GND copper layer with 5 mil dia vias. Each component pad that connects to the TIA inverting and noninverting inputs is connected to an internal copper trace with 5 mil dia vias (see Figure 8 and Figure 9).

This electrostatic guarding scheme provides isolation from leakage currents but adds a 35 pF parasitic capacitance to the TIA inverting node.

FREQUENCY RESPONSE

The ADA4350 evaluation board is configured for a simulated photodiode input. The photodiode capacitance is represented by C1, a 51 pF capacitor. The photodiode current is simulated by the input voltage Vin-N and R2, a 100 kΩ resistor. IPHOTODIODE = (Vin-N)/100 kΩ.

The total capacitance (91 pF) seen by the TIA is the sum of the ADA4350 input capacitances (2 pF + 3 pF), the photodiode capacitance (51 pF), and the parasitic capacitance of the electrostatic guarding (35 pF).

The five feedback resistor values are approximately ½ decade apart. The five compensation capacitors are selected for maximum bandwidth and maximum gain flatness.

The normalized transimpedance and noise gain are shown in Figure 3 and Figure 4 with compensation capacitors installed and not installed.

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Table 1. Powering Up the Analog and Digital Supplies

<table>
<thead>
<tr>
<th>Supply</th>
<th>Supply Range (V)</th>
<th>Dual Supplies (±V_S)</th>
<th>Single Supplies (+V_S)</th>
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<tr>
<td>Analog</td>
<td>3.3 to 12</td>
<td>VCC GND VEE</td>
<td>VCC GND VEE</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+V_S 0 −V_S</td>
<td>+V_S 0 0</td>
</tr>
<tr>
<td>Digital</td>
<td>3.3 to 5.5</td>
<td>VCC to DGND</td>
<td>VCC to DGND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≥3 V</td>
<td>≥3 V</td>
</tr>
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</table>
EVALUATION BOARD CONTROL

This user guide focuses on setting up the evaluation board. For logic tables of the different control modes and for an in depth analysis of the circuit, refer to the ADA4350 data sheet.

**Manual Mode**

The evaluation board is configured for manual gain selection using the DIP switches. The DIP switch on position represents Logic 0. To operate manually, set the enable switch to Logic 1 (off position), and set the MODE switch to Logic 1 (off position).

To select one gain, set all gain select switches, P0 to P4, to Logic 0 (on position) and select a gain by setting the corresponding gain select switch to Logic 1 (off position).

Note that only five feedback paths (FB0 to FB4) can be accessed in the manual mode and that selecting more than one gain connects all the selected feedback resistors in parallel.

**SPI Control (Parallel Mode)**

The parallel mode works very similar to the manual mode except that five digital control lines (P0 to P4) are used instead of the manual switches. Set the enable switch to Logic 1 (off position), and set the MODE switch to Logic 1 (off position). Set the DIP switches (P0 to P4) to Logic 1 (off position), and connect the logic output of an external microcontroller or FPGA to the plated holes next to the P0 to P4 switches. A Logic 1 on each digital line selects the corresponding gain. Applying a Logic 1 to more than one line at a time connects all the selected gains in parallel.

**SPI Control (Serial Mode)**

Set the MODE switch and LATCH switch to Logic 0 (on position), and the ENABLE switch to Logic 1 (off position). Set all other gain select switches (P1 to P4) to Logic 1 (off position), and perform the following steps:

1. Plug the Analog Devices, Inc., SDP-S controller board onto the 120-pin connector on the ADA4350 evaluation board. The SDP-S control board can be purchased from Analog Devices. The user can also use an individual SPI interface through the 5-pin SPI connector on the evaluation board.

2. Download the LabVIEW® control panel from [http://www.analog.com/ada4350-demoinstaller](http://www.analog.com/ada4350-demoinstaller). Unzip the file, click setup.exe, and follow the installation prompts. If the installation is successful, the ADA4350 Evaluation icon appears under Start > Programs > Analog Devices (see Figure 5).

**Switches**

The gain select switches (S0 to S5) have around 350 Ω series internal resistance that appears as a resistance in series with the TIA output, while S6 to S11 has around 150 Ω switch resistances.
EVALUATION BOARD ELECTROSTATIC GUARDING

The guard ring is represented by the red enclosed area around the inputs. The evaluation board uses the guard ring to minimize leakage currents entering the inputs causing offsets.

Note that the guard ring is employed all the way from the top copper layer through the inner layers and into the ground layer.
EVALUATION BOARD SCHEMATIC AND ARTWORK

Figure 10. Schematic
Figure 11. Component Side Assembly Drawing

Figure 12. Layer Stackup

6 LAYER STACKUP

NOMINAL FINISHED BOARD THICKNESS
0.063" +/- 0.007"

PRIMARY SILK SCREEN (.TSK)
PRIMARY SOLDER MASK (.TMK)
PRIMARY SOLDER (.TOP)
GROUND PLANE (.GND)
ADJUST AS NECESSARY
VCC PLANE (.VCC)
GND PLANE (.GND)
VACUUM PLANE (.VEE)
SECONDARY SIDE (.BOT)
SECONDARY SOLDER (.BMK)
SECONDARY SILK SCREEN (.BSK)

CHARACTERISTIC IMPEDANCE = 50 ohms
ARTWORK LINE WIDTH FOR IMPEDANCE CONTROLLED LINES = 15 mils
ADJUST IMPEDANCE CONTROLLED LINES DOWN FOR BEST RESULTS.
ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

<table>
<thead>
<tr>
<th>Qty</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Package</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>None</td>
<td>Analog supply connector</td>
<td>3-pin 100 mil header</td>
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<tr>
<td>1</td>
<td>None</td>
<td>Digital supply connector</td>
<td>2-pin 100 mil header</td>
</tr>
<tr>
<td>1</td>
<td>None</td>
<td>2-pin mode selector</td>
<td>2-pin dip switch</td>
</tr>
<tr>
<td>1</td>
<td>None</td>
<td>5-pin gain selector</td>
<td>5-pin dip switch</td>
</tr>
<tr>
<td>3</td>
<td>C9, C10, C13</td>
<td>10 µF capacitor</td>
<td>1206</td>
</tr>
<tr>
<td>6</td>
<td>C5 to C8, C11, C12</td>
<td>0.1 µF capacitor</td>
<td>0603</td>
</tr>
<tr>
<td>10</td>
<td>CF0 to CF5, C1 to C4</td>
<td>Capacitor, user defined</td>
<td>0603</td>
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<td>ADA4350</td>
<td>See the ADA4350 data sheet packaging information</td>
<td>28-lead TSSOP</td>
</tr>
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<td>1</td>
<td>Vin, _P, Vin, _N, VCM-IN, Vin1, Vout1, Vout2, TIA Out</td>
<td>SMA/SMT</td>
<td>SMA/SMT</td>
</tr>
<tr>
<td>29</td>
<td>R1 to R21, RF0 to RF5, RF, RG</td>
<td>Resistor, user defined</td>
<td>R0603</td>
</tr>
<tr>
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<td>SDP connector</td>
<td>Standard 120-pin SDP connector</td>
<td>MSOP</td>
</tr>
<tr>
<td>1</td>
<td>Small SDP connector</td>
<td>5-pin SPI header</td>
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<tr>
<td>1</td>
<td>24LC32AF</td>
<td>EEPROM</td>
<td></td>
</tr>
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</table>

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