Evaluation Board for the AD7768 24-Bit, 8-Channel, Simultaneous Sampling, 256 kSPS, Sigma-Delta ADC with Power Scaling

FEATURES
Full featured evaluation board for the AD7768
PC control in conjunction with the SDP-H1 System Demonstration Platform (EVAL-SDP-CH1Z)
PC software control and data analysis
Time and frequency domain
Standalone hardware capability

ONLINE RESOURCES
Evaluation Kit Contents
EVAL-AD7768FMCZ evaluation board
Evaluation software CD for the AD7768
Documents Needed
AD7768 data sheet
EVAL-AD7768FMCZ user guide
Required Software
AD7768 evaluation software

EQUIPMENT NEEDED
EVAL-AD7768FMCZ evaluation board
EVAL-SDP-CH1Z System Demonstration Platform
External 7 V to 9 V bench top power supply
DC/AC signal source (Audio Precision or similar high performance signal source)
USB cable
PC running Windows with USB 2.0 port

GENERAL DESCRIPTION
The EVAL-AD7768FMCZ evaluation kit features the AD7768 24-bit, 256 kSPS, analog-to-digital converter (ADC). A 7 V to 9 V external bench top supply is regulated to 5 V and 3.3 V to supply the AD7768 and support components. The EVAL-AD7768FMCZ board connects to the USB port of the PC via a connection to the EVAL-SDP-CH1Z motherboard.

The AD7768 evaluation software fully configures the AD7768 device register functionality and provides dc and ac time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

The EVAL-AD7768FMCZ is an evaluation board that allows the user to evaluate the features of the ADC. The user PC software executable controls the AD7768 over a USB cable through the EVAL-SDP-CH1Z System Demonstration Platform (SDP). The AD7768 evaluation software requires PC running Windows® 7 to Windows 10 with a USB 2.0 port.

Full specifications on the AD7768 are available in the product data sheet, which should be consulted in conjunction with this user guide when working with the evaluation board.
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REVISION HISTORY

10/2017—Rev. 0 to Rev. A
Change to General Description ...................................................... 1
Changes to Evaluation Board Software Section ......................... 10
Added Figure 3 and Figure 4; Renumbered Sequentially ..... 10
Changes to Figure 16...................................................................... 13
Changes to Figure 17 and Help Button Section, Added Sweep
Button Section................................................................................ 14
Changes to Waveform Tab Section and Figure 20 ............... 15
Changes to FFT Tab Section, Histogram Tab Section, Figure 21
through Figure 24.......................................................................... 16
Change to Example Section............................................................ 17

1/2016—Revision 0: Initial Version
To begin using the evaluation board, do the following:

1. Ensure that the EVAL-SDP-CH1Z board is disconnected from the USB port of the PC. Install the evaluation board software from the CD included in the evaluation board kit. Restart the PC after the software installation is complete. (For complete software installation instructions, see the Software Installation Procedures section.)

2. Connect the EVAL-SDP-CH1Z board to the EVAL-AD7768FMCZ board (unpowered). Figure 1 illustrates the connection: J4 of the EVAL-SDP-CH1Z board adapts to the receiving socket on the EVAL-AD7768FMCZ printed circuit board (PCB).

3. Ensure that the boards are connected firmly together.

4. Apply power to the EVAL-AD7768FMCZ board via the supplied 9 V dc adapter at J1 (LK1 in Position B). Alternatively, supply an external voltage in the range of 7 V to 9 V from a bench top power supply using the J3 connector (LK1 in Position A).

5. Connect the 12 V dc supply to the EVAL-SDP-CH1Z board, and then connect to the PC using the supplied USB cable. For Windows XP, the PC may need to search for the EVAL-SDP-CH1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CH1Z board if prompted by the operating system.

6. Launch the AD7768 evaluation software from the Analog Devices subfolder in the Programs menu.
ANALOG INPUTS AND FRONT-END CIRCUIT

As shown in Figure 1, the AIN0± to AIN7± analog inputs are accessible through either the SMBs or the terminal blocks.

Figure 2 shows these connectors and details the 16 main solder links that route the inputs from either the terminal blocks or the SMBs for each of the signals.

In the default board configuration, the input terminals are connected through to the ADA4896-2 on each of the ADC channels.

The ADR444 4.096 V low noise reference is used by default, allowing an absolute input range of 0±4.096 V on each input.

The ADA4896-2 amplifiers are not terminated at the inputs for any particular source impedances.

The on-board, common-mode voltage source on the AD7768 is used to bias the input signal. The default condition is \( V_{CM} = (AVDD1 - AVSS)/2 \).

Figure 2. Analog Inputs: Input Connectors, Solder Links, and Amplifiers
EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7768 is an 8-channel, simultaneously sampling, Σ-Δ ADC. The AD7768 offers an ADC per channel and synchronized sampling. The ADC power scaling is as required for the application, catered for by selecting one of the following modes of operation:

- **Fast**: 256 kSPS maximum, 110.8 kHz input bandwidth, 52 mW per channel
- **Median**: 128 kSPS maximum, 55.4 kHz input bandwidth, 28 mW per channel
- **Economy**: 32 kSPS maximum, 13.8 kHz input bandwidth, 9.5 mW per channel

The AD7768 offers extensive digital filtering:

- **Wideband**: low ripple, non-aliasing, low pass filter with sharp roll off, and full attenuation at Nyquist frequency.
- **Sinc response**: sinc5 filter, low latency path for dc measurements or control loops.

Within these filter options, the user can select a decimation rate of 32, 64, 128, 256, 512, or 1024.

Embedded analog functionality on each ADC channel simplifies system design. A precharge buffer on each analog input reduces analog input current.

Complete specifications for the AD7768 are provided in the product data sheet and should be consulted in conjunction with this user guide when using the evaluation board. Full details about the EVAL-SDP-CH1Z are available on the Analog Devices, Inc., website.

HARDWARE LINK OPTIONS

The default link options are listed in Table 1. The board can be configured to operate from a bench top power supply via Connector J3, or from a 9 V dc adapter via Connector J1. The supply required for the AD7768 comes from the on-board low-dropout regulators (LDOs), which generate their input voltage from J1 or J3 depending on the setting of LK1. Alternatively, the board can be powered by setting LK2 to Position A when used in conjunction with the EVAL-SDP-CH1Z (see Table 3 for details).

### Table 1. Default Link and Solder Link Options

<table>
<thead>
<tr>
<th>Link No.</th>
<th>Default Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>A</td>
<td>LK1 selects the input voltage source. Position A: J3 is selected Position B: J1 is selected</td>
</tr>
<tr>
<td>LK2</td>
<td>B</td>
<td>LK2 selects the input from EVAL-SDP-CH1Z board. Position A: 12 V input from EVAL-SDP-CH1Z Position B: external power supply from either J1 or J3</td>
</tr>
<tr>
<td>SL1</td>
<td>A</td>
<td>SL1 selects between pin or SPI mode operation of the AD7768. Position A: SPI mode Position B: pin mode (pin mode is not compatible with the evaluation software and currently untested on evaluation board)</td>
</tr>
<tr>
<td>SL2</td>
<td>B</td>
<td>Format 0 pin. Position A: IOVDD Position B: DGND</td>
</tr>
<tr>
<td>SL3</td>
<td>A</td>
<td>Format 1 pin. Position A: DGND Position B: IOVDD</td>
</tr>
<tr>
<td>SL4</td>
<td>A</td>
<td>Clock terminal source selection. To choose the Y1 crystal oscillator, do not populate SL4. R253, R254, C46, and C45 must be populated. SL4A must be configured to the crystal oscillator. Position A: selects CMOS Oscillator Y2 Position B: unpopulated terminals J6 and J7 Position C: SDP MCLK</td>
</tr>
<tr>
<td>SL4A</td>
<td>A</td>
<td>Clock select pin CMOS clock option on Pin 32 Crystal oscillator or LVDS option</td>
</tr>
<tr>
<td>SL5</td>
<td>Soldered 0 Ω Resistor</td>
<td>Shorts SYNC_OUT to SYNCIN to allow sync pulses on START to be synchronously applied to SYNCIN.</td>
</tr>
<tr>
<td>SL6</td>
<td>A</td>
<td>Pin 16: PD0/CS Position A: CS chip select pin in SPI mode Position B: Channel 0 to Channel 3 power down (pin mode) Position C: Channel 0 to Channel 3 enabled (pin mode)</td>
</tr>
<tr>
<td>Link No.</td>
<td>Default Option</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>----------------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| SL7     | A              | Pin 17: PD1/SCLK.  
Position A: SCLK in SPI mode  
Position B: Channel 4 to Channel 7 power down (pin mode)  
Position C: Channel 4 to Channel 7 enabled (pin mode) |
| SL8     | A              | Pin 18: DEC1/SDI.  
Position A: SDI in SPI mode  
Position B: IOVDD  
Position C: GND |
| SL9     | A              | Pin 18: DECO/SDO.  
Position A: SDO in SPI mode  
Position B: IOVDD  
Position C: GND |
| SL10    | A              | Pin 12: MODE0/GPIO0.  
Position A: GPIO to SDP  
Position B: GND  
Position C: IOVDD |
Position A: GPIO to SDP  
Position B: GND  
Position C: IOVDD |
Position A: GPIO to SDP  
Position B: GND  
Position C: IOVDD |
Position A: GPIO to SDP  
Position B: GND  
Position C: IOVDD |
| SL14    | A              | Pin configuration mode.  
AD7768 evaluation kit software runs from SPI mode; select the filter via  
the register map. This link selects the filter mode (only available in pin mode).  
Position A: GPIO4  
Position B: sinc5 fast settling filter  
Position C: wideband low-ripple filter |
| SL15    | A              | Select common-mode voltage to bias input signals to one of the following.  
Position A: OP2177 buffered VCM output  
Position B: VCM output from AD7768 |
| SL16    | B              | Select reference path from ADR444 to REFX+.  
Position A: bypass external reference buffer  
Position B: ADR444 input into ADA4841-1 reference buffer |
| SL17    | B              | Select reference path from ADR444 to REFX+.  
Position A: bypass external reference buffer  
Position B: select output from ADA4841-1 reference buffer |
| SL18    |                | Unsoldered  
Shorts IOVDD to DREGCAP, only for IOVDD = 1.8 V operation; see the AD7768 data sheet. |
| SL19    | A              | External common mode buffer input selection.  
Position A: AD7768 VCM pin  
Position B: AVDD1 used for common-mode selection, R166 (0 Ω) and R167 (not inserted) can be  
used as voltage dividers |
| SL22, SL23 |            | Selects the output from Channel 5 surf board option.  
Position A: ADA4896-2  
Position B: bypass driver  
Position C: amplifier surf board header via the J11 and J12 connectors |
<table>
<thead>
<tr>
<th>Link No.</th>
<th>Default Option</th>
<th>Description</th>
</tr>
</thead>
</table>
| SLP1    | A              | AVDD1 input selector.  
Position A: ADP7118ARDZ-5.0 5 V LDO  
Position B: external AVDD1 input, J2-3 |
| SLP2    | A              | AVDD2 LDO selector.  
Position A: ADP7118ARDZ-5.0 5 V LDO  
Position B: external AVDD2 input, J2-4 |
| SLP4    | A              | IOVDD input selector.  
Position A: ADP7118ARDZ-3.3 3.3 V LDO  
Position B: external AVDD2 input, J2-5, 2.25 V to 3.6 V, 1.8 V |
| SL_AMP+ | A              | ADA4896-2 positive supply voltage.  
Position A: AVDD1 ADP7118ARDZ-5.0 5 V supply  
Position B: external supply to board, J1 or J3 input depending on LK1 position |
| SL_AMP- | A              | ADA4896-2 negative supply voltage.  
Position A: evaluation board ground plane  
Position B: external supply to board, J1 or J3 input depending on LK1 position, on-board ADA4896-2 are shorted to ground and VSS pins, replace with capacitors for bipolar amplifier supplies |
| SL7+ to SL0+,  
SL7− to SL0− | A | Selects the input driver for Channel 7, Channel 6, Channel 4, Channel 3, Channel 2, Channel 1, and Channel 0.  
Position A: ADA4896-2  
Position B: bypass driver |
| SL5+, SL5− | A | Selects the input driver for Channel 5.  
Position A: ADA4896-2  
Position B: bypass driver  
Position C: amplifier surf board header via the J11 and J12 connectors |

**On-Board Connectors**

Table 2 provides information about the external connectors on the EVAL-AD7768FMCZ.

**Table 2. On-Board Connectors**

<table>
<thead>
<tr>
<th>Connector</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Wall wart (dc plug) power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board.</td>
</tr>
<tr>
<td>J2</td>
<td>Connector for supplying AVDD1, AVDD2, IOVDD, AVSS, and AGND externally.</td>
</tr>
<tr>
<td>J3</td>
<td>Bench top power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board.</td>
</tr>
<tr>
<td>J6</td>
<td>SMA/SMB connector for XTAL2 (CLKIN/LVDS).</td>
</tr>
<tr>
<td>J7</td>
<td>SMA/SMB connector for XTAL1 (LVDS).</td>
</tr>
<tr>
<td>J8, J9</td>
<td>8-pin connector for input to Channel 4 to Channel 7.</td>
</tr>
<tr>
<td>J11</td>
<td>Optional external connector for driver daughter board. Channel 5.</td>
</tr>
<tr>
<td>J12</td>
<td>Optional external connector for driver daughter board. Channel 5.</td>
</tr>
<tr>
<td>J13, J14</td>
<td>8-pin connector for input to Channel 0 to Channel 3.</td>
</tr>
<tr>
<td>J15</td>
<td>Unpopulated VCM SMA connector.</td>
</tr>
<tr>
<td>A0+ to A7+</td>
<td>Analog input SMA positive terminal for Channel 0 to Channel 7.</td>
</tr>
<tr>
<td>A0− to A7−</td>
<td>Analog input SMA negative terminal for Channel 0 to Channel 7.</td>
</tr>
<tr>
<td>P1</td>
<td>Connector on the underside of the EVAL-AD7768FMCZ board that mates with the EVAL-SDP-CH1Z controller board.</td>
</tr>
</tbody>
</table>
POWER SUPPLIES
The evaluation board requires that an external power supply, either a bench top supply or a wall wart (dc plug) supply, be applied to J1 or J3 (see Table 3 for more information). Linear regulators generate the required power supply levels from the applied $V_{IN}$ rail. The regulators used are the 5 V ADP7118 (U1 and U7), which supply AVDD1, the on-board amplifiers and reference, and the 3.3 V ADP7118 (U16), which delivers 3.3 V to the IOVDD pin of the AD7768.

SERIAL DATA INTERFACE
The AD7768 evaluation board outputs conversion results to the EVAL-SDP-CH1Z via the eight data output pins, DOUT0 to DOUT7. The serial data interface also includes signals such as SCLK, DCLK, and RDY (all are outputs).

SERIAL CONFIGURATION INTERFACE
The AD7768 is configured by the EVAL-SDP-CH1Z via a 4-wire SPI interface. SL1 must be shorted to Position A for this mode to be active.

POWERING DOWN THE SYSTEM DEMONSTRATION PLATFORM
When disconnecting the SDP-H1 evaluation platform and powering down the system, make sure to first exit the evaluation software. Then, press the reset button on the EVAL-SDP-CH1Z board before disconnecting the 12 V supply and then the USB. Failure to follow this procedure can cause damage to the EVAL-SDP-CH1Z board.

<table>
<thead>
<tr>
<th>Power Supply (V_m) From</th>
<th>Voltage Range</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>7 V to 9 V</td>
<td>Wall wart (dc plug) supply to the evaluation board. Supplies LDOs that create 5 V and 3.3 V rails. It also supplies the ADR444 external reference. Ensure that both LK1 and LK2 are set to Position B when the external power supply is applied to this connector.</td>
</tr>
<tr>
<td>J3</td>
<td>7 V to 9 V</td>
<td>Bench top supply to the evaluation board. Supplies LDOs that create 5 V and 3.3 V rails. It also supplies the ADR444 external reference and on-board amplifiers. Ensure that LK1 is set to Position A when the external power supply is applied to this connector and LK2 is set to Position B.</td>
</tr>
<tr>
<td>EVAL-SDP-CH1Z</td>
<td>12 V</td>
<td>If using the EVAL-SDP-CH1Z, power can be taken from this board and supplied to the LDOs. Set LK2 to Position A.</td>
</tr>
</tbody>
</table>

1 Only a single supply is required.
SOCKETS/CONNECTORS

Table 4. Connector Details

<table>
<thead>
<tr>
<th>Connector</th>
<th>Function</th>
<th>Connector Type</th>
<th>Manufacturer/Part No.</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Wall wart (dc plug) power supply voltage input. Apply 7 V.</td>
<td>2 mm dc power connector</td>
<td>Kycon KLDX-SMT2-0202-A</td>
<td>Mouser 806-KLDX-SMT20202A</td>
</tr>
<tr>
<td>J2</td>
<td>Apply voltage within data sheet specified ranges and GND (0 V) to this connector to power the evaluation board. J2 is the connector for supplying AVDD1, AVDD2, IOVDD, AVSS, and AGND externally.</td>
<td>5-pin socket terminal block</td>
<td>Lumberg FRE 05</td>
<td>Farnell 1217310</td>
</tr>
<tr>
<td>J3</td>
<td>Bench top power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board.</td>
<td>3-pin socket terminal block, 3.81 mm pitch</td>
<td>Phoenix Contact MC 1,5/3-G-3,81</td>
<td>Farnell 3704737</td>
</tr>
<tr>
<td>J6</td>
<td>SMA/SMB connector for XTAL2 (CLKIN/LVDS).</td>
<td>Straight PCB mount SMB/SMA jack</td>
<td>Tyco 1-1337482-0</td>
<td>Not inserted</td>
</tr>
<tr>
<td>J7</td>
<td>SMA/SMB connector for XTAL1 (LVDS).</td>
<td>Straight PCB mount SMB/SMA jack</td>
<td>Tyco 1-1337482-0</td>
<td>Not inserted</td>
</tr>
<tr>
<td>J8, J9</td>
<td>8-pin connector for input to Channel 4 to Channel 7.</td>
<td>8-pin socket terminal block, 3.81 mm pitch</td>
<td>Phoenix Contact MC 1,5/8-G-3,81</td>
<td>Farnell 3704774</td>
</tr>
<tr>
<td>J11</td>
<td>Optional external connector for driver daughter board. Channel 5.</td>
<td>7-way, 2.54 mm TH header</td>
<td>Samtec SSW-107-01-T-S</td>
<td>Farnell 1803478</td>
</tr>
<tr>
<td>J12</td>
<td>Optional external connector for driver daughter board. Channel 5.</td>
<td>7-way, 2.54 mm vertical socket</td>
<td>Samtec TLW-107-05-G-S</td>
<td>Farnell 1668499</td>
</tr>
<tr>
<td>J13, J14</td>
<td>8-pin connector for input to Channel 0 to Channel 3.</td>
<td>8-pin socket terminal block, 3.81 mm pitch</td>
<td>Phoenix Contact MC 1,5/8-G-3,81</td>
<td>Farnell 3704774</td>
</tr>
<tr>
<td>J15</td>
<td>Unpopulated VCM SMA connector.</td>
<td>Straight PCB mount SMB/SMA jack</td>
<td>Tyco 1-1337482-0</td>
<td>Farnell 3704737</td>
</tr>
<tr>
<td>A10+ to A17+</td>
<td>Analog input SMA positive terminal for Channel 0 to Channel 7.</td>
<td>Straight PCB mount SMB/SMA jack</td>
<td>Tyco 1-1337482-0</td>
<td>Farnell 1206013</td>
</tr>
<tr>
<td>A10− to A17−</td>
<td>Analog input SMA negative terminal for Channel 0 to Channel 7.</td>
<td>Straight PCB mount SMB/SMA jack</td>
<td>Tyco 1-1337482-0</td>
<td>Farnell 1206013</td>
</tr>
<tr>
<td>P1</td>
<td>Connection to EVAL-SDP-CH1Z controller board.</td>
<td>160-pin, 10 mm male VITA 57 connector</td>
<td>Samtec ASP-134604-01</td>
<td>Farnell 2433507</td>
</tr>
</tbody>
</table>

EVALUATION BOARD SETUP PROCEDURES

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP boards as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CH1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Configuring the Evaluation and SDP Boards

Connect the EVAL-SDP-CH1Z board to P1 (bottom) on the EVAL-AD7768FMCZ board.
EVALUATION BOARD SOFTWARE
SOFTWARE INSTALLATION PROCEDURES

The EVAL-AD7768FMCZ evaluation kit includes a CD containing software to be installed on the PC before using the evaluation board.

There are two parts to the installation:

- AD7768 evaluation board software installation
- EVAL-SDP-CH1Z system demonstration platform board drivers installation

**Warning**

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CH1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC. When disconnecting the board, it is important to follow the power down sequence outlined in the Powering Down the System Demonstration Platform section.

**Installing the Evaluation Board Software**

To install the evaluation board software,

1. The EVAL-AD7768FMCZ evaluation software requires the .NET 3.5 framework in order to operate correctly. Ensure that the correct .NET framework is installed before continuing with the installation. This can be checked by doing the following:
   a) In the Windows Control Panel select Programs and then Programs and Features.
   b) Select the Turn Windows Features on or off section. This will list the features currently installed. In this list change that the .NET framework 3.5 (includes .NET 2.0 and 3.0) has been selected. Figure 3 below shows the dialog box as it appears in Windows 10.

2. With the EVAL-SDP-CH1Z board disconnected from the USB port of the PC, insert the installation CD into the CD-ROM drive.

3. Double-click the setup.exe file to begin the evaluation board software installation. The software is installed to the following default location: C:\Program Files\Analog Devices\AD7768.

4. A dialog box appears requesting permission to allow the program to make changes to the PC. Click Yes.

   a) After selecting the checkbox and clicking OK the dialog box in Figure 4 appears. Please note a valid internet connection is needed for this step. Select the Download files from Windows Update option and after installation the EVAL-AD7768FMCZ will operate as expected.

   ![Figure 4. Prompt to Download Windows Update](image)

   b) Figure 5 shows the dialog box as it appears in Windows 10.

   ![Figure 5. Evaluation Board Software Installation: Granting Permission for Program to Make Changes](image)
5. Select the location to install the software, and then click Next. Figure 6 shows the default installation locations, which are displayed when the window opens. To select a different installation location, click Browse.

![Figure 6. Evaluation Board Software Installation: Selecting the Location for Software Installation](image)

6. A license agreement appears. Read the agreement, select I accept the License Agreement, and then click Next.

![Figure 7. Evaluation Board Software Installation: Accepting the License Agreement](image)

7. A summary of the installation is displayed. Click Next to continue.

![Figure 8. Evaluation Board Software Installation: Reviewing a Summary of the Installation](image)

8. A dialog box informs you when the installation is complete. Click Next.

![Figure 9. Evaluation Board Software Installation: Indicating When the Installation is Complete](image)
Installing the System Demonstration Platform Board Drivers

After the installation of the evaluation software is complete, a welcome window displays for the installation of the SDP drivers.

1. With the EVAL-SDP-CH1Z board still disconnected from the USB port of the PC, make sure that all other applications are closed, and then click Next.

2. Select the location to install the drivers, and then click Next.

3. Click Install to confirm that you want to install the drivers.

4. To complete the drivers installation, click Finish, which closes the installation wizard.

5. Before using the evaluation board, you must restart your computer.
SETTING UP THE SYSTEM FOR DATA CAPTURE

After completing the steps in the Software Installation Procedures and Evaluation Board Hardware sections, set up the system for data capture as follows:

1. Allow the **Found New Hardware Wizard** to run after the **EVAL-SDP-CH1Z** board is plugged into the PC. (If using Windows XP, the PC may need to search for the SDP drivers. Choose to automatically search for the drivers for the SDP board if prompted by the operating system.)

2. Check that the board is connecting to the PC correctly using the **Device Manager** of the PC.
   a. Access the **Device Manager** as follows:
      i. Right-click **My Computer** and then click **Manage**.
      ii. A dialog box appears asking for permission to allow the program to make changes to the computer. Click **Yes**.
      iii. The **Computer Management** box appears. Click **Device Manager** from the list of **System Tools** (see Figure 15).
   b. The **EVAL-SDP-CH1Z** board appears under **ADI Development Tools**, which indicates that the driver software is installed and that the board is connected to the PC correctly.

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**Launching the Software**

After completing the steps in the Setting Up the System for Data Capture section, launch the **AD7768** software as follows:

1. From the Start menu, click **Programs > Analog Devices > AD7768 Evaluation Software**. The main window of the software then displays.

2. If the **AD7768** evaluation system is not connected to the USB port via the **EVAL-SDP-CH1Z** when the software is launched, a connectivity error displays prompting the user to choose an evaluation board (see Figure 16). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and then follow the on-screen instructions.

When the software starts running, it searches for hardware connected to the PC. A dialog box indicates when the SDP board connected to the PC is detected, and then the main window appears (see Figure 17).
SOFTWARE OPERATION

Figure 17. Evaluation Software Main Window

Overview of the Main Window
The main window contains the significant control buttons and analysis indicators of the evaluation software.

Configuration Tab and AD7768 Block Diagram
The Configuration tab is the tab displayed by default when the software first opens. An overview of the AD7768 block diagram is shown, along with buttons that open pop-up menus for quick configuration of the device.

The Waveform tab displays captured waveform data. It also contains options to save the resulting data and shows the outputted header data from the conversion results.

The FFT and Histogram tabs show a more in depth analysis of the outputted data. This data can be saved to a file.

Use the Registers tab to change the configuration of the AD7768.

Sample Button (1)
Click Sample to start ADC sampling; results are reported in the Waveform, FFT, and Histogram tabs. The mode of operation can be set using the Sampling Mode button; the mode can be continuous sampling or a single run.

Sweep Button (2)
Click the Sweep button to open the dialog box to choose where to save the sweep data. Once the file name is written, the software will start sampling at a different decimation rate on each filter type for channel mode A. The results are reported in the Waveform, FFT, and Histogram tabs. The data gathered from the sweep operation is saved and can be viewed from the .csv file.

Number of Samples (3)
The number of samples per channel is variable and can be changed using the Samples control.

MCLK (4)
The MCLK (Hz) control in the Configuration tab must match the frequency of the ADC clock source.

VREF (5)
The Ext. REF (V) in the Configuration tab control must match the reference voltage of the ADC.

ADC Reset (6)
Clicking ADC Reset in the Configuration tab sends a reset command to the ADC via the SPI, and resets the device to its default configuration.

Help Button (7)
The help button is located in the top right corner of the Configuration tab (see Figure 17). Click the help button to show information about the AD7768 software.
**Header Data**

The **Header Data** area shows the header data output in the first eight bits of a conversion. It conveys status information and the channel number. Header data for each channel can be selected by changing the **Analysis Ch** option.

- **CRC Error** indicates that an error has occurred, and a reset is required.
- **Filter not settled** indicates that the filter had not settled before data was sampled.
- **Filter Type** indicates the type of filter that has been selected.
- **Filter saturated** indicates that filter saturation has occurred.

Note that the evaluation software has not been configured to output the CRC check code.

![Header Data](image)

**Figure 18. Example Header Data**

**Channel Enable/Disable Check Box**

The channel enable and disable check boxes, as shown in Figure 19, individually enable channels for display and analysis.

![Channel Enable/Disable Check Boxes](image)

**Figure 19. Channel Enable/Disable Check Boxes**

**Status Indicator and Busy light**

The status bar at the bottom of the screen indicates the current state of the AD7768 software. The **Busy** LED illuminates when the software is busy performing an action. Refrain from carrying out any more actions when this light is lit.

**Waveform Tab**

The **Waveform** tab displays a time-domain graph of the sampled data. Controls beneath the graph allow zooming and panning. Amplitude information is given beneath the graph for the analysis channel selected. The data displayed in the graph is in a direct binary format converted from a two’s complement ADC output.

![Waveform Tab](image)

**Figure 20. Waveform Tab**

**Display Units (8)**

The **Display Units** dropdown menu selects the unit of the code displayed on the y-axis of the waveform graph; either decimal, hexadecimal, or the voltage equivalent of the code.

**Captured Data Button (9)**

Click the **Captured Data** button to open the dialog box to choose where to save the latest captured data. The **Captured Data** button saves only the latest codes after the **Sample** button is clicked.
**FFT Tab**

The FFT tab shows a frequency-domain graph of the sampled data. Controls beneath the graph allow zooming and panning, and control over amplitude and frequency scaling. Frequency and amplitude information is given beneath the graph for the selected analysis channel.

![Figure 21. FFT Tab](image)

**Save Data Button (10 and 11)**

Click the **Save Data** button to open a dialog box to save the histogram and FFT analysis data for the current sample. The data can also be saved by **right clicking** on the graph and choosing **Export** from the dropdown menu.

**Histogram Tab**

The Histogram tab shows a histogram of the sampled data. Controls beneath the graph allow zooming and panning, and control over amplitude scaling. Amplitude information is given beneath the graph for the selected analysis channel.

![Figure 22. Histogram Tab](image)

**Registers Tab**

The Registers tab allows precise control of the AD7768 registers, allowing them to be read back and written to. The registers are grouped together and can be altered in a number of ways, as shown in Figure 23. The register to be written to can be selected from the register map, located on the left hand side of the Registers tab. Individual register bits can be changed from the register section, or the entire register can also be written to by writing the required hexadecimal value. Drop-down options can be selected from the Bitfields section, or the entire bitfield can be written to with a hexadecimal value.

A particular register configuration can be saved to be loaded again at a later time.

![Figure 23. Registers Tab](image)

**Precharge Buffers: Register Operation**

The precharge buffers operate differently to the other registers. To change these registers, it is recommended to navigate to the Registers tab, select **Precharge Buffer 1** or **Precharge Buffer 2** from the register map, and change the value of these registers using the hexadecimal value located on the right hand side of the Register section (see Figure 24). The software reads back the status of the registers correctly; however, to change a bit to 0, for example, a 1 must be written to the given bit in the register. See the AD7768 data sheet for more details.

![Figure 24. Enabling/Disabling the Precharge Buffers](image)

**Exiting the Software**

To exit the software, click the red X at the top right hand corner of the main window. Be sure to press the reset button before the EVAL-SDP-CH1Z is powered off.
Example

In this example, a sample is taken and analyzed with the help of the AD7768 software. The desired data is expected on Channel 2 of the ADC.

1. Start the AD7768 software. Wait for the Busy indicator to turn off.
2. Ensure that MCLK (Hz) and Ext. REF (V) are set to match the clock frequency and reference voltage supplied to the chip (by default, 32 MHz and 4.096 V).
3. Set the number of samples per channel to 32,768 (default).
4. Configure the registers as required using the pop-up menus under the Configuration tab.
5. Click Sample to take a reading. Wait for the Busy indicator to turn off.
6. The sampled data is now present in the data capture tabs (Waveform, FFT, and Histogram tabs). Change between each of these to view the results. In this case, be sure to select Channel 2 on the channel enable and disable check boxes to view the desired data.
7. Change various settings and observe the output. For example, set the number of samples per channel to 16,384.
8. Click Sample to take a reading. Wait for the Busy indicator to turn off.
9. The sampled data is now present in the Waveform, FFT, and Histogram tabs.
NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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