Evaluating the AD7760 and AD7762 Using the EVAL-CED1Z

FEATURES
Full featured evaluation board for the AD7760/AD7762
EVAL-CED1Z-compatible
On-board 4.096 V reference
Crystal clock oscillator MCLK source
Evaluation software for control and data analysis
(download from product page)
Filter programmability—load custom filter to ADC

EVALUATION KIT CONTENTS
EVAL-AD7760EDZ or EVAL-AD7762EDZ evaluation board
EVAL-AD7760EDZ/EVAL-AD7762EDZ software CD
(also available for download from product page)

ADDITIONAL EQUIPMENT NEEDED
EVAL-CED1Z (must order separately), includes a USB cable
Bench top power supply to Connector J2

GENERAL DESCRIPTION
This user guide describes the evaluation boards for the AD7760/
AD7762 Σ-Δ analog-to-digital converters (ADCs). The AD7760,
a 24-bit ADC, combines wide input bandwidth and high speed
with the benefits of Σ-Δ conversion with a performance of 100 dB
SNR at 2.5 MSPS, making it ideal for high speed data acquisition.
The AD7762 derivative is a parallel version with a maximum
output data rate of 625 kSPS.

Complete specifications for the AD7760/AD7762 are available
in the AD7760 and AD7762 data sheets available from Analog
Devices, Inc.; the data sheets should be consulted in conjunction
with this user guide when using the evaluation board.
The evaluation software is available to download from the
AD7760 and AD7762 product pages.
The AD7760 interfacing signals are created by the EVAL-CED1Z
board, which is used in conjunction with the evaluation board
to enable data acquisition via the provided software and USB
link. The kit requires the controller evaluation and development
(CED1) board, the EVAL-CED1Z, which must be purchased
separately. The evaluation board includes all routing required
for evaluating the ADC.
The combination of the evaluation board and the EVAL-CED1Z
board allied with the EVAL-AD7760EDZ/EVAL-AD7762EDZ
software allows the user to upload samples taken by the AD7760/
AD7762 onto a PC showing the waveform being sampled, as well
as allowing the data to be shown in histogram or FFT format.
The AD7760/AD7762 can also be used on a standalone basis
(without the EVAL-CED1Z); however, in this case, the user
must provide the interface and acquisition requirements.

TYPICAL SETUP

Figure 1. Typical Setup (EVAL-AD7760EDZ/EVAL-AD7762EDZ on Left and EVAL-CED1Z on Right)
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REVISION HISTORY

9/15—Revision 0: Initial Version
GETTING STARTED
The EVAL-AD7760EDZ/EVAL-AD7762EDZ controls and evaluates the performance of the AD7760/AD7762 when operated with the EVAL-CED1Z board. The software is compatible with Windows® 2000 and Windows XP. If the setup file does not run automatically, run setup.exe from the CD provided.

INSTALLING THE SOFTWARE
When the CD is inserted into the PC, an installation program automatically begins. This program installs the evaluation software. The user interface on the PC is a dedicated program written especially for the AD7760/AD7762 when operated with the EVAL-CED1Z board.

Warning
The software must be installed before the USB cable is connected between the EVAL-CED1Z and the PC, to ensure that the appropriate USB driver files have been properly installed before the EVAL-CED1Z is connected to the PC.

STARTING THE SOFTWARE
When the software is run for the first time with the EVAL-CED1Z board connected to the PC, the PC automatically finds and identifies the new device. Follow the instructions that appear on screen to install the drivers for the CED1 on the PC.

If an error appears when the software is first started, the PC is not recognizing the USB device. To correct this error,
1. Access the device manager by selecting Device Manager from the Hardware tab of the System Properties window.
2. Examine the devices listed under the Universal Serial Bus Controller heading.
3. If an unknown device is listed, right-click the unknown device and click Update Driver.
4. After the New Hardware Wizard runs twice, note that, under the ADI Development Tools, the following is listed: ADI Converter Evaluation and Development Board (WF).
5. Restart the PC.

SETTING UP THE SYSTEM
Follow the steps in this section to set up the evaluation board, the EVAL-CED1Z, and the software to begin using the complete system.

1. Insert the CD into the appropriate computer drive. Initial software installation information as shown in Figure 2 appears.

2. Choose the destination directory. Note that the default directory is shown. If a different location is preferred, click Browse and select the desired location. Then, click Next.

   ![Figure 2. Initial Software Install](image)

   ![Figure 3. Choose the Destination for the Software](image)
3. Accept the license agreement and click **Next** as shown in Figure 4.

![Figure 4. Accept License Agreement](image)

4. To start the installation, click **Next** as shown in Figure 5. This window shows the installation actions being taken.

![Figure 5. Install Steps](image)

5. Follow the path chosen during installation to locate the software. If the default location was chosen, the location of the software (for the AD7760) is **Start > All Programs > Analog Devices > AD7760_2 > AD7760_2**.

![Figure 6. Default Location of AD7760/AD7762 Software](image)

6. When the installation completes, the window as shown in Figure 7 displays. Restart the PC for the software to take full effect.

![Figure 7. Install Completed](image)
ABOUT THE EVALUATION HARDWARE

POWER SUPPLIES

The EVAL-AD7760EDZ/EVAL-AD7762EDZ must be powered using an external power supply that applies 7.5 V between the V+ and GND terminals of Connector J2.

This 7.5 V supply is then regulated on board using ADP3334 devices (U9 and U6) to provide the 2.5 V and 5 V signals required by the AD7760/AD7762. The AVDD2, AVDD3, and AVDD4 supplies are the 5 V supplies to the AD7760/AD7762. A voltage of 2.5 V supplies the AVDD1, VDRIVE, and DVDD pins of the AD7760/AD7762.

A separately regulated 2.5 V supply powers all the digital functionality on the evaluation board excluding the AD7760/AD7762. An individually regulated 5 V supply also supplies the crystal oscillator and clock buffer devices on the EVAL-AD7760EDZ/EVAL-AD7762EDZ. Setting LK1 to A means that the MCLK buffer is powered by 5 V, enabling the ADC to be operated using an MCLK signal with an amplitude of 5 V.

DIFFERENTIAL INPUT

The differential input to the AD7760/AD7762 is applied through Connector J1, which is an XLR audio standard connector. The differential inputs are routed through the AD7760/AD7762 onboard differential amplifiers using the external circuit components as detailed in the AD7760 and AD7762 data sheets.

STANDALONE OPERATION

The evaluation board can be used in a standalone manner (that is, without using the EVAL-CED1Z). In this case, however, the user must provide all required interface communications and a means to acquire the output data from the board.

DECOUPLING AND LAYOUT RECOMMENDATIONS

The AD7760 and AD7762 data sheets contain specific information about the decoupling and layout recommendations required to achieve optimum specifications.

The EVAL-AD7760EDZ/EVAL-AD7762EDZ adhere to these recommendations completely and are designed as the blueprint for users of the AD7760 and AD7762. The Gerber files for the evaluation board are available for download from the AD7760 and AD7762 product pages.

The EVAL-AD7760EDZ/EVAL-AD7762EDZ are 4-layer boards. One layer is a dedicated ground plane. All supplies to the devices on the EVAL-AD7760EDZ/EVAL-AD7762EDZ are decoupled to this ground plane. In addition to the printed circuit board (PCB) top and bottom layers, there is also a layer for routing power signals. All layers of the boards are detailed in the Evaluation Board Schematics and Artwork section.

In addition, the exposed paddle of an AD7760 or AD7762 is connected by multiple vias to this ground plane. The exposed paddle is not connected to any of the ground pins on the device.

LINK OPTIONS

The link options on the evaluation board are factory set for the required operating setup. The functions of these links are described in Table 1.

<table>
<thead>
<tr>
<th>Link No.</th>
<th>Function</th>
<th>Position Descriptions</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>Link option for power mode of the crystal oscillator</td>
<td>Removing this link places the crystal oscillator (Y1) in standby mode.</td>
<td>Inserted</td>
</tr>
<tr>
<td>R23, R12, R31</td>
<td>Sets the MCLK source for AD7760/AD7762 and EVAL-CED1Z</td>
<td>R23: a 0 Ω link routes the on-board oscillator to two parallel clock buffers in which one goes to MCLK and the other output goes to EVAL-CED1Z board to allow data acquisition using the supplied software. R12, R31: populate R31 to select external MCLK source through Connector J8. R12 may be use for termination of any external MCLK source.</td>
<td>R23</td>
</tr>
</tbody>
</table>
CONNECTING THE EVALUATION HARDWARE

Connecting the hardware is a five step process.

1. Apply power to the EVAL-CED1Z via the +7 V, 15 W power supply provided with the EVAL-CED1Z board. The green LED (labeled Power) on the EVAL-CED1Z lights up to indicate that the EVAL-CED1Z is receiving power. The USB cable can then be connected between the PC and the EVAL-CED1Z.

2. Connect the USB cable between the PC and the EVAL-CED1Z. A green LED positioned beside the USB connector on the EVAL-CED1Z board lights up, indicating that the USB connection has been established.

3. Power up the EVAL-AD7760EDZ/EVAL-AD7762EDZ through Connector J2. Connect a wire from the connector labeled V+ to 7.5 V of an external power supply. In addition, ensure that there is a GND connection between the GND of J2 and the power supply GND connection.

4. Connect the female connector (J3, marked CED1Z PPI), which is on the underside of the evaluation board, to the PPI header of the EVAL-CED1Z board.

5. Start the evaluation software.

The differential input to the AD7760/AD7762 device can be connected to the black XLR connector (J1) marked Differential Input. This differential input is routed to the inputs of the on-board differential amplifier for the device. Because the software powers up the device, do not apply an analog input until the device is fully powered up.

When the hardware is set up, use the software to control the EVAL-CED1Z and the EVAL-AD7760EDZ/EVAL-AD7762EDZ. Launch the software from the Analog Devices menu: from the AD7760_2 submenu, click the AD7760_2 icon.

Note that if an error message appears, click OK and restart the application after checking the connection between the adapter board and the USB port on the PC. Also check that the USB device is identified by the Device Manager, as detailed in the Installing the Software section.
USING THE EVALUATION SOFTWARE

After the hardware is initially installed, follow the instructions to set up the evaluation software each time the system is used. Note that the hardware must be powered up as described in the About the Evaluation Hardware section.

Figure 8. Front Panel Showing Control and Indicator Information and the Performance with a −0.5 dB, 1 kHz Input Tone in Decimate by 32 Mode when Running with the Default 40 MHz MCLK
OVERVIEW OF THE MAIN WINDOW

Refer to the front panel shown in Figure 8 when following these steps.

1. Find the default download location for the evaluation software by clicking Start > All Programs > Analog Devices > AD7760_2 > AD7760_2. For a location other than the default, follow the path entered during setup. The evaluation software GUI appears (see Figure 8).

2. Select the correct device: AD7760 or AD7762.

3. To power up the device under evaluation, click the Power Mode drop-down menu, and select Low Power or Normal Power. This prompts the EVAL-CED1Z to write to the AD7760/AD7762 registers and power up the device.

4. Note that the external voltage supply connected to the EVAL-AD7760EDZ/EVAL-AD7762EDZ shows ~240 mA in Normal Power mode and ~170 mA in Low Power mode. Seeing the current draw levels change when switching between the power modes also verifies that communication between the evaluation board and CED1 board is operational.

5. Change the decimation rate setting by clicking the Decimation Rate drop-down menu as shown in Figure 9. Note that the device powers up in a default decimation setting of 32. Changing the rate allows the user to vary the oversampling rate and implement the five on-chip decimation options offering output data rates ranging from 78 kHz to 2.5 MHz output for the AD7760.

6. Specify the Power Mode, Decimation Rate, and Number of Samples to be acquired (typically 65,536 samples) by using the drop-down menus on the software front panel. The software allows the number of samples specified by the user to be viewed as a waveform, histogram, or FFT.

7. Choosing the different decimation rates in the software controls writes to the AD7760/AD7762 Control Register 2 to change the amount of decimation used in the second internal FIR filter of the AD7760. This filter can be completely bypassed to enable decimate ×8 mode, or otherwise set to decimate from ×2 to ×32 to enable an overall decimation rate of 16 to 256 for the AD7760. Note that the AD7762 only operates in decimation rates of 32, 64, 128, and 256.

8. Click Sample or Continuous to show samples output by the evaluation board. Sample gives one set of samples, the length of which is determined by the Number of Samples selection on the software front panel. Clicking Continuous shows continuously updated samples of the analog input to the device.

9. Check the frequency of the DRDY pulse on an oscilloscope (test point marked DRDY) and ensure that it matches the frequency shown in the Output Data Rate text box in the software front panel.

10. Observe if the frequencies match. If at any stage these frequencies do not match, reset the EVAL-AD7760EDZ/EVAL-AD7762EDZ evaluation board by pressing the RESET push button on the evaluation board. Then, set the Decimation Rate in the software front panel to the correct default value.
WORKING IN MODULATOR MODE

To enter modulator mode,

1. Click **Modulator Enable** as shown in Figure 9. When in modulator mode, the green indicator beside the control button appears lit.

2. Evaluation of the AD7760 device when using this hardware and software allows the user to look at the direct raw modulator output from the device bypassing all of the internal FIR filtering.

3. Running in modulator mode allows the user to see the noise shaping provided by the AD7760 Σ-Δ modulator as shown in Figure 11.

4. Click **Modulator Enable** to exit modulator mode; the green indicator light goes off. Reset by clicking **Reset** and then set the **Decimation Rate** as desired to run with the internal default FIR filters.

![Figure 11. Modulator Mode Example of Noise Shaping Provided by the AD7760; the High Frequency Content of the Modulator Output Leads to the Coarse Nature of the Waveform Shown](image-url)
DOWNLOADING A USER DEFINED FILTER

The final stage of the AD7760/AD7762 FIR filters can be programmed to suit the specific requirements of the user. The filter designed must correspond with the requirements listed in the data sheet; it must be a symmetrical filter with an even number of coefficients. The number of coefficients can range from 12 to 96.

Keep the following points in mind:

- Due to the symmetry of the filter, the coefficients repeat. Therefore, only half of the coefficients are required to be sent to the AD7760/AD7762.
- The device software reads the coefficients from a text file and writes each coefficient to the AD7760/AD7762. The filter file must contain the correct checksum, which is also written to the ADC, and the file must be in the correct format.

An example of this format is shown in Figure 12. This example corresponds to the example digital filter in the device data sheet. Each of the 32-bit words (in this case, there are 12 words for the coefficients and the checksum) are in a hexadecimal format—there must be no spaces between the characters and no text, spaces, or notation before or after any of the hexadecimal words to be written. The software implements a text read from each line of the file and then translates this value to the correct binary 32-bit word to be written to the AD7760/AD7762 as per the description in the data sheet.

To download a filter,

1. Select the number of coefficients for download—this is half the filter length. Therefore, for example, for a 24 tap filter, select 12 from the drop-down selection shown in Figure 13.

![Figure 13. Number of Coefficients](image)

2. Click the folder icon and browse to the location of the filter text file. The installation placed a copy of the data sheet example at Program files/Analog Device/AD7760_2; this file is called filter_12c.txt.

![Figure 14. Browse to Select the Specific Text File](image)

3. Click Configure Filter to download the user defined filter.
4. Click Sample to acquire a batch of samples from the device.

The filter example used in the device data sheet shows a slower transition band. The FFT of this filter implementation is shown in Figure 15. As highlighted, the status bits output by the ADC show whether the filter file was downloaded correctly. The indicators for the DL_OK, FILT_OK and UFILT are all asserted to show a successful filter download.
CHANGE IN THE FILTER TRANSITION BAND FOR CUSTOM FILTER

STATUS BITS INDICATE:
- DL_OK ASSERTED
- FILT_OK ASSERTED
- UFILT ASSERTED

THIS SHOWS THAT A USER DEFINED FILTER IS IN USE AND THAT IT WAS DOWNLOADED CORRECTLY.

Figure 15. User Defined Filter Example Implemented on Evaluation Board, Note Illuminated Indicators and Custom Filter Transition Band
WRITING TO GAIN, OFFSET, AND OVERRANGE REGISTERS

The evaluation board allows the user to write to the on-board registers for control of gain correction, offset correction, and the setting of the overrange flag.

For example, the default value of the gain correction register, 1.25, can be changed to a value of 1.00 by setting the value in the WR_GAIN box to 1.00. Click the white WR_GAIN switch on the front panel to write to the gain register.

To check that the value has been written correctly, click the white RD_GAIN switch on the front panel. The value of the gain register is shown in the RD_GAIN indicator box.

Figure 16. Writing to the On-Board Registers
Figure 18. EVAL-AD7760EDZ/EVAL-AD7762EDZ Schematic—Power Supply Section
Figure 19. EVAL-AD7760EDZ/EVAL-AD7762EDZ Schematic—Interface Section
Figure 20. EVAL-AD7760EDZ/EVAL-AD7762EDZ Component Side Top Silkscreen Artwork

Figure 21. EVAL-AD7760EDZ/EVAL-AD7762EDZ Component Side Layer 1 Artwork
Figure 22. EVAL-AD7760EDZ/EVAL-AD7762EDZ Ground Plane Layer 2 Artwork

Figure 23. EVAL-AD7760EDZ/EVAL-AD7762EDZ Power Plane Layer 2 Artwork
Figure 24. EVAL-AD7760EDZ/EVAL-AD7762EDZ Solder Side Layer 4 Artwork

Figure 25. EVAL-AD7760EDZ/EVAL-AD7762EDZ Component Side Bottom Silkscreen Artwork
## BILL OF MATERIALS

### Table 2.

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Part Number</th>
<th>Part Description</th>
<th>Stock Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>+7V5, /SYNC, 2VSD, 5VD, AVDD1, AVDD2, AVDD3, AVDD4, CS, DRDY, DVDD, GND, GND1 to GND3, MCLK_ADC, MCLK_FPGA, RD/WR, VDD_U5, VDRIVE</td>
<td>Test point, holes must be left free of solder</td>
<td>Do not insert</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C1, C2, C14</td>
<td>33 pF</td>
<td>0603A3301AT2A</td>
<td>50 V, NPO, multilayer ceramic capacitor</td>
<td>FEC 498555</td>
</tr>
<tr>
<td>C3</td>
<td>2.2 pF</td>
<td>CC0603CNPO9BN2R2</td>
<td>50 V, NPO, multilayer ceramic capacitor</td>
<td>FEC 721888</td>
</tr>
<tr>
<td>C4 to C6, C9, C56, C58, C62</td>
<td>0.1 µF</td>
<td>B0603R104KCT</td>
<td>16 V, X7R, multilayer ceramic capacitor</td>
<td>FEC 9406140</td>
</tr>
<tr>
<td>C7, C48, C50, C52 to C54, C57</td>
<td>0.1 µF</td>
<td>CC0402ZRY5V7BB104</td>
<td>16 V, Y5V, multilayer ceramic capacitor</td>
<td>FEC 3019482</td>
</tr>
<tr>
<td>C10, C13</td>
<td>DNI</td>
<td>Not applicable</td>
<td>Optional capacitor footprint (0805)</td>
<td>Do not insert</td>
</tr>
<tr>
<td>C11</td>
<td>100 µF</td>
<td>TAJC107K010RNJ</td>
<td>10 V, tantalum capacitor</td>
<td>FEC 197180</td>
</tr>
<tr>
<td>C15, C32 to C34, C39, C61, C64, C65, C72, C84</td>
<td>DNI</td>
<td>Not applicable</td>
<td>PTH capacitor location</td>
<td>Do not insert</td>
</tr>
<tr>
<td>C16</td>
<td>47 pF</td>
<td>TAJD476K020RNJ</td>
<td>20 V, tantalum capacitor</td>
<td>FEC 197464</td>
</tr>
<tr>
<td>C17</td>
<td>22 pF</td>
<td>GRM1555C1H220JZ01D</td>
<td>50 V, C0G, multilayer ceramic capacitor</td>
<td>FEC 8819629</td>
</tr>
<tr>
<td>C19, C21, C23, C25, C27, C29, C43 to C45, C47, C83</td>
<td>0.1 µF</td>
<td>U0805R104KCT</td>
<td>50 V, X7R, multilayer ceramic capacitor</td>
<td>FEC 9406387</td>
</tr>
<tr>
<td>C20, C22</td>
<td>100 µF</td>
<td>TAJB106K020RNJ</td>
<td>20 V, tantalum capacitor</td>
<td>FEC 197427</td>
</tr>
<tr>
<td>C42</td>
<td>DNI</td>
<td>Not applicable</td>
<td>Optional capacitor footprint (0805)</td>
<td>Do not insert</td>
</tr>
<tr>
<td>C46</td>
<td>10 nF</td>
<td>CM05X7R103K16AH</td>
<td>16 V, X7R, multilayer ceramic capacitor</td>
<td>FEC 9527710</td>
</tr>
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<td>C59</td>
<td>0.1 µF</td>
<td>U0603C101JCT</td>
<td>2 A, rectifier diode</td>
<td>FEC 9843876</td>
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<tr>
<td>C88, C90, C93, C94</td>
<td>10 nF</td>
<td>CC0603KRX7R8BB103</td>
<td>50 V, X7R, multilayer ceramic capacitor</td>
<td>FEC 9406115</td>
</tr>
<tr>
<td>D1</td>
<td>200 µH</td>
<td>74279266LF</td>
<td>Inductor</td>
<td>FEC 7992033</td>
</tr>
<tr>
<td>J1 to J10</td>
<td>100 Ω</td>
<td>72479266LF</td>
<td>Inductor</td>
<td>FEC 4194512</td>
</tr>
<tr>
<td>J1</td>
<td>NC3FAH1-1</td>
<td>XLR female audio connector</td>
<td>Do not insert</td>
<td></td>
</tr>
<tr>
<td>J2</td>
<td>CB5000/2</td>
<td>2-pin, terminal block (5 mm pitch)</td>
<td>Do not insert</td>
<td></td>
</tr>
<tr>
<td>J3</td>
<td>M20-7832046</td>
<td>40-pin (2 × 20) DIL vertical socket</td>
<td>Do not insert</td>
<td></td>
</tr>
<tr>
<td>J6, J8, J12</td>
<td>1 nF</td>
<td>R114426000</td>
<td>50 Q, SMB jack</td>
<td>FEC 9528202</td>
</tr>
<tr>
<td>L1 to L8, L10 to L14</td>
<td>1 nF</td>
<td>2-pin (0.1&quot; pitch) header and shorting shunt</td>
<td>Do not insert</td>
<td></td>
</tr>
<tr>
<td>L9</td>
<td>200 µH</td>
<td>B28496C3100J</td>
<td>Inductor</td>
<td>FEC 1022247</td>
</tr>
<tr>
<td>LK1</td>
<td>10 nH</td>
<td>M20-9990246</td>
<td>Inductor</td>
<td>FEC 3877024</td>
</tr>
<tr>
<td>R1, R2</td>
<td>649 Ω</td>
<td>RN73C1J649RBTG</td>
<td>Precision SMD resistor</td>
<td>FEC 1140503</td>
</tr>
<tr>
<td>R3, R4</td>
<td>1 kΩ</td>
<td>RN73C1J1K0BTG</td>
<td>Precision SMD resistor</td>
<td>FEC 1140509</td>
</tr>
<tr>
<td>R34</td>
<td>220 kΩ</td>
<td>RN73C1J17R8BTG</td>
<td>Precision SMD resistor</td>
<td>FEC 1140429</td>
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<tr>
<td>R5, R6</td>
<td>18 Ω</td>
<td>RN73C1J7R8BTG</td>
<td>Precision SMD resistor</td>
<td>FEC 9330364</td>
</tr>
<tr>
<td>R7, R8, R35</td>
<td>0.063W 0603 1% 100 Ω</td>
<td>SMD resistor</td>
<td>FEC 9330364</td>
<td></td>
</tr>
<tr>
<td>R9</td>
<td>18 Ω</td>
<td>MC 0.063W 0603 5% 18 Ω</td>
<td>SMD resistor</td>
<td>FEC 9331840</td>
</tr>
<tr>
<td>R10, R11, R14 to R16, R18, R21 to R25, R29, R32, R33, R40 to R44, R46</td>
<td>0 Ω</td>
<td>MC 0.063W 0603 0R</td>
<td>SMD resistor</td>
<td>FEC 9331662</td>
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<tr>
<td>R12, R31, R45</td>
<td>DNI</td>
<td>Not applicable</td>
<td>SMD resistor</td>
<td>Do not insert</td>
</tr>
<tr>
<td>R16</td>
<td>1 Ω</td>
<td>RC0603FR-071RL</td>
<td>SMD resistor</td>
<td>FEC 9238123</td>
</tr>
<tr>
<td>R19</td>
<td>160 kΩ</td>
<td>MC 0.063W 0603 1% 160 kΩ</td>
<td>SMD resistor</td>
<td>FEC 9330682</td>
</tr>
<tr>
<td>R20, R26 to R28</td>
<td>10 Ω</td>
<td>MC 0.063W 0603 1% 10 kΩ</td>
<td>SMD resistor</td>
<td>FEC 9330399</td>
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<td>R30</td>
<td>100 Ω</td>
<td>RC0402FR-07100RL</td>
<td>SMD resistor</td>
<td>FEC 9239111</td>
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<td>R34</td>
<td>220 kΩ</td>
<td>MC 0.063W 0603 1% 220 kΩ</td>
<td>SMD resistor</td>
<td>FEC 9330836</td>
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<td>R36</td>
<td>68 kΩ</td>
<td>MC 0.063W 0603 1% 68 kΩ</td>
<td>SMD resistor</td>
<td>FEC 9331468</td>
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<td>R37</td>
<td>110 kΩ</td>
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<td>SMD resistor</td>
<td>FEC 9330461</td>
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<td>R38</td>
<td>10 Ω</td>
<td>MC 0.063W 0603 1% 10 Ω</td>
<td>SMD resistor</td>
<td>FEC 9330429</td>
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</table>
Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. If injury, damage or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board.

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<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Part Number</th>
<th>Part Description</th>
<th>Stock Code1</th>
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<td>R39</td>
<td>100 kΩ</td>
<td>MC 0.063W 0603 1% 100 kΩ</td>
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<td>S1</td>
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<td>B35-1000</td>
<td>SMD push button switch (sealed 6 mm x 6 mm)</td>
<td>FEC 177-807</td>
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<td>U1</td>
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<td>AD7760BSVZ/AD7762BSVZ</td>
<td>AD7760/AD7762 analog-to-digital converter</td>
<td>AD7760BSVZ/</td>
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<td></td>
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<td></td>
<td>AD7762BSVZ</td>
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<tr>
<td>U2, U5</td>
<td></td>
<td>NC7S208MS5</td>
<td>Single AND gate</td>
<td>FEC 1013807</td>
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<tr>
<td>U3</td>
<td></td>
<td>ADR434ARZ</td>
<td>Ultralow noise XFET voltage references</td>
<td>ADR434ARK</td>
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<td>U4</td>
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<td>ADP3330ARTZ-2.5</td>
<td>Low dropout regulator</td>
<td>ADP3330ARTZ-2.5</td>
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<td>U6, U9</td>
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<td>ADP3334ARMZ</td>
<td>Adjustable LDO regulator</td>
<td>ADP3334ARMZ-REEL7</td>
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<td>ADP3330ARTZ-5</td>
<td>Low dropout regulator</td>
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<td>U12</td>
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<td>SN74LVCO8APWR</td>
<td>Quad, two-input, positive AND gate</td>
<td>FEC 1102978</td>
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<td>U14</td>
<td></td>
<td>ADM6711ZAKSZ</td>
<td>Reset generator</td>
<td>ADM6711ZAKSZ</td>
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<td>X1 to X4</td>
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<td></td>
<td>PCB standoff (0.156&quot; hole)</td>
<td>Do not insert</td>
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<tr>
<td>Y1</td>
<td>40 MHz</td>
<td>MX045HS400M0000</td>
<td>HCMOS/TTL clock oscillator</td>
<td>Digi-Key CTK175-ND</td>
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<tr>
<td>Y1 (alternate)</td>
<td>40 MHz</td>
<td>MS06122</td>
<td>40.0 MHz, GXO-U100H/B, 5 V, half size, ±50 ppm stability, 0 + 70°</td>
<td>Second source P/N for Y1</td>
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</table>

1 The FEC stock code notation refers to the stock order code for that component from Farnell Element 14.

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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