Evaluating the AD7380 16-Bit and AD7381 14-Bit, 2-Channel, Simultaneous Sampling, Successive Approximation ADCs

FEATURES
Full featured evaluation board multichannel, simultaneous sampling ADC
On-board reference, reference buffer, and ADC driver
On-board power supplies
Board-compatible, high speed system demonstration platform (SDP-H1) controller
PC software for control and data analysis

EVALUATION KIT CONTENTS
EVAL-AD7380FMCZ or EVAL-AD7381FMCZ evaluation board
Instructions to download software

ADDITIONAL EQUIPMENT NEEDED
EVAL-SDP-CH1Z
Signal source
PC running Windows® Vista SP2 (32-bit or 64-bit), Windows 7 SP1 (32-bit or 64-bit), Windows 8.1 (32-bit or 64-bit), or Windows 10 (32-bit or 64-bit) with a USB 2.0 port

ONLINE RESOURCES
AD7380/AD7381 data sheet
ACE evaluation software
AD738x ACE plug-in

GENERAL DESCRIPTION
The EVAL-AD7380FMCZ and EVAL-AD7381FMCZ are full featured evaluation boards that evaluate all features of the AD7380 and AD7381 analog-to-digital converters (ADCs). The evaluation boards can be controlled by the EVAL-SDP-CH1Z via the 160-way system demonstration platform (SDP) connector, J4. The EVAL-SDP-CH1Z board controls the evaluation boards through the USB port of a PC using the Analysis, Control, Evaluation (ACE) software, which is available for download from the ACE software page.

Complete specifications for the AD7380 and AD7381 are provided in the AD7380/AD7381 data sheet. Consult these specifications in conjunction with this user guide when using the evaluation boards. Full details on the EVAL-SDP-CH1Z are available on the SDP-H1 product page. The comprehensive ACE user guide is available on the ACE software page.

The EVAL-AD7380FMCZ can be used to evaluate the AD4680 and AD4681. The AD4680 and AD4681 have slower throughput rates (at 1 MSPS and 500 kSPS, respectively) than the AD7380. The throughput can be adjusted to fit for AD4680 and AD4681 by adjusting the clock speed and the sampling frequency.

Figure 1 shows the typical setup of the EVAL-AD7380FMCZ board. The setup for the EVAL-AD7381FMCZ board is the same as the EVAL-AD7380FMCZ setup.

Figure 1. Typical Setup of the EVAL-AD7380FMCZ (Left) and the EVAL-SDP-CH1Z (Right)
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# REVISION HISTORY

10/2020—Rev. 0 to Rev. A
Changes to General Description ....................................................... 1

1/2019—Revision 0: Initial Version
The EVAL-AD7380FMCZ and EVAL-AD7381FMCZ are powered by the EVAL-SDP-CH1Z board by default. External power supplies can be applied. See Table 1 for a description of connectors and Table 2 for the link configuration required. To evaluate the AD7380 and AD7381, take the following steps:

1. Download and install the ACE software, available on the AD7380/AD7381 product page. Details of this installation are available on the internal label of the evaluation board box. Ensure that the EVAL-SDP-CH1Z board is disconnected from the USB port of the PC while installing the software. The PC may need to be restarted after the installation.

2. Ensure that the link options are configured as detailed in Table 2.

3. Connect the EVAL-SDP-CH1Z board to the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ, as shown in Figure 2.

4. Connect the EVAL-SDP-CH1Z board to the PC via the USB cable. Choose to automatically search for the drivers for the EVAL-SDP-CH1Z board if prompted by the operating system.

5. Launch the ACE evaluation software from the ACE subfolder in the Analog Devices folder in the All Programs menu.

6. Connect an input signal to Channel A or Channel B.
EVALUATION BOARD HARDWARE

AD7380/AD7381 DESCRIPTION

The 16-bit AD7380 and 14-bit AD7381 are dual, simultaneous sampling, high speed, low power, successive approximation ADCs that operate from a 3.3 V power supply and feature throughput rates of 4 MSPS. The analog input type is differential. The AD7380/AD7381 can accept a wide common mode input voltage and is sampled and converted on the falling edge of CS.

The AD7380/AD7381 has optional, integrated, on-chip oversampling blocks to improve dynamic range and reduce noise at lower bandwidths. An internal 2.5 V reference is included on the device. Alternatively, an external reference up to 3.3 V can be used.

The conversion process and data acquisition use standard control inputs, allowing for easy interfacing to microprocessors or digital signal processors (DSPs). The AD7380/AD7381 is compatible with 1.8 V, 2.5 V, and 3.3 V interfaces using the separate logic supply.

The AD7380/AD7381 is available in a 16-lead LFCSP package with operation specified from −40°C to +125°C.

POWER SUPPLIES

Ensure that all link positions are set according to the required operating mode before applying power and signals to the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ. See Table 2 for the complete list of link options.

The EVAL-AD7380FMCZ and EVAL-AD7381FMCZ are powered by the EVAL-SDP-CH1Z board by default. External power supplies can be applied to the board. See Table 1 for a description of the connectors used and Table 2 for the link configurations required.

Table 1. Optional External Power Supplies

<table>
<thead>
<tr>
<th>Power Supply</th>
<th>Connector</th>
<th>Voltage Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 V</td>
<td>P4-1</td>
<td>12 V, ±10%</td>
<td>Main board power supply for all internal voltage regulators</td>
</tr>
<tr>
<td>GND</td>
<td>P4-2</td>
<td>0 V</td>
<td>Ground</td>
</tr>
<tr>
<td>Vcc</td>
<td>P5-1</td>
<td>3.0 V to 3.6 V</td>
<td>ADC analog power supply</td>
</tr>
<tr>
<td>GND</td>
<td>P5-2</td>
<td>0 V</td>
<td>Ground</td>
</tr>
<tr>
<td>Vlogic</td>
<td>P5-3</td>
<td>1.65 V to 3.6 V</td>
<td>Digital serial peripheral input power supply</td>
</tr>
<tr>
<td>Amp_PWR+</td>
<td>P6-1</td>
<td>5 V, ±5%</td>
<td>Amplifier positive power supply</td>
</tr>
<tr>
<td>GND</td>
<td>P6-2</td>
<td>0 V</td>
<td>Ground</td>
</tr>
<tr>
<td>Amp_PWR−</td>
<td>P6-3</td>
<td>−2.5 V ±5%</td>
<td>Amplifier negative power supply</td>
</tr>
</tbody>
</table>

Figure 3. EVAL-AD7380FMCZ and EVAL-AD7381FMCZ Functional Block Diagram
LINK CONFIGURATION OPTIONS

Multiple link options must be set correctly to select the appropriate operating setup before using the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ. The functions of these options are detailed in Table 2.

Setup Conditions

Ensure that all link positions are set as required by the selected operating mode before applying power and signals to the evaluation boards. Table 2 shows the default positions of the links when the EVAL-AD7380FMCZ and EVAL-AD7381FMCZ are packaged.

Table 2. Link Options for EVAL-AD7380FMCZ and EVAL-AD7381FMCZ

<table>
<thead>
<tr>
<th>Link Name</th>
<th>Function</th>
<th>Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>AMP_PWR−</td>
<td>1</td>
<td>Use internal −2.5 V from U9 for AMP_PWR−.</td>
</tr>
<tr>
<td>LK2</td>
<td>AMP_PWR+</td>
<td>1</td>
<td>Use internal 5 V from U8 for AMP_PWR+.</td>
</tr>
<tr>
<td>LK3</td>
<td>Ext 12V</td>
<td>1</td>
<td>Use 12 V power supply from SDP.</td>
</tr>
<tr>
<td>LK4</td>
<td>VREF</td>
<td>3</td>
<td>Use internal +3V3 from U3 for VREF.</td>
</tr>
<tr>
<td>LK5</td>
<td>VLogic</td>
<td>3</td>
<td>Use internal 2.3 V from U6 for VLogic.</td>
</tr>
<tr>
<td>JP2</td>
<td>AINA−</td>
<td>1 (SMD RES)</td>
<td>Connect internal signal from A2 to ADC U10 input AINA−.</td>
</tr>
<tr>
<td>JP3</td>
<td>AINA+</td>
<td>1 (SMD RES)</td>
<td>Connect internal signal from A2 to ADC U10 input AINA+.</td>
</tr>
<tr>
<td>JP4</td>
<td>REFIO</td>
<td>3 (SMD RES)</td>
<td>The REFIO pin is driven with the external on board reference.</td>
</tr>
<tr>
<td>JP5</td>
<td>Vcc</td>
<td>1</td>
<td>Use internal +3V3 from U2 for Vcc.</td>
</tr>
<tr>
<td>JP6</td>
<td>AINA+</td>
<td>1 (SMD RES)</td>
<td>Connect external SMB Connector J2 to the A1 buffer amplifier.</td>
</tr>
</tbody>
</table>

1 SMD RES is a surface-mount device resistor.
EVALUATION BOARD CIRCUITRY
SOCKETS AND CONNECTORS
The connectors and sockets on the EVAL-AD7380FMCZ and EVAL-AD7381FMCZ are described in Table 3.

The default interface to this evaluation board is via the 160-way connector, which connects the EVAL-AD7380FMCZ and EVAL-AD7381FMCZ to the EVAL-SDP-CH1Z. If using the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ in standalone mode, communication is achieved via the J6 header pins.

<table>
<thead>
<tr>
<th>Connector</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Analog input</td>
</tr>
<tr>
<td>J2</td>
<td>Analog input</td>
</tr>
<tr>
<td>J3</td>
<td>Analog input</td>
</tr>
<tr>
<td>J4</td>
<td>Analog input</td>
</tr>
<tr>
<td>P1</td>
<td>Amplifier mezzanine card inputs</td>
</tr>
<tr>
<td>P2</td>
<td>Amplifier mezzanine card outputs</td>
</tr>
<tr>
<td>P3</td>
<td>Digital SPI signals</td>
</tr>
<tr>
<td>P4</td>
<td>Main board power supply for all internal voltage regulators</td>
</tr>
<tr>
<td>P5</td>
<td>ADC power supply and digital SPI power supply</td>
</tr>
<tr>
<td>P6</td>
<td>Amplifier power supply</td>
</tr>
<tr>
<td>P7</td>
<td>Field-programmable gate array (FPGA) mezzanine card (FMC) to low pin count (LPC) connector</td>
</tr>
<tr>
<td>EXT_REF</td>
<td>External voltage reference</td>
</tr>
</tbody>
</table>

TEST POINTS
There are several test points and single in line (SIL) headers on the EVAL-AD7380FMCZ and EVAL-AD7381FMCZ. These test points provide access to the signals from the evaluation board for probing, evaluation, and debugging.
EVALUATION BOARD SOFTWARE
SOFTWARE INSTALLATION PROCEDURES

Download the ACE evaluation software from the AD7380/AD7381 product page and install on a PC before using the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ evaluation board.

There are two steps to the installation process:

1. ACE evaluation software installation
2. EVAL-SDP-CH1Z driver installation

Warning

The evaluation board software and drivers must be installed before connecting the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ and the EVAL-SDP-CH1Z to the USB port of the PC to ensure that the evaluation system is properly recognized when it is connected to the PC.

Installing the ACE Evaluation Software

To install the ACE evaluation software, take the following steps:

1. Download the ACE evaluation software to a Windows-based PC.
2. Double-click the ACEInstall.exe file to begin the installation. By default, the software is saved to the following location: C:\Program Files (x86)\Analog Devices\ACE.
3. A dialog box appears asking for permission to allow the program to make changes to the PC. Click Yes to begin the installation process.
4. Click Next > to continue the installation, as shown in Figure 4.

5. Read the license and click I Agree.

6. Choose the install location and click Next >.

7. The components to install are preselected. Click Install.
8. The **Windows Security** window appears. Click **Install**.

![Image of the Windows Security window]

**Figure 8. Windows Security Window**

9. The installation is in progress. No action is required.

![Image of the installation in progress]

**Figure 9. Installation in Progress**

10. When the installation is complete, click **Next >**, and then click **Finish** to complete.

![Image of the installation complete]

**Figure 10. Installation Complete**

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**EVALUATION BOARD SETUP PROCEDURES**

The EVAL-AD7380FMCZ and EVAL-AD7381FMCZ connect to the **EVAL-SDP-CH1Z**. The **EVAL-SDP-CH1Z** is the controller board, which is the communication link between the PC and the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ. Figure 2 shows a diagram of the connections between the EVAL-AD7380FMCZ evaluation board and the **EVAL-SDP-CH1Z**.

After following the instructions in the Software Installation Procedures section, set up the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ and **EVAL-SDP-CH1Z** as detailed in the Connecting the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ and the **EVAL-SDP-CH1Z** to a PC section.

The evaluation software and drivers must be installed before connecting the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ and **EVAL-SDP-CH1Z** to the USB port of the PC. Installing the software and drivers prior to connection ensures that the evaluation system is correctly recognized when it is connected to the PC.

**Connecting the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ and the EVAL-SDP-CH1Z to a PC**

1. Ensure that all configuration links are in the appropriate positions, as detailed in Table 2.
2. Connect the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ board securely to the 160-way connector on the **EVAL-SDP-CH1Z**.
3. The EVAL-AD7380FMCZ and EVAL-AD7381FMCZ boards do not require an external power supply adapter.
4. Connect the **EVAL-SDP-CH1Z** board to the PC via the USB cable enclosed in the **EVAL-SDP-CH1Z** kit.

**Verifying the Board Connection**

1. Allow the **Found New Hardware Wizard** to run after the **EVAL-SDP-CH1Z** board is plugged into the PC. Choose to automatically search for the drivers for the **EVAL-SDP-CH1Z** board if prompted by the operating system.
2. Confirm that the evaluation board is connected to the PC correctly using the **Device Manager** window. A dialog box may appear asking for permission to allow the program to make changes to the computer. Click **Yes**. The **Computer Management** window appears. From the list labeled **System Tools**, click **Device Manager**.
3. If the **EVAL-SDP-CH1Z** driver software is installed and the board is connected to the PC correctly, **Analog Devices SDP-H1** appears nested under **ADI Development Tools** in the **Device Manager** window, as shown in Figure 11.
Figure 11. *Device Manager* Window

**Disconnecting the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ**

Always disconnect power from the EVAL-SDP-CH1Z or press the reset tact switch located alongside the mini USB port before removing the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ evaluation board.
AD7380/AD7381 EVALUATION SOFTWARE OPERATION

LAUNCHING THE SOFTWARE

After the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ and EVAL-SDP-CH1Z boards are correctly connected to the PC, launch the ACE evaluation software.

1. From the Start menu, select All Programs > Analog Devices > ACE > ACE.exe, which brings up the window shown in Figure 12.

2. If the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ evaluation board is not connected to the USB port via the EVAL-SDP-CH1Z when the software is launched, the AD7380 Eval Board icon does not show up in the Attached Hardware section. Connect the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ and the EVAL-SDP-CH1Z to the USB port of the PC and wait a few seconds, and then follow the instructions that appear in the dialogue box.

3. Double click the AD7380 Eval Board icon to view the window shown in Figure 13.

4. Double click the AD7380 chip icon to access the window shown in Figure 14.

5. Click Software Defaults and then click Apply Changes.

DESCRIPTION OF CHIP VIEW

After completing the steps in the Software Installation Procedures section and the Evaluation Board Setup Procedures section, set up the system for data capture.

1. Block icons that are dark blue are programmable blocks. Clicking a dark blue block icon opens a configurable pop-up window that allows customization for the data capture, as shown for the over sampling block in Figure 15.

2. Type the value of reference voltage in the Reference voltage box when External Reference is selected. The default value for the external reference is set to 3.3 V, and 2.5 V for the internal reference.
Figure 13. Board View

Figure 14. Chip View
Figure 15. Pop-Up Configurable Window

Figure 16. Memory Map View
DESCRIPTION OF MEMORY MAP WINDOW

Click Proceed to Memory Map in the chip view to open the window shown in Figure 16. The memory map shows all registers of the AD7380/AD7381.

Apply Changes

The registers are in default values when powered up. To implement the values changed in all of the registers, click Apply Changes to write to the registers.

Apply Selected

In some cases, the values of every register have been changed, but the user wants to implement changes on a selected register only. Click Apply Selected to write the new value on the selected register to the AD7380 or AD7381.

Read All

Clicking Read All results in a read of the values of all the registers from the chip.

Read Selected

Clicking Read Selected results in a read of the selected register from the chip.

Reset Chip

Clicking Reset Chip causes the software to reset the AD7380 or AD7381.

Diff

Clicking Diff checks for difference in register values between software and chip.

Software Defaults

To revert the register values back to their defaults, click Software Default, and then click Apply Changes to write to the AD7380 or AD7381.

![Figure 17. Analysis View](image-url)
DESCRIPTION OF ANALYSIS WINDOW

Click **Proceed to Analysis** in the chip view to open the window, as shown in Figure 17. The analysis view contains the Waveform tab, Histogram tab, and FFT tab.

WAVEFORM TAB

The **Waveform** tab displays data in form of time vs. discrete data values with the results, as shown in Figure 18. The **Capture** pane contains capture settings, which reflect into the registers automatically before data capture.

**Capture**

**General Capture Settings**

The **Sample Count** list allows the user to select the number of samples per channel per capture.

The **SPI Frequency(Mhz)** list allows the user to select the SPI clock frequency used to transfer data between the FPGA device and the AD7380/AD7381 during device register reads and writes and during data capture. This frequency must be set relatively higher than the set throughput rate.

The user can enter the input sample frequency in kSPS in the **Sample Frequency(KSPS)** box. Refer to the AD7380/AD7381 data sheet to determine the maximum sampling frequency for the selected mode.

**Device Settings**

The **Over Sampling Ratio** list, when enabled, can be set between 2 to 32 and provides improved signal-to-noise ratio (SNR) performance. Refer to the AD7380/AD7381 data sheet to determine the maximum oversampling ratio for the selected oversampling mode.

Select **18-Bit Resolution** to enter 18-bit resolution mode. The resolution boost is used in conjunction with the oversampling rate to provide two extra bits of resolution.

The **Over Sampling Mode** list allows the user to select the mode of oversampling. This setting is only applicable when oversampling is enabled.

**Run Once**

Click **Run Once** to start a data capture of the samples at the sample rate specified in the **Sample Count** list. These samples are stored on the FPGA device and are only transferred to the PC when the sample frame is complete.

Run Continuously

Click **Run Continuously** to start a data capture that gathers samples continuously with one batch of data at a time. The **Run Once** operation is run continuously.

**Results**

**Display Channels**

**Display Channels** allows the user to select the channels to capture. The channel data is shown only if that channel is selected before the capture.

**Waveform Results**

**Waveform Results** displays amplitude, sample frequency, and noise analysis data for the selected channels.

**Export Capture Data**

Click **Export Capture Data** to export captured data. The waveform, histogram, and FFT data is stored in .xml files along with the values of parameters at capture.

**Waveform Graph**

The data waveform graph shows each successive sample of the ADC output. The user can zoom and pan the waveform using the embedded waveform tools. The channels to display can be selected in **Display Channels**.

**Display Units and Axis Controls**

Click the **Display Units** dropdown list to select whether the data graph displays in units of Hex, volts, or codes. The axis controls are dynamic.

When selecting either y-scale dynamic or x-scale dynamic, the corresponding axis width automatically adjusts to show the entire range of the ADC results after each batch of samples.

HISTOGRAM TAB

The **Histogram** tab contains the histogram graph and the results pane, as shown in Figure 19.

**Results**

**Results** displays the information related to the dc performance.

**Histogram Graph**

The histogram graph displays the number of hits per code within the sampled data. This graph is useful for dc analysis, and indicates the noise performance of the device.
Figure 18. Waveform Tab

Figure 19. Histogram Tab
Figure 20 shows the FFT tab, which displays fast Fourier transform (FFT) information for the last batch of samples gathered.

**FFT TAB**

**Analysis**

**General Settings**

The General Settings pane allows the user to set up the preferred configuration of the FFT analysis, including how many tones are analyzed. The fundamental is set manually.

**Windowing**

The Windowing pane allows the user to select the windowing type used in the FFT analysis, the number of harmonic bins, and the number of fundamental bins that must be included.

**Single Tone Analysis and Two Tone Analysis**

The Single Tone Analysis and Two Tone Analysis panes allow the user to select the fundamental frequency included in the FFT analysis. Use Two Tone Analysis when there are two frequencies that must be analyzed.

**Results**

**Signal**

The Signal pane displays the sample frequency, fundamental frequency, and fundamental power.

**Noise**

The Noise pane displays the SNR and other noise performance results.

**Distortion**

The Distortion pane displays the harmonic content of the sampled signal and dc power when viewing the FFT analysis.

**EXITING THE SOFTWARE**

To exit the software, click File and then click Exit.
NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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