Evaluating the **AD7172-2** Low Power, 24-Bit, 31.25 kSPS, Sigma-Delta ADC with True Rail-to-Rail Buffers

**FEATURES**
- Full featured evaluation board for the AD7172-2
- PC control in conjunction with the system demonstration platform (SDP), see the EVAL-SDP-CB1Z data sheet for additional information
- PC software for control and data analysis (time domain)
- Standalone capability

**EVALUATION KIT CONTENTS**
- AD7172-2
- EVAL-AD7172-2SDZ evaluation board
- AD717x Eval+ evaluation software (CD)
- 7 V to 9 V ac-to-dc adapter
- Plastic screw and washer set

**EQUIPMENT NEEDED**
- DC signal source
- PC running Windows XP, Windows 8, or Windows 10

**GENERAL DESCRIPTION**

The EVAL-AD7172-2SDZ evaluation kit features the AD7172-2, a 24-bit, 31.25 kSPS analog-to-digital converter (ADC) with integrated rail-to-rail analog input buffers, on-board power supply regulation, and an external amplifier section for amplifier evaluation. A 7 V to 9 V ac-to-dc adapter is regulated to 5 V and 3.3 V; this supplies the AD7172-2 and supports its components. The EVAL-AD7172-2SDZ connects to a USB port via the EVAL-SDP-CB1Z (SDP-B) controller board.

The AD717x Eval+ software fully configures the AD7172-2 device functionality via an interactive block diagram and a user accessible register interface, and provides dc time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

For full specifications, see the AD7172-2 data sheet, which must be consulted in conjunction with this user guide when using the evaluation board.

**EVAL-AD7172-2SDZ BLOCK DIAGRAM**

![EVAL-AD7172-2SDZ Block Diagram](Figure 1)
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3/2015—Revision 0: Initial Version
EVAL-AD7172-2SDZ QUICK START GUIDE

RECOMMENDED QUICK START GUIDE

To set up the evaluation board, take the following steps:

1. Disconnect the SDP-B board from the USB port of the PC.
2. Install the AD717x Eval+ software from the enclosed CD.
3. Restart the PC after installation.
4. Connect the SDP-B board to the evaluation board, as shown in Figure 2.
5. Fasten the evaluation board to the SDP-B board with the enclosed plastic screw and washer set.
6. Connect the external 9 V power supply to the J5 connector of the evaluation board, as shown in Figure 2. Set LK2 to Position B.
7. Connect the SDP-B board to the PC via the USB cable. For PCs using Windows® XP, it can be necessary to search for the SDP-B drivers. If prompted by the Windows operating system, choose to automatically search for the drivers for the SDP-B board.
8. Launch the AD717x Eval+ software from the Analog Devices subfolder in the Programs menu.

QUICK START NOISE TEST

To test the noise performance, take the following steps:

1. Insert Link LK8 to Link LK12 to initiate the noise performance test mode. In this mode, the analog input channels short to the REFOUT pin.
2. Click Sample to acquire samples from the ADC (see Figure 16).

The Samples text field in the top right corner of the main window sets the number of samples collected in each batch (see Figure 16).

Figure 2. Hardware Configuration, Setting Up the EVAL-AD7172-2SDZ
EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7172-2 is a highly accurate, high resolution, multiplexed, 2-/4-channel (fully differential/single-ended) Sigma-Delta ADC. The AD7172-2 has a maximum channel-to-channel scan rate of 6.21 kSPS (161 µs) for fully settled data. The output data rates range from 1.25 SPS to 31.25 kSPS. The device includes integrated rail-to-rail analog input and reference input buffers, an integrated precision 2.5 V reference, and an integrated oscillator.

See the AD7172-2 data sheet for complete specifications. Full details for the SDP-B board are available on the SDP-B product page on the Analog Devices website.

Table 1. Default Link and Solder Link Options

<table>
<thead>
<tr>
<th>Link</th>
<th>Default Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>A</td>
<td>Selects the voltage applied to the power supply sequencer circuit (U3); dependent on AVDD1. Place in Position A if using a 5 V supply for AVDD1, or Position B if using a 2.5 V supply for AVDD1.</td>
</tr>
<tr>
<td>LK2</td>
<td>B</td>
<td>Selects the external power supply from Connector J3 (Position A) or Connector J5 (Position B).</td>
</tr>
<tr>
<td>LK3 to LK7</td>
<td>Not inserted</td>
<td>Prior to inserting SL8 to SL11, inserting these links sets up the on-board noise test to short the inputs to the on-board amplifiers, U8 and U9. In this mode, all inputs short to REFOUT.</td>
</tr>
<tr>
<td>LK8 to LK12</td>
<td>Inserted</td>
<td>Inserting these links sets up the on-board noise test, close to the ADC analog inputs. In this mode, all inputs short to REFOUT.</td>
</tr>
<tr>
<td>SL1</td>
<td>A</td>
<td>Sets the voltage applied to the AVDD2 pin. Operates using the AVDD1 supply (default). Position B sets the AVDD2 voltage to the 3.3 V supply from the ADP7118 (3.3 V) (U10) regulator.</td>
</tr>
<tr>
<td>SL2</td>
<td>A</td>
<td>Selects between an external (Position B) or on-board AVDD1 source (Position A). Supplies AVDD1 from the ADP7118 (3.3 V) (U7) (default).</td>
</tr>
<tr>
<td>SL3</td>
<td>A</td>
<td>Selects between an external (Position B) or on-board AVSS source (Position A). Supplies AVSS from the ADP7182 (−2.5 V) (U4) (default).</td>
</tr>
<tr>
<td>SL4</td>
<td>C</td>
<td>Connects AIN4 to: A4/J6 (Position A), REFOUT pin on the AD7172-2 (Position B), or AVSS (Position C). Position B and Position C are used to simplify the input using a single-ended input source.</td>
</tr>
<tr>
<td>SL5</td>
<td>B</td>
<td>Selects between an external or on-board IOVDD source. Supplies IOVDD from the ADP7118 (3.3 V) (U10) (default). The evaluation board operates with a 3.3 V logic.</td>
</tr>
<tr>
<td>SL8</td>
<td>A</td>
<td>Routes A0 to: AIN0 pin on the AD7172-2 (Position A), Buffer/In Amp U8 (Position B), Funnel Amp U9 with gain of 0.8x (Position C), or J10-1 (Position D).</td>
</tr>
<tr>
<td>SL9</td>
<td>A</td>
<td>Routes A2 to: AIN2 pin on the AD7172-2 (Position A), Buffer U12 (Position B), or Funnel Amp U9 with gain of 0.4x (Position C).</td>
</tr>
<tr>
<td>SL10</td>
<td>A</td>
<td>Routes A3 to: AIN3 pin on the AD7172-2 (Position A), Buffer U12 (Position B), or Funnel Amp U9 with gain of 0.4x (Position C).</td>
</tr>
<tr>
<td>SL11</td>
<td>A</td>
<td>Routes A1 to: AIN1 pin on the AD7172-2 (Position A), Buffer/In-amp U8 (Position B), Funnel Amp U9 with gain of 0.8x (Position C), or J10-7 (Position D).</td>
</tr>
<tr>
<td>G16</td>
<td>Inserted</td>
<td>Sets the on board in-amp (U8) to a gain of 16. Insert only one of the G16, G32, G64, or G128 links at a time.</td>
</tr>
<tr>
<td>G32</td>
<td>Not inserted</td>
<td>Sets the on-board in-amp (U8) to a gain of 32. Insert only one of the G16, G32, G64, or G128 links at a time.</td>
</tr>
<tr>
<td>G64</td>
<td>Not inserted</td>
<td>Sets the on-board in-amp (U8) to a gain of 64. Insert only one of the G16, G32, G64, or G128 links at a time.</td>
</tr>
<tr>
<td>G128</td>
<td>Not inserted</td>
<td>Sets the on-board in-amp (U8) to a gain of 128. Insert only one of the G16, G32, G64, or G128 links at a time.</td>
</tr>
<tr>
<td>R49 to R51</td>
<td>Inserted</td>
<td>Connects AVSS and AGND for single-supply operation. To operate in split supply mode, remove these links.</td>
</tr>
</tbody>
</table>
### SOCKETS AND CONNECTORS

**Table 2. Connector Details**

<table>
<thead>
<tr>
<th>Connector</th>
<th>Function</th>
<th>Connector Type</th>
<th>Manufacturer</th>
<th>Manufacturer Number</th>
<th>Stock Code(^1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Connector to the SDP-B</td>
<td>120-way connector, 0.6 mm pitch</td>
<td>Hirose</td>
<td>FXB-120S-SV(21)</td>
<td>FEC1324660</td>
</tr>
<tr>
<td>J2</td>
<td>External MCLK input</td>
<td>Straight PCB mount SMB/SMA jack</td>
<td>TE Connectivity</td>
<td>1-1337482-0</td>
<td>Not applicable</td>
</tr>
<tr>
<td>J3</td>
<td>External bench top voltage supply for the EVAL-AD7172-2SDZ</td>
<td>Power socket block, 3-pin, 3.81 mm pitch</td>
<td>Phoenix Contact</td>
<td>MC 1.5/3-G-3.81</td>
<td>FEC3704737</td>
</tr>
<tr>
<td>J5</td>
<td>External ac-to-dc adapter input for the EVAL-AD7172-2SDZ, 7 V to 9 V</td>
<td>DC power connectors, 2 mm SMT power jack</td>
<td>Lumberg</td>
<td>161314</td>
<td>FEC1243245</td>
</tr>
<tr>
<td>J6</td>
<td>Analog input terminal block; wired connection to external source or sensor</td>
<td>Power socket block, 8-pin, 3.81 mm pitch</td>
<td>Phoenix Contact</td>
<td>MC 1.5/8-G-3.81</td>
<td>FEC3704774</td>
</tr>
<tr>
<td>J9</td>
<td>External bench top voltage supply option for AVDD1/AVDD2, IOVDD, and AVSS inputs on the AD7172-2</td>
<td>Screw terminal block, 3.81 mm pitch</td>
<td>Phoenix Contact</td>
<td>1727036</td>
<td>FEC370-4592</td>
</tr>
<tr>
<td>J10</td>
<td>Optional header</td>
<td>7-way, 2.54 mm pin header</td>
<td>Samtec</td>
<td>SSW-107-01-T-S</td>
<td>FEC1803478</td>
</tr>
<tr>
<td>J13</td>
<td>Optional header</td>
<td>7-way, 2.54 mm socket header</td>
<td>Samtec</td>
<td>TLW-107-05-G-S</td>
<td>FEC1668499</td>
</tr>
<tr>
<td>A0 to A4</td>
<td>Analog inputs to ADC</td>
<td>Straight PCB mount SMB/SMA jack</td>
<td>TE Connectivity</td>
<td>1-1337482-0</td>
<td>Not applicable</td>
</tr>
<tr>
<td>A7</td>
<td>PMOD-compatible header</td>
<td>6-Pin, single in line (SIL) header(0.1 inch pitch)</td>
<td>Harwin</td>
<td>20-9990646</td>
<td>FEC1022255</td>
</tr>
</tbody>
</table>

\(^1\) Stock codes that begin with FEC are for Farnell Electronic Components.
SERIAL INTERFACE

The EVAL-AD7172-2SDZ evaluation board connects to the Blackfin® ADSP-BF527 on the SDP-B via the serial peripheral interface (SPI). The SPI has four primary signals: the CS, SCLK, and DIN input signals, and the OUT/RDY output signal.

To operate the evaluation board in standalone mode, disconnect the evaluation board from the SDP-B controller board. Use the test points to connect the signals to an alternative digital capture setup or the PMOD-compatible header (A7).

POWER SUPPLIES

Power the evaluation board from the ac-to-dc adapter connected to J5, or from an external bench top supply applied to J3 or J9. Linear LDOs generate the required voltages from the applied input voltage (Vin) rail when using J3 or J5. Use J9 to bypass the on-board regulators. An ADP7118 regulator generates the 5 V (single supply) and 2.5 V (split supply) supplies for the AVDD1 and AVDD2 rails to the ADC; a second ADP7118 generates 3.3 V for the IOVDD rail. The ADP7104 supplies +5 V for the SDP-B controller board, as well as +5 V for the ADM660 voltage converter to generate −5 V to supply the ADP7182. The ADP7182 generates the −2.5 V supply for AVSS when operating in split supply mode. Each supply is decoupled where it enters the board and at each device in accordance with the schematics shown in Figure 24 to Figure 28.

Table 3 shows the various power supply configurations available, including split supply operation.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Input Voltage Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Supply</td>
<td>7 V to 9 V</td>
<td>The 7 V to 9 V input is regulated to 5 V for AVDD1/AVDD2 and 3.3 V for IOVDD. This input also powers the external 5 V reference. See the Single Supply (Regulated) section in the Power Supply Configurations section.</td>
</tr>
<tr>
<td>(Regulated)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single Supply</td>
<td>7 V to 9 V, 5 V, and</td>
<td>The input is unregulated and connects directly to AVDD1/AVDD2 and IOVDD from J5. The 7 V to 9 V input powers the external 5 V reference. See the Single Supply (Unregulated) section in the Power Supply Configurations section.</td>
</tr>
<tr>
<td>(Unregulated)</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>Split Supply</td>
<td>7 V to 9 V</td>
<td>The 7 V to 9 V input is regulated to +2.5 V for AVDD1/AVDD2, −2.5 V for AVSS, and +3.3 V for IOVDD. The 7 V to 9 V input powers the external 5 V reference. See the Split Supply (Regulated) section in the Power Supply Configurations section.</td>
</tr>
<tr>
<td>(Regulated)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Split Supply</td>
<td>+7 V to +9 V, ±2.5 V, and +3.3 V</td>
<td>The input is unregulated and connects directly to AVDD1/AVDD2 and IOVDD from J5. The 7 V to 9 V input powers the external 5 V reference. See the Split Supply (Unregulated) section in the Power Supply Configurations section.</td>
</tr>
<tr>
<td>(Unregulated)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Only one configuration can be used at a time.
POWER SUPPLY CONFIGURATIONS

Single Supply (Regulated)

There are two available power supply options for the single-supply (regulated) configuration.

- An ac-to-dc adapter (included) connected to J5. Set LK2 to Position B.
- A bench top power supply connected to J3. Set LK2 to Position A, and ensure that AVSS = AGND = 0 V.

Set all other links and solder links to the default settings, as outlined in Table 1.

Single Supply (Unregulated)

To set up the evaluation board, use the following procedure:

1. Move SL2 to Position B and SL5 to Position A.
2. Connect the two terminals of J9 labeled AGND and AVSS.
3. Connect 0 V (GND) to J9 at the terminal labeled AGND.
4. Connect 5 V to J9 at the terminal labeled AVDD.
5. Connect 3.3 V to J9 at the terminal labeled IOVDD.
6. Connect the 7 V to 9 V input to J5.

Set all other links and solder links to the default settings, as outlined in Table 1.

Split Supply (Regulated)

To set up the EVAL-AD7172-2SDZ evaluation board, use the following procedure:

1. Move SL2, SL3 to Position B and SL5 to Position A.
2. Remove R49 to R51.
3. Insert a 0 Ω resistor at R67 and R85.
4. Connect 0 V (GND) to J9 at the terminal labeled AGND.
5. Connect 2.5 V to J9 at the terminal labeled AVDD.
6. Connect −2.5 V to J9 at the terminal labeled AVSS.
7. Connect 3.3 V to J9 at the terminal labeled IOVDD.
8. Connect 7 V to 9 V to J5.
9. Set LK1 to Position B. This sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.

Set all other links and solder links set to the default settings, as outlined in Table 1.

ANALOG INPUTS

The primary analog inputs of the EVAL-AD7172-2SDZ evaluation board can be applied in two separate ways.

- J6 connector on the left side of the board
- A0 to A4 SMB/SMA footprints on the evaluation board

The analog inputs route directly to the associated analog input pins on the AD7172-2, provided that the LK8 to LK12 links (on-board noise test) are removed. The AD717x Eval+ software is set up to analyze dc inputs to the ADC. The AD7172-2 input buffers work for dc input signals.

REFERENCE OPTIONS

The EVAL-AD7172-2SDZ evaluation board includes an external 5 V reference, the ADR445. The AD7172-2 includes an internal 2.5 V reference. The default operation is to use the external reference input, which is set to accept the 5 V ADR445 on the evaluation board.
EVALUATION BOARD SOFTWARE INSTALLATION

Install the AD717x Eval+ software before connecting the evaluation board and the SDP-B board to the USB port of the PC to ensure that the evaluation system is properly recognized when connected to the PC.

There are two parts to the installation, noted by the following:
1. AD717x Eval+ software installation
2. AD717x Eval+ Dependencies installation
   a. SDP-B board drivers
   b. Ssrc SVG plug-in
   c. Microsoft .NET Framework 3.5

INSTALLING THE AD717x Eval+ SOFTWARE

To install the AD717x Eval+ software, take the following steps:
1. Ensure that the SDP-B board is disconnected from the USB port of the PC and insert the CD into the CD-ROM drive.
2. Double click the setup.exe file to begin the evaluation board software installation. The default installation location for the software is C:\Program Files\Analog Devices\AD717x Eval+.
3. A dialogue box appears asking for permission to allow the program to make changes to the PC (See Figure 3). Click Yes.
4. Select a location to install the software and click Next>>. Figure 4 shows the default locations displayed when the dialogue box opens. To select another location click Browse.
5. A license agreement appears. Read the agreement, select I accept the License Agreement, and click Next>> (see Figure 5).
6. A summary of the installation displays. Click Next>> to continue (see Figure 6).

Figure 6. Reviewing a Summary of the Installation

7. The message shown in Figure 7 appears when the installation is complete.

Figure 7. Installation Complete Window

INSTALLING THE EVAL+ DEPENDENCIES
After the installation of the evaluation software is complete, a welcome window displays to install the Eval+ Dependencies.

1. Ensure that the SDP-B board is still disconnected from the USB port of the PC and that all other applications are closed, and then click Install (see Figure 8).

Figure 8. Beginning the Drivers Installation

2. The Src SVG plug-in installs first, then the SDP drivers, and finally, the .NET Framework 3.5.

3. If using Windows 8 or Windows 10, see the Installing .NET Framework 3.5 for Windows 8/Windows 10 section.

4. To complete the SDP-B drivers installation and close the installation setup wizard, click Close (see Figure 9).

Figure 9. Completing the Drivers Setup Wizard
5. Before using the evaluation board, restart the PC (see Figure 10).

![Figure 10. Restarting the PC](image)

**Installing .NET Framework 3.5 for Windows 8/Windows 10**

Windows 8 and Windows 10 have a built-in installer for the .NET Framework 3.5. To run this installer, an internet connection is required, and administrator privileges can be required. Contact a system administrator if the following steps do not work.

1. When the Eval+ Dependencies installer reaches the .NET Framework 3.5 installation step, a window appears, as shown in Figure 11.

![Figure 11. Windows 8/Windows 10 .NET Framework 3.5 Installation](image)

2. Follow the steps shown in the installation wizard to complete the installation.

3. If the window shown in Figure 11 does not appear, the .NET Framework 3.5 may already be installed on the PC. To confirm that the software is installed, open the **Control Panel > Programs > Programs and Features**, and then select **Turn Windows features on or off**. In the pop-up window, find .NET Framework 3.5 and confirm that the software is enabled.

**SETTING UP THE SYSTEM FOR DATA CAPTURE**

After completing the steps in the Installing the AD717x Eval+ Software section and the Installing the Eval+ Dependencies section, take the following steps to set up the system for data capture:

1. Connect the SDP-B board to the PC and allow the Found New Hardware Wizard to run. If using Windows XP, search for the SDP-B drivers and choose to automatically search for the drivers if prompted by the operating system.

2. Use the **Device Manager** to confirm that the board is properly connecting to the PC.

3. Access the **Device Manager** by completing the following steps:
   a. From the **Start** menu, right-click **My Computer** and then click **Manage**.
   b. A dialog box appears asking for permission to allow the program to make changes to the PC. Click **Yes**.
   c. The **Computer Management** window appears. Click **Device Manager** from the list of **System Tools** (see Figure 12).
   d. The SDP-B board appears under **ADI Development Tools**, indicating that the driver software has installed and the board is connecting to the PC properly.

![Figure 12. Device Manager](image)
LAUNCHING THE SOFTWARE

After completing the steps in the Setting Up the System for Data Capture section, take the following steps to launch the AD717x Eval+ software:

1. From the Start menu, click Programs > Analog Devices > AD717x EVAL+ > AD717x Eval+.

2. The dialogue box in Figure 13 appears; select AD7172-2 Evaluation Board and click the Select button. The main window of the software box displays as shown in Figure 16.

3. If the EVAL-AD7172-2SDZ evaluation system is not connected to the USB port via the SDP-B board when the software is launched, the software displays the dialog box shown in Figure 14. Connect the evaluation board to the USB port of the PC; wait a few seconds, click Refresh, and the option shown in Figure 13 appears.

4. The AD717x Eval+ software can also be used without connecting hardware. Click the Simulation button and the options shown in Figure 15 appear. This option uses a software model and allows the AD7172-2, AD7172-4, AD7173-8, AD7175-2, AD7175-8, AD7176-2, or AD7177-2 to be evaluated.
EVALUATION BOARD SOFTWARE OPERATION

OVERVIEW OF THE MAIN WINDOW
The main window of the AD717x Eval+ software displays the significant control buttons and analysis indicators of the AD717x Eval+ software. This window is divided into five tabs: Configuration, Waveform, Histogram, Modelled Performance, and Registers.

CONFIGURATION TAB
Figure 16 shows the Configuration (1) tab when Hardware mode is selected and Figure 17 shows the Configuration tab when Simulation mode is selected. The controls highlighted in Figure 17 are only available in Simulation mode.

Select Product/Evaluation Mode Pane
The Evaluation Mode (2) pane displays the evaluation mode in use. To switch between modes, click the Select Product… button, and the dialog box shown in Figure 13 appears.

Tutorial Icon
Click the tutorial icon (3) to open a tutorial and view additional information on using the AD717x Eval+ software.

Functional Block Diagram and Configuration Pop-Up Buttons
The functional block diagram (4) of the ADC shows each of the separate functional blocks within the ADC. Click a configuration button (5) on any of the functional blocks to open the configuration pop-up window for the block selected. Not all blocks have a configuration button.

Analog and Digital Supply Voltage
The text fields labeled 6, 7, and 14 in Figure 16 and Figure 17 are input fields that are used to take the supply voltage levels selected for the AD7172-2. Checks are performed to ensure that the power supply voltage levels entered are within the specified limits. These power supply voltage levels are also used for the modelled performance to calculate the power dissipation.

External Reference
The Ext. REF-(V) and Ext. REF+(V) (8) text fields set the positive and negative external reference voltage values. The difference of these fields is used to calculate the results for both the Waveform and Histogram tabs. The evaluation board has an external 5 V ADR445 reference, which can be bypassed by removing R32. Change the external reference voltage value in the external reference text fields to ensure the correct calculation of results in the Waveform and Histogram tabs.

Register Configuration Summary
Click the Summary (9) button to display the selected configuration of the AD7172-2, which includes channel configuration, information on each of the individual setups, as well as information on any error present.
Reset ADC

Click the Reset ADC (10) button to perform a software reset of the AD7172-2. The AD7172-2 does not have a hardware reset pin. To perform a hard reset, the power must be removed from the board. The software reset has the same effect as a hard reset.

Menu Bar

The menu bar (11) has three sections: File, Edit, and Help.

File

Three options are available in the File menu: Save, Load, and Exit.

The Save option allows the user to save register configurations or waveform data. Register configurations can be saved as a JavaScript Object Notation (JSON) file or a header file. If the configuration is only used in the AD717x Eval+ software environment, it is recommended to use the JSON file setting. Waveforms are saved as .csv files and the user is prompted to save the register configuration.

The Load option allows the user to load saved register configurations or waveform data. To load a header file into the AD717x Eval+ software, the file must be in the same format as the file that is saved from the AD717x Eval+ software. The header file can be used when developing firmware. When loading the waveform data, the user is prompted to load the register configuration. This step is so the software can correctly analyze the data.

Click Exit to close the AD717x Eval+ software.

Edit

There are two options available in the Edit dropdown menu: Change Product Selection and Reset ADC. The Change

Product Selection option performs the same action as the Select Product button and Reset ADC performs the same action as the Reset ADC button.

Help

The Help dropdown menu provides links to extra information about the AD7172-2, which includes links to the product page, the evaluation board user guide, the datasheet, and the No-OS Drivers.

Selecting the AD717x Eval+ Tutorial

To open this tutorial, click the tutorial icon (3). For details on the version of the software, the About option opens a dialog box displaying the current version of the software and the relevant licenses.

Status Bar

The status bar (12) displays the busy indicator and status updates, such as Analysis Completed and Reset Completed during software use.

Device Error

The Device Error (13) LED icon illuminates when a when an ADC error is detected or when a cyclic redundancy check (CRC) error occurs. The CRC functionality on the AD7172-2 is disabled by default and must be enabled for this indicator to work. More information on the CRC error can be found in the Register Configuration Summary section.
External MCLK Frequency
The Ext. MCLK(Hz) text field (15) sets the external MCLK frequency. The Ext. MCLK(Hz) control is only visible in the Configuration tab when an external clock source is selected by the ADC. The value entered in this field is used by the functional model shown in the Modelled Performance tab.

Analog Input Voltage
The input fields shown in the Simulated Input pane (16) are only available when the AD717x Eval+ software is executed in simulation mode. These simulated inputs allow the analog input voltages to be set and can be changed at any time when the device is in simulation mode.

External SCLK Frequency
The SCLK(Hz) text field (17) sets the external SCLK frequency for the SPI interface. This text field is only available in simulation mode to determine if the SCLK frequency is within the permitted range.
Figure 18. Waveform Tab of the AD717x Eval+ Software

WAVEFORM TAB

Figure 18 shows the Waveform tab (18) of the AD717x Eval+ Software.

**Sampling Mode**

The Sampling Mode control (19) is unrelated to the ADC mode. This control can be set to capture a defined sample set (single capture), or continuously gather batches of samples (repeated capture). The user can also select data logging, which runs in a similar manner to the repeated capture option; however, selecting data logging posts the results to a .csv file. When saving the results, the .csv file prompts the user to save the register configuration, which is necessary to load the analysis of the data back into the software.

**Samples**

The Samples text field (20) sets the number of samples gathered per batch. The Single Capture option selected from the Sampling Mode dropdown list returns the number of samples entered in the Samples text field. The Repeated Capture option continues to return batches of the number entered in the Samples text field until sampling is stopped by the user.

**Sample**

Click the Sample button (21) to start gathering ADC results. Results appear in the waveform graph (22).

**Waveform Graph and Controls**

The waveform graph (22) shows each successive sample of the ADC output. Zoom in on the data using the control toolbar (23). Click the x-axis and y-axis to change the scales on the graph.

**Channel Selection**

The channel selection control (24) allows the user to choose which channels display on the data waveform graph. These controls only affect the display of the channels and do not have any effect on the channel settings in the ADC register map.

**Noise Analysis Pane**

The Noise Analysis pane (25) displays the results of the noise analysis for the selected analysis channel; this includes noise and resolution measurements.

**Analysis Channel**

The noise analysis dropdown list (26) and histogram graph show the analysis of the channel selected.


**Display Units and Axis Controls**

In the *Graph Configuration* pane (27), select the *Units: V/mV/μV/nV* dropdown menu to select the unit that the data displays in the graph. This control affects the waveform graph (22) and the histogram graph (see Figure 19). The axes controls can be switched between dynamic and fixed. When dynamic control is selected, the axes automatically adjust to show the entire range of the ADC results after each batch of samples. When fixed control is selected, the user can program the ranges of the axes. These ranges do not automatically adjust after each batch of samples.
HISTOGRAM TAB
Figure 19 shows the Histogram tab (28) of the AD717x Eval+ software.

Histogram Graph and Controls
The histogram graph (29) shows the number of times each sample of the ADC output occurs. The control toolbar (30) in the histogram graph allows you to zoom in on the data (see Figure 19). Click the x-axis and y-axis to change the scales on the graph.

Figure 19. Histogram Tab of the AD7172-2 Evaluation Software
MODELLED PERFORMANCE TAB

The **Modelled Performance** tab (31) shows a number of ADC performance parameters, which are calculated using the ADC functional model.

There are three main options in the **Modelled Performance** tab: **Filter Profile**, **Filter Step Response**, and **Timing Diagram/Power**. These options can be selected from the dropdown list (33). Figure 20 shows this tab when **Filter Profile** is selected.

**Modelled Performance Analysis Channel**

The analysis channel dropdown list (32) selects the channel to be evaluated by the functional model.

**Filter Profile Graph**

This graph (34) shows the frequency response for the selected digital filter. The graph controls allows the user to zoom in on the data. Click the x-axis and y-axis to change the scales on the graph.

**Filter Rejection**

The **Filter Rejection** pane (35) shows the rejection/attenuation of the digital filter over the rejection bandwidth for $f_1$ and $f_2$ in decibels. The $f_1$, $f_2$, and **Bandwidth** values can be changed.

**Filter Performance**

The **Filter Performance** pane (36) shows timing information for the data rate of the selected output. This pane shows the ADC initial settling time ($T_{settle}$), the first frequency notch ($F_{notch}$), and the actual sampling frequency ($f_{ADC}$).
**Filter Step Response**

The Filter Step Response dropdown list (37) allows the user to switch between the three sections of the Modelled Performance tab. Figure 21 shows this tab when Filter Step Response is selected from the dropdown list.

**Step Response Graph**

This graph (38) shows how long the filter takes to settle when the voltage is stepped from one voltage to the next. For this analysis, it is assumed the ADC is continuously converting on only one channel.

**Step Configuration**

The controls in the Step Configuration pane (39) allow the user to set the voltage before and after the step, as well as the step position. The Step Position text field is set as a percentage where 0% is 1/fADC and 100% is 2/fADC.

**Step Response**

The controls in the Step Response pane (40) provide timing information for the data rate of the selected output. This pane shows the actual sampling frequency (fADC), the ADC initial settling time (Tsettle), and the settling time between conversions (1/fADC).

**Graph Units**

Use the controls in the Graph Units pane (41) to switch the step response between Percentage, Volts, and Codes.
**Timing Diagram/Power**

This dropdown list (42) allows the user to switch between the three sections of the Modelled Performance tab. Figure 22 shows the tab when Timing Diagram/Power is selected from the dropdown list.

**Estimated Power Consumption**

The Estimated Power Consumption pane (43) shows the total power consumption of the device in the selected configuration, as well as the current consumption on each of the power supply rails. Note that the estimated power consumption is for continuous conversion mode only. No other mode of operation is supported by this control.

**Timing Diagram**

The graph shown in the Timing Diagram pane (44) shows the digital interface timing diagram for the current configuration. The graph shows the timing for the configuration of the ADC and the subsequent data reads from the ADC.
Figure 23. **Registers** Tab of the AD717x Eval+ Software

**REGISTERS TAB**

Figure 23 shows the **Registers** tab (45).

**Register Tree**

This register list control (46) shows the full register map in a tree control format. Each register is shown; click the expand button next to each register to show all of the bit fields contained within that register.

**Register**

The **Register** pane (47) allows the user to change the individual bit of the register selected in the register tree by clicking the bits or by entering the register value directly into the text field on the right side of the pane.

**Bitfields**

The **Bitfields** pane (48) shows the bit fields of the register selected in the register tree. Change the values in this pane by using the **Setting** dropdown lists or by directly entering a value into the **value** text fields.

**Documentation**

The **Documentation** pane (49) contains the documentation for the register or bit field selected in the register tree.

**Save and Load**

The **Save** (50) and **Load** (51) buttons allow the user to save the current configuration of the AD7172-2 by saving the register map settings to a file and loading the settings from the same file. When using these buttons, the register configurations are saved and loaded as JSON files.

**EXITING THE SOFTWARE**

To exit the software, click the close button at the top right corner of the AD717x Eval+ software.
Figure 24. AD7172-2 Schematic
Figure 25. Amplifier Schematic
Figure 26. Power Supply Sequencing Schematic
Figure 27. Regulator Schematic
Figure 28. SDP-B Connector Schematic
Figure 30. Bottom PCB Silkscreen

Figure 31. Layer 1, Component Side
Figure 32. Layer 2, Ground Plane

Figure 33. Layer 3, Power/Ground Plane
Figure 34. Layer 4, Solder Side
# ORDERING INFORMATION

## BILL OF MATERIALS

Table 4.

<table>
<thead>
<tr>
<th>Qty.</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Stock Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>A0 to A6</td>
<td>Straight PCB mount SMB jack, keep hole clear of solder, do not insert</td>
<td>TE Connectivity</td>
<td>1-1337482-0</td>
<td>Do not insert</td>
</tr>
<tr>
<td>1</td>
<td>A7</td>
<td>6-pin SIL header, 0.1 inch pitch</td>
<td>Harwin</td>
<td>20-9990646</td>
<td>FEC 1022255</td>
</tr>
<tr>
<td>2</td>
<td>C1, C17</td>
<td>Ceramic capacitor, 6.3 V, X5R, 0603, 4.7 μF</td>
<td>Murata</td>
<td>GRM188R60J475K</td>
<td>FEC 173-5527</td>
</tr>
<tr>
<td>2</td>
<td>C2, C38</td>
<td>Ceramic capacitor, 50 V, X7R, 0603, 0.1 μF</td>
<td>Murata</td>
<td>GRM188R71H104K</td>
<td>FEC 882-0023</td>
</tr>
<tr>
<td>1</td>
<td>C3</td>
<td>Ceramic capacitor, 10 V, X5R, 0603, 0.1 μF</td>
<td>KEMET</td>
<td>C0603C475K8PACTU</td>
<td>FEC 157-2625</td>
</tr>
<tr>
<td>2</td>
<td>C4, C6</td>
<td>Capacitor, 0805, 50 V, X7R, 1 μF</td>
<td>Murata</td>
<td>GRM21BR71H105KA12L</td>
<td>FEC 1735541</td>
</tr>
<tr>
<td>22</td>
<td>C5, C7, C9, C16, C24, C25, C29, C41, C42, C61 to C63, C65, C66, C69, C70, C78 to C82</td>
<td>Ceramic capacitor, 0402, do not insert</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>C10, C11</td>
<td>Ceramic capacitor, crystal, 0402, do not insert</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>C12 to C14, C18, C20 to C22, C33, C34, C37, C40, C44, C52 to C54, C58, C60, C72, C73, C75, C87, C89, C91</td>
<td>Capacitor, 16 V, X7R, 0402</td>
<td>Murata</td>
<td>GRM155R71C104K</td>
<td>FEC 881-9742</td>
</tr>
<tr>
<td>5</td>
<td>C15, C30, C56, C57, C76</td>
<td>Capacitor, 6.3 V, 0603, 1 μF</td>
<td>Murata</td>
<td>GRM188R70J105KA01D</td>
<td>FEC 184-5765</td>
</tr>
<tr>
<td>8</td>
<td>C19, C27, C28, C55, C59, C83, C85, C86</td>
<td>Ceramic capacitor, 50 V, C0G/NPO, 0603</td>
<td>AVX Corporation</td>
<td>06035A271JAT2A</td>
<td>FEC 1734627</td>
</tr>
<tr>
<td>4</td>
<td>C23, C26, C84, C88</td>
<td>Ceramic capacitor, 50 V, X7R, 0402, do not insert</td>
<td>KEMET</td>
<td>C0603C681J5GACTU</td>
<td>FEC 1414648</td>
</tr>
<tr>
<td>3</td>
<td>C31, C50, C51</td>
<td>Ceramic capacitor, 16 V, X7R, 0402, do not insert</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>C32, C35, C36, C39, C48, C49, C64, C67</td>
<td>Capacitor, MLCC (multilayer ceramic capacitor) 10 V, X5R, 10 μF, 0603</td>
<td>TDK Corporation</td>
<td>C1608X5R1A106K080AC</td>
<td>FEC 221-1164</td>
</tr>
<tr>
<td>6</td>
<td>C43, C45 to C47, C71, C77</td>
<td>Capacitor, MLCC, 10 V, X5R, 2.2 μF, 0603</td>
<td>Newark</td>
<td>MC0603X225K100CT</td>
<td>FEC 232-0817</td>
</tr>
<tr>
<td>4</td>
<td>C68, C74, C90, C92</td>
<td>Capacitor, MLCC, 50 V, X7R</td>
<td>Yageo</td>
<td>2238 586 15623</td>
<td>FEC 722170</td>
</tr>
<tr>
<td>3</td>
<td>D2, D6, D16</td>
<td>LED, red, high intensity (&gt;90 mcd), 0603</td>
<td>Broadcom Limited</td>
<td>HSMC-C191</td>
<td>FEC 855-4528</td>
</tr>
<tr>
<td>1</td>
<td>D4</td>
<td>LED, green, SMD</td>
<td>Osram</td>
<td>LGQ971</td>
<td>FEC 1226372</td>
</tr>
<tr>
<td>1</td>
<td>D5</td>
<td>Zener diode, 0.5 W, 5.1 V</td>
<td>Vishay</td>
<td>BZT52BSV1-V-GS08</td>
<td>FEC 1617767</td>
</tr>
<tr>
<td>1</td>
<td>G16</td>
<td>2-pin header and shorting shunt, 2 mm pitch</td>
<td>Harwin</td>
<td>M22-2010205 and M22-1920005</td>
<td>FEC 671915 and 510944</td>
</tr>
<tr>
<td>3</td>
<td>G32, G64, G128</td>
<td>2-pin header, 2 mm pitch</td>
<td>Harwin</td>
<td>M22-2010205</td>
<td>FEC 671915</td>
</tr>
<tr>
<td>19</td>
<td>GND, GND1 to GND6, GPIO0, GPIO1, REF-, REF+, TDIN, TDOUT, TERR, TCLK, TSYNC, TXTAL1, TXTAL2, TCS</td>
<td>Test point, keep hole clear of solder, do not insert</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J1</td>
<td>120-way connector, 0.6 mm pitch</td>
<td>Hirose Electric Group</td>
<td>FX8-1205-SV(21)</td>
<td>FEC 1324660</td>
</tr>
<tr>
<td>Qty.</td>
<td>Reference Designator</td>
<td>Description</td>
<td>Manufacturer</td>
<td>Part Number</td>
<td>Stock Code</td>
</tr>
<tr>
<td>------</td>
<td>----------------------</td>
<td>------------------------------------------------------------------------------</td>
<td>-------------------</td>
<td>-------------------</td>
<td>--------------</td>
</tr>
<tr>
<td>1</td>
<td>J2</td>
<td>Straight PCB mount, SMB jack, keep hole clear of solder, do not insert</td>
<td>TE Connectivity</td>
<td>1-1337482-0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J3</td>
<td>Socket terminal block, 3.81 mm pitch</td>
<td>Phoenix Contact</td>
<td>MC 1.5/3-G-3.81</td>
<td>FEC 370-4737</td>
</tr>
<tr>
<td>1</td>
<td>J4</td>
<td>Screw terminal block, 3.81 mm pitch, do not insert</td>
<td>Phoenix Contact</td>
<td>1727023</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J5</td>
<td>DC power connectors, 2 mm pitch, SMT power jack</td>
<td>Lumberg</td>
<td>161314</td>
<td>FEC 1243245</td>
</tr>
<tr>
<td>1</td>
<td>J6</td>
<td>8-pin terminal header, 3.81 mm pitch, vertical</td>
<td>Phoenix Contact</td>
<td>MC 1.5/8-G-3.81</td>
<td>FEC 3704774</td>
</tr>
<tr>
<td>1</td>
<td>J7</td>
<td>Connector, 3.81 mm pitch, right angle, do not insert</td>
<td>Phoenix Contact</td>
<td>MC 1.5/4-G-3.81 and 180-3594</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J8</td>
<td>8-pin screw terminal, 3.81 mm pitch, vertical, do not insert</td>
<td>Phoenix Contact</td>
<td>1727078</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J9</td>
<td>Screw terminal block, 3.81 mm pitch</td>
<td>Phoenix Contact</td>
<td>1727036</td>
<td>FEC 370-4592</td>
</tr>
<tr>
<td>1</td>
<td>J10</td>
<td>7-way SSW, 2.54 mm vertical socket, line up with connector on surf board</td>
<td>Samtec</td>
<td>SSW-107-01-T-S</td>
<td>FEC 1803478</td>
</tr>
<tr>
<td>2</td>
<td>J11, J14</td>
<td>Screw terminal block, 3.81 mm pitch, do not insert</td>
<td>Phoenix Contact</td>
<td>MKDS1/4-3.81</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J12</td>
<td>4-way power socket block, 3.81 mm pitch</td>
<td>Phoenix Contact</td>
<td>MC1.5/4-G-3.81</td>
<td>FEC 370-4749 and FEC 370-4920</td>
</tr>
<tr>
<td>1</td>
<td>J13</td>
<td>7-way SIP, 2.54 mm through-hole header, line up with connector on surf board</td>
<td>Samtec</td>
<td>TLW-107-05-G-S</td>
<td>FEC 1668499</td>
</tr>
<tr>
<td>1</td>
<td>J15</td>
<td>4-way power socket block, 3.81 mm pitch</td>
<td>Phoenix Contact</td>
<td>MC1.5/4-G-3.81</td>
<td>FEC 370-4749 and FEC 370-4920</td>
</tr>
<tr>
<td>4</td>
<td>L1 to L4</td>
<td>Ferrite bead, 0.3 Ω at dc, 1000 Ω at 100 MHz, 350 mA, 0805</td>
<td>TE Connectivity</td>
<td>BMB2A1000LN2</td>
<td>FEC 119-3421</td>
</tr>
<tr>
<td>2</td>
<td>LK1, LK2</td>
<td>3-pin (3 × 1) header and shorting block in, 0.1 inch pitch, Position A</td>
<td>Harwin</td>
<td>M20-9990346 and M7566-05</td>
<td>FEC 1022249 and 150-411</td>
</tr>
<tr>
<td>5</td>
<td>LK3 to LK7</td>
<td>2-pin header, 0.1 inch pitch</td>
<td>Harwin</td>
<td>M20-9990246</td>
<td>FEC 1022247</td>
</tr>
<tr>
<td>5</td>
<td>LK8 to LK12</td>
<td>2-pin header and shorting shunt, 0.1 inch pitch</td>
<td>Harwin</td>
<td>M20-9990246</td>
<td>FEC 1022247 and 150-411</td>
</tr>
<tr>
<td>1</td>
<td>Q1</td>
<td>Diode, MOSFET, negative channel, 30 V, 3.6 A, SOT-23</td>
<td>Vishay</td>
<td>SI2304DDS-T1-GE3</td>
<td>FEC 1858939</td>
</tr>
<tr>
<td>1</td>
<td>Q2</td>
<td>Transistor, NPN, SOT-23</td>
<td>ON Semiconductor</td>
<td>MMBT3904LT1G</td>
<td>FEC 1459100</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>Resistor, 0603, do not insert</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>R2 to R4, R7, R48, R66, R75</td>
<td>Resistor, 100 kΩ, 0.063 W, 1%, 0603</td>
<td>Newark</td>
<td>MC0063W06031100K</td>
<td>FEC 9330402</td>
</tr>
<tr>
<td>3</td>
<td>R5, R6, R77</td>
<td>Resistor, 10 kΩ, 0.063 W, 1%, 0402</td>
<td>Newark</td>
<td>MC00625W0402110K</td>
<td>FEC 1358069</td>
</tr>
<tr>
<td>2</td>
<td>R8, R71</td>
<td>Resistor, 1%, 0402</td>
<td>Yageo</td>
<td>CRCW040210K0FKEAHP</td>
<td>FEC 173-8864</td>
</tr>
<tr>
<td>31</td>
<td>R9 to R13, R27, R30, R32, R41, R63, R78, R81 to R84, R87, R95, R99, R101, R103, R105, R107, R111, R114, R117, R121, R124, R128 to R131</td>
<td>Resistor, 0603 1%, 0R</td>
<td>Newark</td>
<td>MC0063W060303R</td>
<td>FEC 9331662</td>
</tr>
<tr>
<td>1</td>
<td>R14</td>
<td>Resistor, 0402, 1%, 39 kΩ</td>
<td>Newark</td>
<td>MC00625W0402139K</td>
<td>FEC 1358085</td>
</tr>
<tr>
<td>4</td>
<td>R15, R17, R18, R24</td>
<td>Resistor, SMD</td>
<td>Newark</td>
<td>MC 0.0625W 0402 1% 10K2</td>
<td>FEC 1803137</td>
</tr>
<tr>
<td>1</td>
<td>R16</td>
<td>Resistor, 0402, 1%, 69K8</td>
<td>Newark</td>
<td>MC 0.0625W 0402 1% 69K8</td>
<td>FEC 1803735</td>
</tr>
<tr>
<td>Qty.</td>
<td>Reference Designator</td>
<td>Description</td>
<td>Manufacturer</td>
<td>Part Number</td>
<td>Stock Code</td>
</tr>
<tr>
<td>------</td>
<td>----------------------</td>
<td>-------------</td>
<td>--------------</td>
<td>-------------</td>
<td>------------</td>
</tr>
<tr>
<td>15</td>
<td>R19 to R22, R35 to R38, R40, R58, R59, R61, R62, R70, R116</td>
<td>Resistor, 0402</td>
<td>Vishay</td>
<td>CRCW04020000Z0ED</td>
<td>FEC 146-9661</td>
</tr>
<tr>
<td>1</td>
<td>R23</td>
<td>Resistor, 0402, 1%, 86K6</td>
<td>Newark</td>
<td>MC 0.0625W 0402 1% 86K6</td>
<td>FEC 1803744</td>
</tr>
<tr>
<td>2</td>
<td>R25, R57</td>
<td>Resistor, 0402, 1%, 30k1</td>
<td>Newark</td>
<td>MC 0.0625W 0402 1% 30k1</td>
<td>FEC 1803699</td>
</tr>
<tr>
<td>32</td>
<td>R26, R28, R29, R31, R33, R56, R64, R67, R72, R74, R76, R80, R85, R86, R88, R98, R100, R102, R108 to R110, R112, R113, R115, R118 to R120, R122, R123, R125, R126, R132</td>
<td>Resistor, SMD, 0603, do not insert</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>R34, R39, R46, R47</td>
<td>Resistor, 10 kΩ, 0.063 W, 1%, 0603</td>
<td>Newark</td>
<td>MC0063W0603110R</td>
<td>FEC 9330429</td>
</tr>
<tr>
<td>4</td>
<td>R42 to R45</td>
<td>Resistor, thick film, 10 kΩ, 62.5 mW, 5%</td>
<td>Yageo</td>
<td>RC0402JR-1310KL</td>
<td>FEC 179-9316</td>
</tr>
<tr>
<td>4</td>
<td>R49 to R52</td>
<td>Resistor, 1206</td>
<td>Newark</td>
<td>MC 0.125W 1206 0R</td>
<td>FEC 9336974</td>
</tr>
<tr>
<td>2</td>
<td>R53, R65</td>
<td>Resistor, 10 kΩ, 0.063 W, 1%, 0603</td>
<td>Newark</td>
<td>MC0063W0603110K</td>
<td>FEC 9330399</td>
</tr>
<tr>
<td>1</td>
<td>R54</td>
<td>Resistor, thick film, 4.53 kΩ, 63 mW, 1%</td>
<td>Vishay</td>
<td>CRCW04024K53FKED</td>
<td>FEC 1151244</td>
</tr>
<tr>
<td>1</td>
<td>R55</td>
<td>Resistor, 0402, 1%, 61R9</td>
<td>Newark</td>
<td>MC 0.0625W 0402 1% 61R9</td>
<td>FEC 1802915</td>
</tr>
<tr>
<td>1</td>
<td>R60</td>
<td>Resistor, thick film, 2.4 kΩ, 0603, 100 mW, 1%</td>
<td>Yageo</td>
<td>RC0603FR-072K4L</td>
<td>FEC 1799329</td>
</tr>
<tr>
<td>1</td>
<td>R68</td>
<td>Resistor, 0603, 4K75, 0.1%, 0.1 W</td>
<td>Panasonic</td>
<td>ERA3AR84751V</td>
<td>FEC 209-4611</td>
</tr>
<tr>
<td>2</td>
<td>R69, R104</td>
<td>Resistor, 0603, 0.1%, 0.1 W, 75 kΩ</td>
<td>Panasonic</td>
<td>ERA3AR8753P</td>
<td>FEC 171-7620</td>
</tr>
<tr>
<td>1</td>
<td>R73</td>
<td>Resistor, 88R7, 0.063 W, 0.1%, 0402</td>
<td>TE Connectivity</td>
<td>RN73C1E88R7B</td>
<td>FEC 173-7900</td>
</tr>
<tr>
<td>1</td>
<td>R79</td>
<td>Resistor, 121 kΩ, 0.063 W, 0.1%, 0603</td>
<td>TE Connectivity</td>
<td>RN73C1J121RBTG</td>
<td>FEC 114-0465</td>
</tr>
<tr>
<td>1</td>
<td>R90</td>
<td>Resistor, 0402, do not insert</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>R91</td>
<td>Resistor, 2K26, 0.063 W, 0.1%, 0402</td>
<td>TE Connectivity</td>
<td>RN73C1E2K26B</td>
<td>FEC 173-8050</td>
</tr>
<tr>
<td>1</td>
<td>R92</td>
<td>Resistor, 51R1, 0.063 W, 0.1%, 0603</td>
<td>TE Connectivity</td>
<td>RN73C1J51R1BTG</td>
<td>FEC 114-0446</td>
</tr>
<tr>
<td>2</td>
<td>R93, R106</td>
<td>Resistor, 0603</td>
<td>Vishay</td>
<td>CRCW06030000Z0EA</td>
<td>FEC 146-9739</td>
</tr>
<tr>
<td>1</td>
<td>R94</td>
<td>Resistor, 0603, 1K13, 0.1%, 0.1 W</td>
<td>Panasonic</td>
<td>ERA3AR81131V</td>
<td>FEC 209-4485</td>
</tr>
<tr>
<td>1</td>
<td>R96</td>
<td>Resistor, 1K07, 0.063 W, 1%, 0603</td>
<td>Newark</td>
<td>MC0063W0603110K7</td>
<td>FEC 1170792</td>
</tr>
<tr>
<td>1</td>
<td>R97</td>
<td>Resistor, 1K02, 0.063 W, 1%, 0603</td>
<td>Newark</td>
<td>MC0063W060311K02</td>
<td>FEC 1170789</td>
</tr>
<tr>
<td>1</td>
<td>R127</td>
<td>Resistor, 0603</td>
<td>Vishay</td>
<td>CRCW06030000Z0EA</td>
<td>FEC 146-9739</td>
</tr>
<tr>
<td>1</td>
<td>SL1</td>
<td>2-way resistor link option</td>
<td>Newark</td>
<td>MC 0.063W 0603 0R</td>
<td>FEC 9331662</td>
</tr>
<tr>
<td>2</td>
<td>SL2, SL3</td>
<td>2-way solder link, use OR 0603 resistor, insert link in Position A</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>FEC 933-1662</td>
</tr>
<tr>
<td>1</td>
<td>SL4</td>
<td>3-way solder link, use OR 0603 resistor, insert link in Position C</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>FEC 933-1662</td>
</tr>
<tr>
<td>1</td>
<td>SL5</td>
<td>2-way solder link, use OR 0603 resistor, insert link in Position B</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>FEC 933-1662</td>
</tr>
<tr>
<td>1</td>
<td>SL8</td>
<td>4-way solder link, use OR 0603 resistor, insert link in Position A</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>FEC 933-1662</td>
</tr>
<tr>
<td>2</td>
<td>SL9, SL10</td>
<td>3-way solder link, use OR 0603 resistor, insert link in Position A</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>FEC 933-1662</td>
</tr>
<tr>
<td>1</td>
<td>SL11</td>
<td>4-way solder link, use OR 0603 resistor, insert link in Position A</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>FEC 933-1662</td>
</tr>
<tr>
<td>1</td>
<td>STAR3</td>
<td>Ground link, copper short</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>Not applicable</td>
</tr>
<tr>
<td>1</td>
<td>U1</td>
<td>Serial EEPROM, 32 kb, 1C</td>
<td>Microchip</td>
<td>24LC32A-I/MS</td>
<td>FEC1331330</td>
</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>Qty.</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Stock Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U2</td>
<td>Linear regulator, 5 V, 20 V, 500 mA, ultralow noise, CMOS</td>
<td>Analog Devices, Inc.</td>
<td>ADP7104ARPDZ-5.0</td>
<td>ADP7104ARPDZ-5.0</td>
</tr>
<tr>
<td>1</td>
<td>U3</td>
<td>Quad voltage monitor and sequencer</td>
<td></td>
<td>ADI</td>
<td>ADM1185ARMSZ-1</td>
</tr>
<tr>
<td>1</td>
<td>U4</td>
<td>Linear regulator, 8 V, ~200 mA, low noise</td>
<td>ADI</td>
<td>ADP7182AUXZ</td>
<td>ADP7182AUXZ-R7</td>
</tr>
<tr>
<td>1</td>
<td>U5</td>
<td>ADC</td>
<td>ADI</td>
<td>AD7172-2BRUZ</td>
<td>AD7172-2BRUZ</td>
</tr>
<tr>
<td>1</td>
<td>U6</td>
<td>Reference, 5 V, XFET</td>
<td>ADI</td>
<td>ADI4556BRZ</td>
<td>ADI4556BRZ</td>
</tr>
<tr>
<td>1</td>
<td>U7</td>
<td>Linear regulator 2.5 V, ultralow noise, CMOS</td>
<td>ADI</td>
<td>ADP7118ARPDZ-2.5</td>
<td>ADP7118ARPDZ-2.5-R7</td>
</tr>
<tr>
<td>1</td>
<td>U8</td>
<td>Dual op amp, 5.0 V, ultralow noise, zero drift, rail-rail input output (RRIO)</td>
<td>ADI</td>
<td>ADA4528-2ARMSZ</td>
<td>ADA4528-2ARMSZ</td>
</tr>
<tr>
<td>1</td>
<td>U9</td>
<td>Funnel amplifier, fully differential</td>
<td>ADI</td>
<td>AD8475ARMSZ</td>
<td>AD8475ARMSZ</td>
</tr>
<tr>
<td>1</td>
<td>U10</td>
<td>Linear regulator 3.3 V, ultralow noise, CMOS</td>
<td>ADI</td>
<td>ADP7118ARPDZ-3.3</td>
<td>ADP7118ARPDZ-3.3-R7</td>
</tr>
<tr>
<td>1</td>
<td>U11</td>
<td>Voltage converter, switched capacitor, CMOS</td>
<td>ADI</td>
<td>ADM660ARZ</td>
<td>ADM660ARZ</td>
</tr>
<tr>
<td>1</td>
<td>U12</td>
<td>5.0 V ultralow noise, zero-drift, RRIO, dual op-amp</td>
<td>ADI</td>
<td>ADA4528-2ARMSZ</td>
<td>ADA4528-2ARMSZ</td>
</tr>
<tr>
<td>4</td>
<td>V1 to V4</td>
<td>1206 place holder, do not insert</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Y1</td>
<td>Crystal, miniature, SMD, 16 MHz, 10 ppm, 9 pF</td>
<td>Epson</td>
<td>FA-20H</td>
<td>FEC 171-2814</td>
</tr>
</tbody>
</table>

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).