Evaluation Board for the **AD7124-4** 4-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADC with In-Amp and Reference

### FEATURES
- Full featured evaluation board for the AD7124-4
- PC control in conjunction with the Analog Devices, Inc., System Demonstration Platform (EVAL-SDP-CB1Z)
- PC software for control and data analysis (time domain)
- Standalone capability

### EVALUATION KIT CONTENTS
- EVAL-AD7124-4SDZ evaluation board
- Evaluation software CD for the AD7124-4

### ONLINE RESOURCES
**Documents Needed**
- AD7124-4 data sheet
- EVAL-AD7124-4SDZ user guide

**Required Software**
- AD7124-4 EVAL+ Software

### EQUIPMENT NEEDED
- EVAL-AD7124-4SDZ evaluation board
- EVAL-SDP-CB1Z System Demonstration Platform
- DC signal source
- USB cable
- PC running Windows with USB 2.0 port

### GENERAL DESCRIPTION
The EVAL-AD7124-4SDZ evaluation kit features the AD7124-4 24-bit, low power, low noise analog-to-digital converter (ADC). A 7 V to 9 V external supply is regulated to 3.3 V to supply the AD7124-4 and to support all necessary components. The EVAL-AD7124-4SDZ board connects to the USB port of the PC via the connection to the EVAL-SDP-CB1Z motherboard.

The AD7124-4 EVAL+ Software fully configures the AD7124-4 device register functionality and provides dc time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

The EVAL-AD7124-4SDZ is an evaluation board that allows the user to evaluate the features of the ADC. The user PC software executable controls the AD7124-4 over the USB through the EVAL-SDP-CB1Z System Demonstration Platform (SDP) board.

Full specifications on the AD7124-4 are available in the product data sheet, which should be consulted in conjunction with this user guide when working with the evaluation board.
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REVISION HISTORY

7/15—Revision 0: Initial Version
NOTES
1. FOR SIMPLICITY, DECOUPLING NOT SHOWN.
To begin using the evaluation board, do the following:

1. With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, install the AD7124-4 EVAL+ Software (the software is included on the CD in the evaluation kit, or it can be downloaded from the Analog Devices website). The PC must be restarted after the software installation is complete. (For complete software installation instructions, see the Software Installation Procedures section.)
2. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7124-4SDZ board.
3. Screw the two boards together using the plastic screw and washer set included in the evaluation board kit to ensure that the boards are connected firmly together.
4. Apply an external voltage in the range of 7 V to 9 V to the J3 or J5 connector of the EVAL-AD7124-4SDZ board. This provides the power supply for the board.
5. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable. If you are using Windows® XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.
6. From the Programs menu, go to the Analog Devices subfolder, and click AD7124 Eval+ to launch the AD7124-4 EVAL+ Software (see the Launching the Software section for further details).
EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7124-4 is a low power, low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit, Σ-∆ ADC. It can be configured to have four differential inputs or seven single-ended or pseudo differential inputs. The on-chip low noise instrumentation amplifier means that signals of small amplitude can be interfaced directly to the ADC. Other on-chip features include a low drift 2.5 V reference, excitation currents, reference buffers, multiple filter options, and many diagnostic features.

Complete specifications for the AD7124-4 are provided in the product data sheet, which should be consulted in conjunction with this user guide when using the evaluation board. Full details about the EVAL-SDP-CB1Z are available on the Analog Devices website.

HARDWARE LINK OPTIONS

Table 1 lists the default link options. By default, the board is configured to operate from a wall wart (dc plug) power supply via Connector J5. The supply required for the AD7124-4 comes from the on-board ADP1720 low dropout regulators (LDOs), which generate their voltage from J5.

<table>
<thead>
<tr>
<th>Link No.</th>
<th>Default Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>A</td>
<td>Connects the AVDD voltage to the power supply sequencer, ADM1185. When AVDD equals 3.3 V, LK1 must be in Position A. When AVDD equals 1.8 V, LK1 must be in Position B.</td>
</tr>
<tr>
<td>LK2</td>
<td>B</td>
<td>Selects the connector for the external 7 V to 9 V power supply. In Position A, this link selects the external 7 V to 9 V power supply to come from Connector J3. In Position B, this link selects the external 7 V to 9 V power supply to come from Connector J5.</td>
</tr>
<tr>
<td>LK3</td>
<td>Inserted</td>
<td>Inserting this link connects REFIN(−) to AVSS.</td>
</tr>
<tr>
<td>LK4</td>
<td>2.5 V</td>
<td>Selects the reference source for the ADC. In Position 2.5 V, REFIN1(+) is connected to the external 2.5 V reference (ADR4525). In Position INT REF, REFIN1(+) is connected to the REFOUT pin of the AD7124-4. The internal reference of the AD7124-4 can be enabled and applied to the AD7124-4 external to the ADC.</td>
</tr>
<tr>
<td>LK5</td>
<td>Inserted</td>
<td>This link shorts AIN0 to AIN1. This is useful for performing noise tests on the AD7124-4. The internal bias can be enabled on AIN0 or AIN1 so that AIN0 and AIN1 are at an appropriate voltage for the noise test.</td>
</tr>
<tr>
<td>LK6</td>
<td>Inserted</td>
<td>LK6 can be used to connect the AIN4 and AIN5 channels to external components such as an external amplifier. The jumpers in Position A and Position B at LK6 must be opened to include the external component on the front end. Jumper A and Jumper B of this link can be used to connect the AIN4 and AIN5 channels to external components such as an external amplifier. For this, the jumpers must be open. Having Jumper A and Jumper B in place connects AIN4 and AIN5 to on-board thermistor used for cold junction measurements.</td>
</tr>
<tr>
<td>SL2</td>
<td>A</td>
<td>Sets the voltage applied to the AVDD pin. In Position A, this link sets the voltage applied to the AVDD pin to be a 3.3 V supply from the ADP1720-3.3 (U7) regulator or a 2.5 V supply from the ADP1720 (U4) regulator. In Position B, this link sets the voltage applied to the AVDD pin to be supplied from an external voltage source via Connector J9.</td>
</tr>
<tr>
<td>SL3, SL7</td>
<td>A, A</td>
<td>With SL3 and SL7 in Position A, AVDD is supplied with 3.3 V from the ADP1720-3.3 (U7) regulator. With SL3 and SL7 in Position B, AVDD is supplied with 1.8 V from the ADP1720 (U4) regulator.</td>
</tr>
<tr>
<td>SL5</td>
<td>B</td>
<td>With this link in Position A, the IOVDD supply is provided from an external source via Connector J9. With this link in Position B, the 3.3 V supply is generated by the ADP1720-3.3 (U10) regulator. The evaluation system operates with 3.3 V logic.</td>
</tr>
<tr>
<td>AVSS to AGND</td>
<td></td>
<td>When these links are inserted, AVSS is tied to AGND. When AVSS is set to −1.8 V, these links must be removed.</td>
</tr>
</tbody>
</table>
On-Board Connectors

Table 2 provides information about the external connectors on the EVAL-AD7124-4SDZ.

<table>
<thead>
<tr>
<th>Connector</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>A 120-pin connector that mates with the EVAL-SDP-CB1Z (controller board).</td>
</tr>
<tr>
<td>J2</td>
<td>Straight PCB mount SMB/SMA jack for master clock (not inserted). The EVAL-AD7124-4SDZ has the footprint to include an SMB/SMA connector, if an external clock source is being used to provide the master clock to the ADC.</td>
</tr>
<tr>
<td>J3</td>
<td>Bench top power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board.</td>
</tr>
<tr>
<td>J5</td>
<td>Wall wart (dc plug) power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board.</td>
</tr>
<tr>
<td>J6</td>
<td>Analog input connector. Connections to AIN0 to AIN5 are available along with REFIN1(±) connections. This connector can be used to connect an RTD to the AD7124-4.</td>
</tr>
<tr>
<td>J9</td>
<td>Optional external connector, allowing external bench top or alternative supply for AVDD and IOVDD. When split supplies are used, AVSS is supplied externally via J9.</td>
</tr>
<tr>
<td>J11</td>
<td>Analog input connector. Connections to AIN6 to AIN7 are available along with REFIN1(±) and analog power supply connections. This connector can be used to connect a load cell to the AD7124-4.</td>
</tr>
<tr>
<td>J12</td>
<td>6-pin connector. Provides an I2C interface to allow the SDP to interface to a digital temperature sensor. This is required if a thermocouple is interfaced to the AD7124-4 using Connector A2.</td>
</tr>
<tr>
<td>J13</td>
<td>7-pin connector that can be used to connect an external amplifier to Channel AIN4/Channel AIN5.</td>
</tr>
<tr>
<td>J14</td>
<td>7-pin connector that allows connection to the AIN4 and AIN5 pins.</td>
</tr>
<tr>
<td>A0</td>
<td>Straight PCB mount SMB/SMA jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the signal to the AIN4 analog input.</td>
</tr>
<tr>
<td>A1</td>
<td>Straight PCB mount SMB/SMA jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the signal to the AINS analog input.</td>
</tr>
<tr>
<td>A2</td>
<td>Thermocouple connector. This connector is required if a thermocouple is being interfaced to the evaluation board.</td>
</tr>
<tr>
<td>A5</td>
<td>Straight PCB mount SMB/SMA jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the REFIN1(+) signal.</td>
</tr>
<tr>
<td>A6</td>
<td>Straight PCB mount SMB/SMA jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the REFIN1(−) signal.</td>
</tr>
</tbody>
</table>
POWER SUPPLIES

The evaluation board requires that an external power supply—either a bench top supply or a wall wart (dc plug) supply—be applied to J3 or J5 (see Table 3 for more information). Linear regulators generate the required power supply levels from the applied VIN rail. The regulators used are the ADP1720-3.3 (U7) and the ADP1720 (U4), which supply 3.3 V and 1.8 V, respectively, to AVDD of the ADC. The 3.3 V ADP1720 (U10) delivers 3.3 V to the IOVDD pin of the AD7124-4.

When a split power supply is used, the AVss voltage must be applied from an external source via Connector J9. AVDD and IOVDD can also be provided via Connector J9. However, the 7 V to 9 V supply is still required because the on-board reference (ADR4525) is supplied from this power supply.

Each supply is decoupled at the point where it enters the board and again at the point where it connects to each device (see the schematics shown in Figure 26 to Figure 29 to identify decoupling points).

<table>
<thead>
<tr>
<th>Power Supply (Vin) Applied To</th>
<th>Voltage Range</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J3</td>
<td>7 V to 9 V</td>
<td>Bench top supply to the evaluation board. Supplies LDOs that create the 3.3 V and 1.8 V rails. It also supplies the ADR4525 external reference. Ensure that LK2 is set to Position A when the external power supply is applied to this connector.</td>
</tr>
<tr>
<td>J5</td>
<td>7 V to 9 V</td>
<td>Wall wart (dc plug) supply to the evaluation board. Supplies LDOs that create the 3.3 V and 1.8 V rails. It also supplies the ADR4525 external reference. Ensure that LK2 is set to Position B when the external power supply is applied to this connector.</td>
</tr>
</tbody>
</table>

SERIAL INTERFACE

The EVAL-AD7124-4SDZ evaluation board connects via the serial peripheral interface (SPI) to the Blackfin® ADSP-BF527 on the EVAL-SDP-CB1Z. There are four primary signals: CS, SCLK, DIN, and DOUT/RDY (all are inputs, except for DOUT/RDY, which is an output).

To operate the EVAL-AD7124-4SDZ in standalone mode, the AD7124-4 serial interface lines can be disconnected from the 120-pin header by removing the 0 Ω links, R9 through R13. The test points can then be used to fly-wire the signals to an alternative digital capture setup.

ANALOG INPUTS

The EVAL-AD7124-4SDZ primary analog inputs can be applied in two ways:

- Using J6 and J11, the green screw in terminal connectors
- Using the A0 and A1 SMB/SMA footprints on the evaluation board, which connect to the AIN4 and AIN5 analog inputs.

The AD7124-4 EVAL+ Software is set up to analyze dc inputs to the ADC.
REFERENCE OPTIONS

The EVAL-AD7124-4SDZ includes an external 2.5 V reference (the ADR4525) and an internal 2.5 V reference. The default operation is to use the external reference input, which is set to accept the 2.5 V ADR4525 on the evaluation board.

The reference used for a conversion is selected by choosing the reference in the configuration registers associated with Setup 0 to Setup 7. Switch between using the internal reference and external reference by accessing the AD7124-4 registers through the pop-up windows (discussed in more detail in the following sections) via the evaluation software. Figure 3 shows how to select the reference source for Setup 0 to Setup 7. Figure 4 shows the ADC_CONTROL register setting that enables the internal reference.

EVALUATION BOARD SETUP PROCEDURES

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP boards as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Configuring the Evaluation and SDP Boards

1. Connect the EVAL-SDP-CB1Z board to Connector A or Connector B on the EVAL-AD7124-4SDZ board. Screw the two boards together using the plastic screw and washer set included in the evaluation board kit to ensure that the boards are connected firmly together.
2. Connect the power supplies to the EVAL-AD7124-4SDZ board. The EVAL-AD7124-4SDZ board, by default, uses the wall wart (dc plug) supply that accompanies the evaluation kit. Connect this supply to J5 on the EVAL-AD7124-4SDZ board. (For more information about the required connections and available options, see the Power Supplies section.)
3. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable.
EVALUATION BOARD SOFTWARE
SOFTWARE INSTALLATION PROCEDURES

The EVAL-AD7124-4SDZ evaluation kit includes a CD containing software to be installed on the PC before using the evaluation board.

There are two procedures in the installation:

- AD7124-4 EVAL+ Software installation
- EVAL-SDP-CB1Z SDP board drivers installation

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Installing the AD7124-4 EVAL+ Software

To install the AD7124-4 EVAL+ Software, do the following:

1. With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, insert the installation CD into the CD-ROM drive.
2. Double-click the setup.exe file to begin the evaluation board software installation. The software installs to the following default location: C:\Program Files\Analog Devices\AD7124 EVAL+.
3. A dialog box appears asking for permission to allow the program to make changes to your PC. Click Yes.
4. Select the location to install the software, and then click Next. (Figure 6 shows the default locations, which are displayed when the window opens; you can select another location by clicking Browse.)
5. A license agreement appears. Read the agreement, select I accept the License Agreement, and click Next.

Figure 5. AD7124-4 EVAL+ Software Installation: Granting Permission for the Program to Make Changes to Your PC

Figure 6. AD7124-4 EVAL+ Software Installation: Selecting the Location for Software Installation

Figure 7. AD7124-4 EVAL+ Software Installation: Accepting the License Agreement
6. A summary of the installation displays. Click Next to continue.

![Figure 8](image8.png)

Figure 8. AD7124-4 EVAL+ Software Installation: 
Reviewing a Summary of the Installation

7. The message in Figure 9 appears when the installation is complete. Click Next.

![Figure 9](image9.png)

Figure 9. AD7124-4 EVAL+ Software Installation: 
Indicating When the Installation Is Complete

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**Installing the EVAL-SDP-CB1Z System Demonstration Platform Board Drivers**

After the installation of the evaluation software is complete, a welcome window displays for the installation of the SDP board drivers.

1. With the EVAL-SDP-CB1Z board still disconnected from the USB port of the PC, make sure that all other applications are closed, and then click Next.

![Figure 10](image10.png)

Figure 10. EVAL-SDP-CB1Z Drivers Setup: 
Beginning the Drivers Installation

2. Select the location to install the drivers, and then click Next.

![Figure 11](image11.png)

Figure 11. EVAL-SDP-CB1Z Drivers Setup: 
Selecting the Location for Drivers Installation
3. Click **Install** to confirm that you want to install the drivers.

![Figure 12. EVAL-SDP-CB1Z Drivers Setup: Granting Permission to Install Drivers](image1)

4. To complete the drivers installation, click **Finish**, which closes the setup wizard.

![Figure 13. EVAL-SDP-CB1Z Drivers Setup: Completing the Drivers Setup Wizard](image2)

5. Before using the evaluation board, you must restart the PC.

![Figure 14. EVAL-SDP-CB1Z Drivers Setup: Restarting the PC](image3)

---

### Setting Up the System for Data Capture

After completing the steps in the Software Installation Procedures and Evaluation Board Hardware sections, set up the system for data capture as follows:

1. Allow the **Found New Hardware Wizard** to run after the **EVAL-SDP-CB1Z** board is plugged into your PC. (If you are using Windows XP, you may need to search for the **EVAL-SDP-CB1Z** drivers. Choose to automatically search for the drivers for the **EVAL-SDP-CB1Z** board if prompted by the operating system.)

2. Check that the board is connecting to the PC correctly using the **Device Manager** of the PC.

3. Access the **Device Manager** as follows:
   a. Right-click **My Computer** and then click **Manage**.
   b. A dialog box appears asking for permission to allow the program to make changes to your PC. Click **Yes**.
   c. The **Computer Management** window appears. From the list of **System Tools**, click **Device Manager** (see Figure 15).
   d. The **EVAL-SDP-CB1Z** board should appear under **ADI Development Tools**, which indicates that the driver software is installed and that the board is connecting to the PC correctly.

![Figure 15. Device Manager: Checking that the Board Is Connected to the PC Correctly](image4)
Launching the Software

After completing the steps in the Setting Up the System for Data Capture section, launch the AD7124-4 EVAL+ Software as follows:

1. From the **Start** menu, click **Programs > Analog Devices > AD7124 Eval+ > AD7124 Eval+**. The dialog box in Figure 19 appears; select **EVAL-AD7124-4SDZ**, and the main window of the software then displays as shown in Figure 20.

2. If the AD7124-4 evaluation system is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched, a connectivity error displays (see Figure 16). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and then follow the on-screen instructions.

![Select the Interface to use:](image)

**Figure 16. Connectivity Error Alert**

When the software starts running, it searches for hardware connected to the PC. A dialog box indicates when the generic SDP attached to the PC is detected, and then the main window appears (see Figure 20). Press the **RESET** button on the SDP board, as shown in Figure 17.

![Select the Interface to use:](image)

**Figure 17. SDP Connectivity Board—RESET Button**

Pressing the **RESET** button causes the software to rescan for a connected SDP board. If found, the message shown in Figure 18 displays.

![Select the Interface to use:](image)

**Figure 18. Connectivity when SDP and Evaluation Boards are Found**

SOFTWARE OPERATION

Overview of the Main Window

The evaluation software supports both the AD7124-4 and the AD7124-8 devices. On running the software, the user selects the evaluation board that is connected to the PC. For the AD7124-4, select **EVAL-AD7124-4SDZ** from the drop-down list, as shown in Figure 19.

![Select the Eval Board being used](image)

**Figure 19. EVAL-AD7124-4SDZ Evaluation Board Selection**

After selecting the EVAL-AD7124-4SDZ evaluation board, the main window of the evaluation software displays, as shown in Figure 20. Figure 20 shows the significant control buttons and analysis indicators of the AD7124-4 EVAL+ Software. The main window of the AD7124-4 EVAL+ Software contains four tabs:

- **Configuration**
- **Waveform**
- **Histogram**
- **Register Map**

**CONFIGURATION TAB**

The **Configuration** tab shows a block diagram of the AD7124-4. It allows the user to set up the ADC, reset the ADC, read the diagnostics to see errors present, as well as configure the device for different demo modes. Figure 20 shows the **Configuration** tab in more detail, and the following sections discuss the different elements on the **Configuration** tab of the software window.

**ADC Reset**

Click **ADC RESET** (Label 2) to perform a software reset of the AD7124-4. There is no hardware reset pin on the AD7124-4. A hard reset can be performed by removing power to the board. The software reset has the same effect as a hard reset.

**Selecting External Reference**

There are a number of different options that can be used when selecting the reference to the AD7124-4. Two options are AVdd and **Refin1(+/-)** (Label 3). The **Refin1(+/-)** field sets the external reference voltage that is connected between **REFIN1(+)** and **REFIN1(−)**. Using the EVAL-AD7124-4SDZ evaluation board, the AVDD voltage is 3.3 V. Either of these can be used in calculating the results on the **Waveform** and **Histogram** tabs.

The evaluation board has an external 2.5 V ADR4525 reference, which can be bypassed; if bypassing the ADR4525 on board, be sure to change the external reference voltage value in **Refin1(+/-)** to ensure correct calculation of results in the **Waveform** and **Histogram** tabs.
Tutorial Button
Clicking TUTORIAL (Label 4) opens a tutorial on using the software, which provides additional information on using the AD7124-4 EVAL+ Software.

Functional Block Diagram
The functional block diagram of the ADC (Label 5) shows each of the functional blocks within the ADC. Clicking a configuration button on this graph opens the configuration popup window for that block.

Configuration Pop-Up Button
Each configuration pop-up button (Label 6) opens a different window allowing configuration of the relevant functional block.

CONFIG SUMMARY
Clicking CONFIG SUMMARY (Label 7) displays the channel configuration, information on the individual setups, as well as information on any error present. These tabs can be used to quickly check how the ADC channels are configured, as well as any errors that are present.

Demo Modes
The AD7124-4 EVAL+ Software supports a number of demo modes (Label 8); these demo modes configure the AD7124-4 for each of the modes shown. A help file is available for each demo mode; to access this help file, click the question mark button.

Status Bar
The status bar (Label 9) displays status updates such as Analysis Completed, Reset Completed, and Configuring Demo Mode during software use, as well as the software version and the Busy indicator.

Figure 20. Configuration Tab of the AD7124-4 EVAL+ Software
WAVEFORM TAB

The Waveform tab graphs the conversions and processes the data, calculating the p-p noise, rms noise, and resolution (see Figure 21).

Waveform Graph and Controls
The data waveform graph (Label 1) shows each successive sample of the ADC output. Zoom in on the data using the control toolbar (Label 2) in the graph. Change the scales on the graph by typing values into the x-axis and y-axis.

Analysis Channel
The Noise Analysis section and histogram graph show the analysis of the channel selected via the Analysis Channel control (Label 3).

Samples
The Samples numeric control (Label 4) and batch control (Label 5) set the number of samples gathered per batch and whether a single batch or multiple batches of samples are gathered. This control is unrelated to the ADC mode. The user can capture a defined sample set or continuously gather batches of samples. In both cases, the number of samples set in the Samples numeric input dictates the number of samples.

Sample
Click SAMPLE (Label 6) to start gathering ADC results. Results appear in the waveform graph (Label 1).

Channel Selection
The channel selection control (Label 7) chooses which channels display on the data waveform, and also shows the analog inputs for the channel labeled next to the on and off controls. These controls only affect the display of the channels and have no effect on the channel settings in the ADC register map.

Display Units and Axis Controls
Click the Display Units drop-down list (Label 8) to select whether the data graph displays in units of voltages or codes. This control affects both the waveform graph and the histogram graph. The axis controls can be switched between dynamic and fixed. When dynamic is selected, the axis automatically adjusts to show the entire range of the ADC results after each batch of sample. When fixed is selected, the user can program the axis ranges; the axis ranges do not automatically adjust after each batch of sample.

CRC Error and Overall Error
The CRC Error LED indicator (Label 9) illuminates when a cyclic redundancy check (CRC) error is detected in the communications between the software and the AD7124-4. The CRC functionality on the AD7124-4 is disabled by default and must be enabled for this indicator to work. The Error Present LED indicates if an overall error is present in the diagnostics register. For this indicator to work, the check for the different diagnostic errors must be enabled in the Error_EN register.

Noise Analysis
The Noise Analysis section (Label 10) displays the results of the noise analysis for the selected analysis channel, which includes both noise and resolution measurements.
Figure 21. **Waveform** Tab of the AD7124-4 EVAL+ Software
HISTOGRAM TAB

The Histogram tab generates a histogram using the gathered samples and processes the data, calculating the peak-to-peak noise, rms noise, and resolution (see Figure 22).

Histogram Graph and Controls

The data histogram graph (Label 1) shows the number of times each sample of the ADC output occurs. Zoom in on the data using the control toolbar (Label 6) in the graph. Change the scales on the graph by typing values into the x-axis and y-axis.

Analysis Channel

The Noise Analysis section and histogram graph show the analysis of the channel selected via the Analysis Channel control (Label 2).

Noise Analysis

The Noise Analysis section (Label 3) displays the results of the noise analysis for the selected analysis channel, which includes both noise and resolution measurements.

Display Units and Axis Controls

Click the Display Units drop-down list (Label 4) to select whether the data graph displays in units of voltages or codes. This control affects both the waveform graph and the histogram graph. The axis controls can be switched between dynamic and fixed. When dynamic is selected, the axis automatically adjusts to show the entire range of the ADC results after each batch of sample. When fixed is selected, the user can program the axis ranges; the axis ranges do not automatically adjust after each batch of sample.

CRC Error and Overall Error

The CRC Error LED indicator (Label 5) illuminates when a cyclic redundancy check (CRC) error is detected, in the communications between the software and the AD7124-4. The CRC functionality on the AD7124-4 is disabled by default and must be enabled for this indicator to work. The Error Present LED (Label 5) indicates if an overall error is present in the diagnostics register. For this indicator to work, the check for the different diagnostic errors must be enabled in the Error_EN register.

Figure 22. Histogram Tab of the AD7124-4 EVAL+ Software
REGISTER MAP TAB

Use the Register Map tab to access the registers of the AD7124-4. Figure 23 shows the view when Register Map tab is selected. This tab can be used to quickly change register settings and also to obtain additional information about each of the bits in each of the individual registers.

Register Map

On the left-hand side of Figure 23 are the registers of the AD7124-4. Click any register to read the register value. Each register of the AD7124-4 can be accessed quickly using this register map (Label 1).

Save and Load Buttons

The Save and Load buttons (Label 2) in the Register Map tab allow the user to save and load register settings. Click Save to save all the current register settings to a file for use again later. Click Load to load a previously saved register map.

Register

The Register section (Label 3) shows the value that is currently set in the selected register. The value of the register can be checked in this section by clicking the bits that are to be changed. Clicking any of the individual bit changes that bit from 1 to 0 or 0 to 1, depending on the initial state of the bit. The register value can also be changed by writing the hex value to the input field on the right-hand side of the individual bits.

Bitfields

The individual bitfields of the selected register are shown in the Bitfields section (Label 4). In this section, the register is broken by name into its bitfields, name of the bitfields, a description of each of each bitfield, as well as the access information. The options for the individual bitfields can be viewed by clicking the arrow next to the bitfield. Changing the bitfield value can also be done through this drop-down list. The value of the bitfield can also be changed by writing the appropriate hex value to the associated Value input field on the right-hand side of the bitfield.

Documentation

The Documentation section (Label 5) shows information relating to the different bit fields when selected from the register map section on the left. This information is the same information that is presented in the AD7124-4 data sheet.

---

Figure 23. Register Map Tab of the AD7124-4 EVAL+ Software
NOISE TEST—QUICK START DEMONSTRATION

Click the NOISE TEST demo button to configure the device for the noise test. The AD7124-4 is now configured for the noise test demo, where the output data rate is set to 9.38 SPS, with the sinc4 digital filter, full power mode of operation, and the REFIN1(±) external reference selected. Gain and offset are the default factory values following a reset.

To gather samples, change the Samples field to the number of samples required value, then click SAMPLE to acquire the samples from the ADC. Figure 24 shows an example of the main window after running a noise test.

Reading Samples from the ADC

The evaluation board is set up to use the external 2.5 V on-board reference (ADR4525). To read samples from the ADC, take the following steps:

1. The value in the Refin1(+-) field on the Configuration tab is set to 2.5 V by default to use the external 2.5 V on-board reference (ADR4525). If a different reference is used, set the value in the Refin1(+-) field accordingly. The analysis results are based on the value set in this field.
   a. When Single Run is selected from the drop-down list, a batch of samples is read when SAMPLE is clicked, with the batch size being set by the value in the Samples box.
   b. When the drop-down box is set to Continuous Run, the software performs a continuous capture from the ADC when SAMPLE is clicked.
   c. Click Stop to stop streaming data.

2. Use the navigation tools within each graph to control the cursor, zooming, and panning.

Waveform

The waveforms resulting from the gathered samples are shown in this tab. The waveform graph shows each successive sample of the ADC output (input referred). The indicators beside this graph show the channels being converted. Navigation tools are provided to allow the user to control the cursor, zooming, and panning. The conversions can be displayed as codes or as volts.

Parameters such as peak-to-peak noise and rms noise are displayed below the graph in the Analysis section for the current batch of samples. If several analog input channels are enabled, each enabled channel can be selected and the conversions on that channel analyzed using Analysis Channel.

The conversion data can be saved in a text file from the File menu. To save the data into an Excel file, right-click the waveform graph and select Export Data from the drop-down list that appears. A Save dialog box displays, prompting the user to save the data to an appropriate folder location.

Figure 24. Example of the Waveform Tab After Running a Noise Test
**Histogram**

This tab shows the histogram analysis. The indicators beside this graph show the channels being converted. Navigation tools are provided to allow you to control the cursor, zooming, and panning. The conversions can be displayed as codes or as volts.

Parameters such as peak-to-peak noise and rms noise are displayed in the **Analysis Results** section for the current batch of samples.

The conversion data can be saved in a text file from the **File** at menu. To save the data into an Excel file, right-click the histogram graph and select **Export Data** from the drop-down list that appears. A **Save** dialog box displays, prompting the user to save the data to an appropriate folder location.

*Figure 25. Example of the Histogram Tab After Running a Noise Test*
Figure 26. Schematic
Figure 27. Schematic—Power Supply
Figure 28. Schematic—Regulators
Figure 29. Schematic—SDP

SDP CONNECTOR  EEPROM—SW/USB ID

VDD: Use to set ID voltage max draw 20mA
VIN Use this pin to power the SDP requires 4.7V 200mA

Note: Pull up with a 10K resistor to set SDP to boot from a SPI FLASH on the daughter board.
Figure 30. Top Printed Circuit Board (PCB) Silkscreen
Figure 31. Layer 1—Component Side

Figure 32. Layer 2—Ground Plane
## BILL OF MATERIALS

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part No.</th>
<th>Stock Code</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A0, A1, A5, A6, J2</strong></td>
<td>Straight PCB mount SMB jack, keep hole clear of solder</td>
<td>Tyco</td>
<td>1-1337482-0</td>
<td>Do not insert</td>
</tr>
<tr>
<td>A2</td>
<td>Miniature thermocouple connector</td>
<td>Omega</td>
<td>PCC-SMP-U-50</td>
<td>Do not insert</td>
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<tr>
<td>C1, C17, C29, C30, C43, C47</td>
<td>Capacitor, ceramic, 6.3 V, X5R, 0603, 4.7 µF, ±10%</td>
<td>Murata</td>
<td>GRM188R60J475K</td>
<td>FEC 173-5527</td>
</tr>
<tr>
<td>C2, C22, C25, C26, C36, C38, C54, C55</td>
<td>Capacitor, ceramic, 50 V, X7R, 0603, 0.1 µF, ±10%</td>
<td>Murata</td>
<td>GRM188R71H104K</td>
<td>FEC 882-0023</td>
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<tr>
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<td>Capacitor, ceramic, 10 V, X5R, 0603, 4.7 µF, ±10%</td>
<td>Kemet</td>
<td>C0603C475K8PACTU</td>
<td>FEC 157-2625</td>
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<td>Capacitor, ceramic, 10 V, X7R, 1 µF, ±10%</td>
<td>Murata</td>
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<td>FEC 173-5541</td>
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<td>C5, C9, C7, C8, C9, C16</td>
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<td>N/A</td>
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<tr>
<td>C10 to C12, C24, C27, C28</td>
<td>Ceramic capacitor, 50 V, NPO, 0603, 0.01 µF</td>
<td>Phycomp</td>
<td>223B 586 15636</td>
<td>FEC 722-236</td>
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<td>C13, C14, C18, C20, C21, C31, C33, C34, C44, C50 to C53</td>
<td>Capacitor, ceramic, 16 V, X7R, 0402, 0.1 µF, ±10%</td>
<td>Murata</td>
<td>GRM155R71C104K</td>
<td>FEC 881-9742</td>
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<td>Capacitor, 6.3 V, 1 µF, ±10%</td>
<td>Murata</td>
<td>GRM188R70J105KA01D</td>
<td>FEC 184-5765</td>
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<td>C19, C59</td>
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<td>GRM32ER61H106K</td>
<td>FEC 184-5764</td>
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<td>D2, D6</td>
<td>Red LED, high intensity (&gt;90 mCd), 0603</td>
<td>Avago Tech</td>
<td>HSMC-C191</td>
<td>FEC 855-8528</td>
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<td>D4</td>
<td>LED, SMD, green</td>
<td>OSRAM</td>
<td>LGQ971</td>
<td>Digike 475-1409-1-ND</td>
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<td>D5</td>
<td>Diode, Zener, 0.5 W, 5.1 V, BZTS2</td>
<td>Vishay</td>
<td>BZTS2BSV1-V-G508</td>
<td>FEC 161-7767</td>
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<td>GND, GN1 to GND6, MCLK, REF+, REF−, REFOUT, S1 to S8, S1’ to S8’</td>
<td>Test point, not inserted, keep hole clear of solder</td>
<td>N/A</td>
<td>N/A</td>
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<td>J1</td>
<td>120-way connector, 0.6 mm pitch</td>
<td>Hirose</td>
<td>FXB-120S-S(21)</td>
<td>FEC 132-4660</td>
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<td>Socket terminal block, 3.81 mm pitch</td>
<td>Phoenix Contact</td>
<td>MC 1.5/3-G-3.81</td>
<td>FEC 370-4737</td>
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<td>Screw terminal block, pitch 3.81 mm</td>
<td>Phoenix Contact</td>
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<tr>
<td>J5</td>
<td>DC power connectors, 2 mm, SMT, power jack</td>
<td>Kycon</td>
<td>KLDX-SMT2-0202-A</td>
<td>MOUSER 806-KLDX-SMT2020A</td>
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<td>Phoenix Contact</td>
<td>MC 1.5/ 8-G-3.81</td>
<td>FEC 370-4774</td>
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<tr>
<td>J7</td>
<td>Connector, pitch 3.81 mm, right angle, 1 x 4-pin</td>
<td>Phoenix Contact</td>
<td>MC 1.5/ 4-G-3.81 and 180-3594</td>
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<td>1727078</td>
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<td>Phoenix Contact</td>
<td>1727036</td>
<td>FEC 370-4592</td>
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<td>PCB pads, 6-way solder slot for Analog Devices PCB, 6-way</td>
<td>Aragon</td>
<td>ADT7320-CJC-PCB</td>
<td>ADT7320-CJC-PCB</td>
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<td>Samtec</td>
<td>SSW-107-01-T-S</td>
<td>FEC 180-3478</td>
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<td>J14</td>
<td>7-way sip, 2.54 mm, TH header</td>
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<td>TLW-107-05-G-S</td>
<td>FEC 166-8499</td>
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<td>Do not insert</td>
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<td>N/A</td>
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<td>L3</td>
<td>Ferrite bead, 0.3 Ω at dc, 1000 Ω at 100 MHz, 350 mA, 8050, 1000 Ω</td>
<td>Tyco</td>
<td>BMB2A1000LN2</td>
<td>FEC 119-3421</td>
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<td>LK1, LK2</td>
<td>3-pin (3x1), 0.1” header and shorting block in Position A</td>
<td>Harwin</td>
<td>M20-9990346 and M7566-05</td>
<td>FEC 102-2249 and 150-411</td>
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<td>Manufacturer</td>
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<td>2-pin (0.1&quot; pitch) header and shorting shunt</td>
<td>Harwin</td>
<td>M20-9990246</td>
<td>FEC 102-2247 and 150-411</td>
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<td>Harwin</td>
<td>M20-9983646 and M7566-05</td>
<td>FEC 1022244 and 150-411 (36-pin strip)</td>
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<td>Q1</td>
<td>MOSFET transistor</td>
<td>Vishay Siliconix</td>
<td>SI2304DDS-T1-GE3</td>
<td>FEC 185-8939</td>
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<td>Q2</td>
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<td>ON Semiconductor</td>
<td>MMBT3904LTIG</td>
<td>FEC 145-9100</td>
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<td>Multicomp</td>
<td>MC 00625W 0603 1% 100K</td>
<td>FEC 933-0402</td>
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<td>Vishay</td>
<td>CRCW040210K0FKEAHP</td>
<td>FEC 173-8864</td>
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<tr>
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<td>Multicomp</td>
<td>MC 00625W 0402 1% 30K</td>
<td>FEC 135-8082</td>
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<td>Resistor, 0402, 1%, 30 kΩ</td>
<td>Multicomp</td>
<td>MC 00625W 0402 1% 10K2</td>
<td>FEC 180-3137</td>
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<tr>
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<td>SMD resistor, 10.2 kΩ, 1%</td>
<td>Multicomp</td>
<td>MC 00625W 0402 1% 69K</td>
<td>FEC 180-3735</td>
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<td>R16</td>
<td>Resistor, 0402, 69.9 kΩ</td>
<td>Vishay Dale</td>
<td>CRCW0402K53F7KED</td>
<td>FEC 115-1244</td>
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<tr>
<td>R23</td>
<td>Resistor, 0402, 1%, 86.6 kΩ</td>
<td>Multicomp</td>
<td>MC 00625W 0402 1% 86K6</td>
<td>FEC 180-3744</td>
</tr>
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<td>Multicomp</td>
<td>MC 00625W 0402 1% 15K</td>
<td>FEC 1358073</td>
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<td>Multicomp</td>
<td>MC 00625W 0603 1% 1K</td>
<td>FEC 933-0380</td>
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<tr>
<td>R28</td>
<td>Thermistor, 1950 Ω to 1990 Ω</td>
<td>Infineon</td>
<td>Q62705-K110</td>
<td>Philips (Arrow) KTY81/110</td>
</tr>
<tr>
<td>R31, R90</td>
<td>Resistor, not inserted, 0402</td>
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<td>N/A</td>
<td>Do not insert</td>
</tr>
<tr>
<td>R33, R34, R39, R47, R81 to R84, R87, R89</td>
<td>Resistor, 0603, 0 Ω, 1%</td>
<td>Vishay Draloric</td>
<td>CRCW06030000Z0EA</td>
<td>FEC 146-9739</td>
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<td>R42 to R45</td>
<td>Resistor, thick film, 10 kΩ, 62.5 mW, 5%</td>
<td>Yageo</td>
<td>RC0402JR-1310KL</td>
<td>FEC 179-9316</td>
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<tr>
<td>R49 to R52</td>
<td>Resistor, 1206, 0 Ω, 5%</td>
<td>Multicomp</td>
<td>MC 0125W 1206 0R</td>
<td>FEC 933-9674</td>
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<td>R53</td>
<td>Resistor, 0402, 27 kΩ, 1%</td>
<td>Multicomp</td>
<td>MC 00625W 0402 1% 27K</td>
<td>FEC 135-8081</td>
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<td>R54</td>
<td>Resistor, thick film, 4.53 kΩ, 63 mW, 1%</td>
<td>Vishay Dale</td>
<td>CRCW0402K53F7KED</td>
<td>FEC 115-1244</td>
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<td>R55</td>
<td>Resistor, 0402, 1%, 61.9 Ω</td>
<td>Multicomp</td>
<td>MC 00625W 0402 1% 61R9</td>
<td>FEC 180-2915</td>
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<td>R56</td>
<td>Resistor, 0402, 57.6 kΩ, 1%</td>
<td>Multicomp</td>
<td>MC 00625W 0402 1% 57K6</td>
<td>FEC 185-1295</td>
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<td>R60</td>
<td>Resistor, thick film, 2.4 kΩ, 0603, 100 mW, 1%</td>
<td>Yageo</td>
<td>RC0603FR-072K4L</td>
<td>FEC 179-9329</td>
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<td>R88</td>
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<td>N/A</td>
<td>N/A</td>
<td>Do not insert</td>
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<tr>
<td>SL2, SL3, SL7</td>
<td>2-way solder link (use 0 Ω, 0603 resistor)</td>
<td>N/A</td>
<td>Insert in Link Position A</td>
<td>FEC 933-1662</td>
</tr>
<tr>
<td>SL5</td>
<td>2-way solder link (use 0 Ω, 0603 resistor)</td>
<td>N/A</td>
<td>Insert in Link Position B</td>
<td>FEC 933-1662</td>
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<td>STAR3</td>
<td>Ground link</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
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<td>U1</td>
<td>32k i²C serial EEPROM</td>
<td>Microchip</td>
<td>24LC32A-I/M5</td>
<td>FEC133-1330</td>
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<td>U2</td>
<td>Linear regulator 5 V, 20 V, 500 mA, ultralow noise, CMOS</td>
<td>Analog Devices</td>
<td>ADP7104ARDZ-5.0</td>
<td>ADP7104ARDZ-5.0</td>
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<tr>
<td>U3</td>
<td>Quad voltage monitor and sequencer</td>
<td>Analog Devices</td>
<td>ADM1185ARZM-1</td>
<td>ADM1185ARZM-1</td>
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<td>U4</td>
<td>50 mA, high voltage, micropower linear regulator, ADJ</td>
<td>Analog Devices</td>
<td>ADP1720ARMZ-R7</td>
<td>ADP1720ARMZ-R7</td>
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<tr>
<td>U5</td>
<td>4-channel, low power, low noise, Σ-Δ ADC</td>
<td>Analog Devices</td>
<td>AD7124-8BCPZ</td>
<td>AD7124-8BCPZ</td>
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<td>U6</td>
<td>2.5 V low noise reference</td>
<td>Analog Devices</td>
<td>ADR4525BRZ</td>
<td>ADR4525BRZ</td>
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<td>ADP1720ARMZ-3.3-R7</td>
<td>ADP1720ARMZ-3.3-R7</td>
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<td>V1 to V4</td>
<td>1206, place holder</td>
<td>N/A</td>
<td>N/A</td>
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1 N/A means not applicable.