Evaluating the AD5380/AD5382 40-/32-Channel, 14-Bit Voltage Output DACs with On-Chip Reference

**FEATURES**

- Full featured evaluation board for the AD5380/AD5382
- On-board reference
- Various link options
- PC control in conjunction with the Analog Devices, Inc., EVAL-SDP-CB1Z system demonstration platform (SDP)

**ONLINE RESOURCES**

**Documents Needed**
- AD5380/AD5382 data sheets
- EVAL-AD5380SDZ/EVAL-AD5382SDZ user guide

**Required Software**
- AD538x evaluation software (download from the EVAL-AD5380SDZ/EVAL-AD5382SDZ product pages)

**ADDITIONAL EQUIPMENT AND SOFTWARE NEEDED**

- EVAL-SDP-CB1Z system demonstration platform, includes a USB cable
- PC running Windows XP SP2, Windows Vista, or Windows 7 with USB 2.0 port

**EVALUATION KIT CONTENTS**

- EVAL-AD5380SDZ/EVAL-AD5382SDZ evaluation board
- CD includes
  - Self-installing evaluation software that allows users to control the board and exercise all functions of the device
  - Electronic version of the EVAL-AD5380SDZ/EVAL-AD5382SDZ user guide

**TYPICAL EVALUATION SETUP**

Figure 1.
Table of Contents

Features ................................................................. 1
Evaluation Kit Contents ............................................. 1
Additional Equipment and Software Needed .......... 1
Online Resources ..................................................... 1
Typical Evaluation Setup ........................................... 1
Revision History ...................................................... 2
General Description ................................................ 3
Getting Started ....................................................... 4
  Installing the Software ......................................... 4
  Evaluation Board Setup Procedures ..................... 4
Evaluation Board Hardware ..................................... 5
  Power Supplies ................................................... 5
  Input Signals ....................................................... 5
  Output Signals .................................................... 5
  Link Configuration Options ................................ 6
  Setup Conditions ................................................ 6
  Evaluation Board Circuitry .................................... 7
  How to Use the Software ....................................... 8
    Starting the Software ........................................ 8
    Overview of the Main Window ......................... 8
  Evaluation Board Schematics .............................. 10
  Ordering Information .......................................... 12
    Bill of Materials ............................................... 12

Revision History

12/14—Rev. 0 to Rev. A
Changes to Table 2 ................................................ 6

9/14—Revision 0: Initial Version
GENERAL DESCRIPTION

This user guide details the operation of the evaluation boards for the AD5380/AD5382 40-/32-channel, 14-bit voltage output digital-to-analog converter (DAC) with on-chip reference.

The EVAL-AD5380SDZ/EVAL-AD5382SDZ evaluation boards are designed to help users quickly prototype new AD5380/AD5382 circuits and reduce design time. Each evaluation board is populated with an AD5380BSTZ-5 (EVAL-AD5380SDZ) or an AD5382BSTZ-5 (EVAL-AD5382SDZ). Each AD5380/AD5382 operates from a 4.5 V to 5.5 V analog supply and from a 2.7 V to 5.5 V digital supply. The AD5380/AD5382 incorporate an internal 1.25 V/2.5 V reference to attain an output voltage span of 2.5 V or 5 V. An external reference (a 2.5 V reference is provided on the evaluation board) can also be used to attain an output from 0 V to V_{REF}.

Full data on the AD5380 and AD5382 can be found in the respective product data sheets, which should be consulted in conjunction with this user guide when using the evaluation board.

The evaluation boards interface to the USB port of a PC via the EVAL-SDP-CB1Z SDP-B controller board, which is available for order on the Analog Devices website at www.analog.com. Software is supplied with the evaluation board to allow the user to program the AD5380/AD5382. Only the SPI interface is supported by the software.

The evaluation boards can be used without the SDP-B controller board. Digital control signals can be applied via Connector J1 or Connector J2, and power supplies can be connected to Connector J7 and Connector J8.
GETTING STARTED
INSTALLING THE SOFTWARE

The evaluation kit for the AD5380/AD5382 includes self-installing software on a CD. The software is compatible with Windows® XP, Windows Vista (32-bit version), and Windows 7 (32-bit and 64-bit versions). The software must be installed before connecting the SDP board to the USB port of the PC to ensure that the SDP board is recognized when it is connected to the PC.

To install the software, take the following steps:

1. Start the Windows operating system and insert the CD.
2. The installation software should open automatically. If it does not open automatically, run the setup.exe file from the CD.
3. After installation is completed, power up the evaluation board as described in the Power Supplies section.
4. Connect the evaluation board to the SDP board and connect the SDP board to the PC using the USB cable included in the EVAL-SDP-CB1Z kit.
5. When the software detects the evaluation board, proceed through any dialog boxes that appear to finalize the installation.

EVALUATION BOARD SETUP PROCEDURES

To set up the evaluation board, take the following steps:

1. Connect the evaluation board to the SDP board, and connect the USB cable between the SDP board and the PC.
2. Power the SDP and evaluation boards by connecting 6 V to Connector J9.
EVALUATION BOARD HARDWARE

POWER SUPPLIES

To use the evaluation board with the SDP board, a 6 V power supply is required. The supply is connected to Connector J9. Two voltage regulators on the evaluation board generate the 5 V analog and digital supplies. These supplies are applied to the AD5380/AD5382 when the LK1 and LK2 links are in Position A. The digital supply is also used to power the SDP board.

The evaluation board can be used without the SDP board. In this case, Connector J7 is the AVCC power supply input, and Connector J8 is the DVCC power supply input. The LK1 and LK2 links must be in Position B.

AGND and DGND inputs are provided on the board. The AGND and DGND planes are connected at one location close to the AD5380/AD5382. It is recommended that AGND and DGND not be connected elsewhere in the system to avoid ground loop problems.

All supplies are decoupled to ground using 10 µF tantalum and 0.1 µF ceramic capacitors.

Table 1. Power Supply Connectors

<table>
<thead>
<tr>
<th>Connector Number</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>J7</td>
<td>Analog power supply, AVCC</td>
</tr>
<tr>
<td>J8</td>
<td>Digital power supply, DVCC</td>
</tr>
<tr>
<td>J9</td>
<td>6 V board positive power supply</td>
</tr>
</tbody>
</table>

INPUT SIGNALS

When the SDP board is used to control the AD5380/AD5382 evaluation board, the digital input signals are applied to Connector J10. When the SDP board is not used, apply the digital signal to Header J1 or Header J2.

OUTPUT SIGNALS

The DAC output voltages are available on the 40-way header, J3. VOUT 0 is also available on J5. MON_OUT is available on J6.

Figure 2. Evaluation Board Block Diagram
LINK CONFIGURATION OPTIONS

Multiple jumper (LKx) options must be set correctly to select the appropriate operating setup before using the evaluation board. The functions of these options are described in Table 2.

SETUP CONDITIONS

Before applying power and signals to the evaluation board, ensure that all link positions are as required by the operating mode. There are two modes in which to operate the evaluation board. The evaluation board can be operated in SDP controlled mode to be used with the SDP board, or the evaluation board can be used in standalone mode.

The Default Position column of Table 2 shows the default positions in which the links are set when the evaluation board is packaged. When the board is shipped, the evaluation board is set up to operate with the SDP board in SDP controlled mode.

Table 2. Link Functions

<table>
<thead>
<tr>
<th>Link No.</th>
<th>Function</th>
<th>Default Position</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>This link selects the source of the AVCC supply. Position A selects a 5 V supply from the ADP3331 (U3). Position B selects the external power supply connected to J7.</td>
<td>A</td>
</tr>
<tr>
<td>LK2</td>
<td>This link selects the source of the DVCC supply. Position A selects a 5 V supply from the ADP3367 (U5). Position B selects the external power supply connected to J8.</td>
<td>A</td>
</tr>
<tr>
<td>LK3 to LK5</td>
<td>These links select the logic level for LDAC, CLR, and RESET, respectively. When a link is inserted, the relevant pin is connected to DGND. When the link is removed, the relevant pin is pulled to DVCC. Remove these links when using the SDP controller board.</td>
<td>Removed</td>
</tr>
<tr>
<td>LK6</td>
<td>This link sets the logic level of the PD pin. Position A puts the AD5380/AD5382 into power-down mode. Position B puts the AD5380/AD5382 into normal operating mode.</td>
<td>B</td>
</tr>
<tr>
<td>LK7</td>
<td>This link selects the source for the REFOUT/REFIN pin. In Position A, an external reference source can be connected to Connector J4. Use this option if the AD5380/AD5382 internal reference is used. In Position B, the reference source comes from the ADR421 2.5 V reference.</td>
<td>B</td>
</tr>
<tr>
<td>LK8</td>
<td>This link enables/disables the FIFO function. In Position A, the FIFO function is enabled. In Position B, the FIFO function is disabled. The software supplied with the AD5380/AD5382 evaluation board does not support FIFO operation.</td>
<td>B</td>
</tr>
<tr>
<td>LK9</td>
<td>This link selects serial or parallel interface operation of the AD5380/AD5382. In Position A, a serial interface is selected. LK10 determines if an SPI or i2C interface is used. The software supplied with the AD5380/AD5382 evaluation board only supports the SPI interface. In Position B, the parallel interface is selected. Parallel interface signals are applied to the AD5380/AD5382 using Connector J2.</td>
<td>A</td>
</tr>
<tr>
<td>LK10</td>
<td>This link selects the SPI or i2C interface mode of the AD5380/AD5382. Position A selects the i2C interface mode. Position B selects the SPI interface mode. Select this option when the evaluation board is used with the SDP controller board.</td>
<td>B</td>
</tr>
<tr>
<td>LK11</td>
<td>This link position is determined by the function of the CS/SYNC/A0 pin. When the AD5380/AD5382 are used in i2C mode, this pin determines the state of the A0 address bit. In Position A the address bit is 1 In Position B, the address bit is 0 Remove this link when the AD5380/AD5382 are used in SPI or parallel mode.</td>
<td>Removed</td>
</tr>
<tr>
<td>LK12</td>
<td>This link position is determined by the function of the WR/DCEN/A1 pin. When the AD5380/AD5382 are used in i2C mode, this pin determines the state of the A1 address bit. In Position A, the address bit is 1. In Position B, the address bit is 0. Remove this link when the AD5380/AD5382 are used in SPI mode, this pin enables/disables daisy-chain mode. In Position A, daisy-chain mode is enabled. The AD5380/AD5382 evaluation software does not support daisy-chain mode. In Position B, daisy-chain mode is disabled. Remove this link when the AD5380/AD5382 are used in parallel mode.</td>
<td>B</td>
</tr>
</tbody>
</table>
EVALUATION BOARD CIRCUITY

The EVAL-AD5380SDZ/EVAL-AD5382SDZ evaluation boards allow the function and performance of the AD5380/AD5382 to be easily tested. Each evaluation board contains two voltage regulators that generate the analog and digital power supplies and that also power the SDP board if it is connected. The two regulators are powered via a 6 V supply attached to Connector J9. Alternatively, separate analog and digital supplies can be attached via Connector J7 and Connector J8, respectively.

Control of the AD5380/AD5382 is typically performed by the SDP board, which is attached to Connector J10. The SDP board allows the software provided with the kit to be used to load register values, set the voltage of the DAC outputs, and write to the control register of the AD5380/AD5382. When the SDP board is not required, the control signals can be applied to the AD5380/AD5382 by connecting them to the relevant pins on Connector J1 or Connector J2.

In addition to the on-chip reference of the AD5380/AD5382, an external 2.5 V reference is also provided and can be connected to the REFOUT/REFIN pin of the AD5380/AD5382 using Link LK7. The DAC output voltages are available on the 40-way header, J3.
HOW TO USE THE SOFTWARE

STARTING THE SOFTWARE

To run the program, take the following steps:

1. Connect the evaluation board to the SDP board, and connect the USB cable between the SDP board and the PC.
2. Power the SDP board and the evaluation board by connecting 6 V to Connector J3.
3. Click Start > All Programs > Analog Devices > AD538x > AD538x Evaluation Software. When the software connects to the evaluation board, the message shown in Figure 3 displays.

4. If the SDP board is not connected to the USB port when the software is launched, a connectivity error displays (see Figure 4), and the software continues to operate in simulation mode. In simulation mode, the user can exercise all the functionality of the AD5380/AD5382. Expected output voltages are displayed based on the input data, and the 24 bits of data that would have been sent to the AD5380/AD5382 are displayed at the bottom right of the screen.

OVERVIEW OF THE MAIN WINDOW

The main window of the AD5380/AD5382 evaluation software is shown in Figure 5. The DAC Registers tab allows the X, M, and C registers of individual DACs to be programmed. LDAC is high by default. Click Pulse LDAC to update the outputs. The software displays the expected output voltages based on the register contents and the voltage reference value.

Figure 6 shows the Control & Special Function Registers tab. This tab allows the user to select the functions contained in the control register of the AD5380/AD5382. This tab also allows control of the LDAC and CLR pins.

The user can reset the AD5380/AD5382 by clicking Hardware Reset or Software Reset from the File menu.
Figure 5. Main Window, **DAC Registers** Tab

Figure 6. Main Window, **Control & Special Function Registers** Tab
EVALUATION BOARD SCHEMATICS

Figure 7. EVAL-AD5380SDZ/EVAL-AD5382SDZ Schematic, Page 1 of 2
Figure 8. EVAL-AD5380SDZ/EVAL-AD5382SDZ Schematic, Page 2 of 2
## ORDERING INFORMATION

### BILL OF MATERIALS

<table>
<thead>
<tr>
<th>Qty</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Supplier/Part Number</th>
<th><strong>Note</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>C1, C3, C5, C10, C12, C14, C15, C17, C18</td>
<td>Capacitor, Case A, 10 µF, 10 V</td>
<td>FEC 197-130</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>C2, C4, C6, C7, C9, C11, C13, C16</td>
<td>Capacitor, 100 nF, 50 V, 0603</td>
<td>FEC 8820023</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>C8</td>
<td>Unpopulated capacitor location, keep holes free of solder</td>
<td>Do not insert</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J1</td>
<td>7-pin (1x7) header, 0.1” pitch</td>
<td>FEC 1022257</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J2</td>
<td>28-pin (2x14) SMT header, 0.1” pitch</td>
<td>Digi-Key M20-8761446-ND</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J3</td>
<td>40-pin (2x20), 0.1” pitch, SMT header</td>
<td>Digi-Key M20-8762046-ND</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>J4 to J6</td>
<td>50 Ω, straight SMT jack</td>
<td>FEC 1111349</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>J7 to J9</td>
<td>2-pin terminal block (5 mm pitch)</td>
<td>FEC 151789</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J10</td>
<td>120-way female connector, 0.6 mm pitch</td>
<td>FEC 1324660 or Digi-Key H1219-ND</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>Ferrite bead</td>
<td>Digi-Key 490-1024-1-ND</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>LK1, LK2, LK6 to 12</td>
<td>3-pin SIL header, 0.1” pitch, and red jumper</td>
<td>FEC 1022248 &amp; 150411</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>LK3, LK4</td>
<td>2-pin SIL header, 0.1” pitch, and red jumper</td>
<td>FEC 1022247 &amp; 150-411</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>R1, R2</td>
<td>Resistor, 0603, 1%, 0 Ω</td>
<td>FEC 9331662</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>R3 to R6</td>
<td>Resistor, 10 kΩ, 0.063 W, 1%, 0603</td>
<td>FEC 9330399</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>R7</td>
<td>Unpopulated resistor location, keep holes free of solder</td>
<td>Do not insert</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>R8</td>
<td>Resistor, 1.5 Ω, 0.063 W, 1%, 0603</td>
<td>FEC 9330640</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>R9</td>
<td>Resistor, 300 kΩ, 0.063 W, 1%, 0603</td>
<td>FEC 9330992</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>R10</td>
<td>Resistor, 1 MΩ, 0.063 W, 1%, 0603</td>
<td>FEC 9330410</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>R11 to R13</td>
<td>SMD resistor, 0603</td>
<td>Do Not insert</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>R14, R15</td>
<td>Resistor, 100 kΩ, 0.063 W, 1%, 0603</td>
<td>FEC 9330402</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>TP1 to TP10</td>
<td>Black test point</td>
<td>FEC 8731128</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>U1</td>
<td>40-/32-channel, 14-bit DAC</td>
<td>AD5380BSTZ-5/AD5382BSTZ-5</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>U2</td>
<td>2.5 V reference</td>
<td>ADR421ARZ</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>U3</td>
<td>Adjustable LDO regulator</td>
<td>ADP3331ARTZ</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>U4</td>
<td>32k iC serial EEPROM</td>
<td>FEC 1331330</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>U5</td>
<td>5 V fixed, adjustable voltage regulator</td>
<td>ADP3367ARZ</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Screw1, Screw2</td>
<td>Screw, cheese, nylon, M3X10, PK100</td>
<td>FEC 7070597</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Nut1, Nut2</td>
<td>Nut/washer, nylon, M3, PK100</td>
<td>FEC 7061857</td>
<td></td>
</tr>
</tbody>
</table>

1. FEC is Farnell Electronics Components.
I2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the “Evaluation Board”), you are agreeing to be bound by the terms and conditions set forth below (“Agreement”) unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you (“Customer”) and Analog Devices, Inc. (“ADI”), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board; and (iii) permit any Third Party to access the Evaluation Board. As used herein, the term “Third Party” includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED “AS IS” AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER’S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI’S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). Export. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.