Evaluating the ADF4371 Microwave Wideband Synthesizer with Integrated VCO

FEATURES
Self-contained board, including ADF4371 frequency synthesizer with integrated VCO, loop filter (180 kHz), USB interface, and voltage regulators
Windows®-based software allows control of synthesizer functions from a PC
Externally powered by 6 V

REQUIRED SOFTWARE
ACE software, Version 1.10 or newer
ADF4371 plugin, Version 0.1.6 or newer

GENERAL DESCRIPTION
The EV-ADF4371SD2Z evaluates the performance of the ADF4371 frequency synthesizer with an integrated voltage controlled oscillator (VCO) for phase-locked loops (PLLs). A photograph of the evaluation board is shown in Figure 1. The evaluation board contains the ADF4371 frequency synthesizer with an integrated VCO, a USB interface, power supply connectors, and subminiature Version A (SMA) connectors.

This board requires an SDP-S board (not supplied with the kit). The SDP-S allows software programming of the EV-ADF4371SD2Z device.

Full specifications for the ADF4371 frequency synthesizer are available in the product data sheet, which must be consulted in conjunction with this user guide when working with the evaluation board.

EVALUATION BOARD PHOTOGRAPH

Figure 1.
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REVISION HISTORY
1/2019—Revision 0: Initial Version
GETTING STARTED
SOFTWARE INSTALLATION PROCEDURES
To install the ACE software and ADF4371 plugin, perform the following steps:
1. Install the latest version of the ACE software platform.
2. If the ADF4371 plugin appears automatically, proceed to Step 4.
3. Double click the ADF4371 plugin file, Board.ADF371.0.1.6.acezip.
4. Check that the ADF4371 plugin appears when the EV-ADF4371SD2Z board is attached through the system demonstration platform (SDP) connector to the PC.

EVALUATION BOARD SETUP PROCEDURES
To run the software, perform the following steps:
1. Select Start > All Programs > Analog Devices > ACE.
2. On the Select Device and Connection tab, choose ADF4371 and the ADF4371 board appears under attached hardware.
3. When connecting the EV-ADF4371SD2Z board, allow 5 sec to 10 sec for the label on the status bar to change.
EVALUATION BOARD HARDWARE

The EV-ADF4371SD2Z requires the SDP-S platform that uses the EVAL-SDP-CS1Z. The SDP-B is not recommended.

The EV-ADF4371SD2Z schematics are shown in Figure 10, Figure 11, Figure 12, and Figure 13. The silkscreens for the evaluation board are shown in Figure 14 and Figure 15.

POWER SUPPLIES

The EV-ADF4371SD2Z board is powered by a 6 V power supply connected to the VSUPPL SMA, or the red banana plug, P2. Connect GND to the black banana plug, P4.

The power supply circuitry has two LT3045, high performance, low noise, and low dropout (LDO) regulators.

One LT3045 is used to generate 5 V to drive the VCO supply pins. The remaining supplies are powered from the other LT3045, which is set to 3.3 V voltage.

Use Switch S1 to switch the 6 V to the board on and off.

RF OUTPUT

The EV-ADF4371SD2Z has three pairs of SMA, 3.5 mm output connectors: RF8P/RF8N, AUX8P/AUX8N, and RF16P/RF16N (differential outputs). The EV-ADF4371SD2Z board has one single 2.92 mm connector, J3, for the RF32P pin. RF32 is also differential, but the RF32N pin is terminated by a 50 Ω on-board resistor.

Because they are sensitive to impedance mismatch, connect the radio frequency (RF) outputs to equal load impedances.

If only one port of a differential pair is used, terminate the complementary port with an equal load terminator (in general, a 50 Ω terminator).

LOOP FILTER

The loop filter schematic is included in the board schematic in Figure 10. Figure 2 shows the loop filter component placement.

The loop filter on the evaluation board is optimized for fractional mode performance with a phase frequency detector (PFD) frequency of 100 MHz and 1.8 mA charge pump current. The values of the loop filter components are as follows:

- Resistors: RCPOUT = 91 Ω, R2 = 400 Ω, R4 = 200 Ω, R15 = 0 Ω
- Capacitors: C20 = 220 pF, C19 = 0.018 μF, C23 = 330 pF

The lowest rms jitter is achieved in integer mode by using a high PFD frequency. This jitter can be tested by using the same filter with a PFD frequency of 200 MHz (enabling the doubler) and 2.4 mA charge pump current. Additional optimization is still possible depending on target frequency and integration limits.

In general, narrower loop filter bandwidths have lower spurious signals. Wide loop filters in integer N mode can achieve <50 fs jitter with very clean reference frequency input (REFin) signals.

ADDITIONAL OPTIMIZATION ON LOOP FILTER

The PLL loop bandwidth can be optimized for different parameters like reference spurs or VCO noise, depending on the system requirements.

Reducing Σ-Δ Modulator (SDM) Noise

In fractional mode, SDM noise becomes apparent and starts to contribute to overall phase noise. This noise can be reduced to insignificant levels by using a series resistor between the CPOUT pin and the loop filter. Place this resistor close to the CPOUT pin. Select a reasonable resistor value that does not affect the loop bandwidth and phase margin of the designed loop filter. In most cases, a 91 Ω resistor value produces the best results. This resistor is not required in integer mode (SDM not enabled) or when a narrow-band loop filter (SDM noise attenuated) is used. This resistor is labeled as RCPOUT in schematics.

Optimizing Spurious Signals

On the evaluation board, the loop filter is placed at the secondary side of the board to create a more compact layout and so that the board is more tolerant to external signals. Using a capacitor on the same side with the ADF4371 (the primary side) results in higher isolation on internally generated spurious signals. For this purpose, a small valued capacitor (10 pF) can be placed close to the VTUNE pin to achieve lower spurious signal levels.

REFERENCE SOURCE

The EV-ADF4371SD2Z board is supplied with a low noise 100 MHz crystal oscillator (XO) from Crystek (CCHD-575-50-100.000).

To use an external single-ended REFIN, connect a low noise reference source to the REFP SMA connector. Remove Resistor R19 (0 Ω) and Resistor R20 (0 Ω) to remove power from the crystal and break the connection to the REFP input.

DEFAULT CONFIGURATION

All components necessary for local oscillator (LO) generation are inserted on the EV-ADF4371SD2Z board. The EV-ADF4371SD2Z board is shipped with 100 MHz XO, the ADF4371 synthesizer with an integrated VCO, and a 180 kHz loop filter (charge pump current (ICP) = 1.8 mA).

DOUBLER AND QUADRUPLER OUTPUT

The ADF4371 contains a frequency doubler and quadrupler to double the 4 GHz to 8 GHz VCO signal on RF16P and RF16N and quadruple the VCO signal on RF32P and RF32N. It is advised to not enable the doubler and quadrupler at the same time.
Figure 3. Evaluation Board Setup Diagram
EVALUATION BOARD SOFTWARE
The ACE software is the main platform that is used to control the EV-ADF4371SD2Z. The ADF4371 plugin includes user interfaces that relate to the ADF4371 and allow evaluation of the device. Use the following steps to open the main control window for ADF4371.

1. Launch the ACE application. With the SDP-S board connected to the EV-ADF4371SD2Z, the attached hardware appears in the graphical user interface (GUI) as shown in Figure 4.
2. Double click the ADF4371 Board icon, and the tab shown in Figure 5 appears.
3. Double click the ADF4371 icon that appears on the board GUI to open the main control window shown in Figure 8.

![Figure 4. ACE Start Page, Attached Hardware (ADF4371 Evaluation Board)](image)
MAIN CONTROLS

The main controls are available in the high level register map shown in Figure 8. To modify registers, perform the following steps:

1. Click **Write All Registers/Initialize** to load all registers and initialize the device.
2. Modify the registers as desired.
3. Click **Apply Changes** to load modified settings to the device. This action loads the updated registers only. All registers can be reloaded using the **Write All Registers/Initialize** button.

QUADRUPLER OUTPUT CONTROLS

For the main, auxiliary, and doubler outputs, the optimal harmonic performance is achieved by using the automatic filter outputs. However, for the quadrupler output, some additional software settings may need to be adjusted to achieve optimal performance.

The settings are available in the **Outputs** section (shown in Figure 6). The output settings include the **Tracking Filter Mux** box that can be set to automatic or manual, the **Quad Bias** box that varies from the lowest setting 0 to the highest of 3, and the **Quad Band Filter** box that varies from 0 to 7.

The bias and filter settings in Table 1 are recommended for quadrupler output.

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>Filter</th>
<th>Bias</th>
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</thead>
<tbody>
<tr>
<td>&lt;18</td>
<td>7</td>
<td>3</td>
</tr>
<tr>
<td>18 to 19</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>19 to 20.5</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>20.5 to 26</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>&gt;26</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 1. Filter and Bias Setting for Quadrupled Output
The recommended settings for quadrupler frequencies from 16 GHz to 18 GHz are shown in Figure 6. The summarized filter performance is shown in Figure 7.

Figure 6. Recommended Quadrupler Filter Settings, 16 GHz to 18 GHz

Figure 7. Aggregated Quadrupler Filter Performance, 3/4 Quadrupler Output and 5/4 Quadrupler Output

Figure 8. Software Front Panel Display, Main Controls
EVALUATION AND TEST

To evaluate and test the performance of the ADF4371, prepare the hardware and software setup as explained in the Evaluation Board Hardware section and the Evaluation Board Software section.

Run the software and set the VCO Frequency Output to 5 GHz. Measure the output spectrum and single sideband phase noise on a spectrum analyzer. Figure 9 shows a phase noise plot of the SMA RF8P pin equal to 5 GHz.
EVALUATION BOARD SCHEMATICS AND ARTWORK

Figure 10. Evaluation Board Schematic, ADF4371 Connections and Loop Filter
Figure 11. Evaluation Board Schematic, 5 V LDO Regulator
Figure 12. Evaluation Board Schematic, 3.3 V LDO Regulator
Figure 13. Evaluation Board Schematic, Board Connector
Figure 15. Evaluation Board Silk Screen, Bottom Side
Figure 17: Evaluation Board Layer 2, Ground
Figure 19. Evaluation Board Layer 4, Secondary
## ORDERING INFORMATION

### BILL OF MATERIALS

Table 2. Reference Designator Description Value Manufacturer Part Number

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>Description</th>
<th>Value</th>
<th>Manufacturer</th>
<th>Part Number</th>
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<tr>
<td>AUX8N, AUX9N, RF8P,</td>
<td>Printed circuit boards (PCBs), SMA, right angle jack connectors</td>
<td>32K243-</td>
<td>Rosenberger</td>
<td>32K243-40ML5</td>
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<tr>
<td>RF16N, RF16P</td>
<td>Capacitors, ceramic, X6S</td>
<td>1 μF</td>
<td>TDK</td>
<td>C1005X6S1C105K050BC</td>
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<td>C1, C3, C8, C9, C12,</td>
<td>Ceramic capacitors, C0G (NP0), general-purpose</td>
<td>10 pF</td>
<td>Murata</td>
<td>GRM0335C1E100JA01D</td>
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<tr>
<td>C17, C24</td>
<td>Ceramic capacitors, X5R, general-purpose</td>
<td>10 μF</td>
<td>Murata</td>
<td>GRM21BR61C106KE15L</td>
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<td>C10, C11, C28, C29,</td>
<td>Ceramic capacitors, X7R, general-purpose</td>
<td>0.01 μF</td>
<td>Murata</td>
<td>GRM155R71E103KA01D</td>
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<td>C30, C35</td>
<td>Ceramic capacitors, X5R, general-purpose</td>
<td>4.7 μF</td>
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<td>GRM21BR61E475KA12L</td>
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<td>06033C183JAT2A</td>
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<td>C1608CG1H221J</td>
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<td>Ceramic capacitors, X7R, general-purpose</td>
<td>330 pF</td>
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<td>CG13E3CG2D331J080AA</td>
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<tr>
<td>C18, C25</td>
<td>Multilayer ceramic capacitors (MLCCs), NP0, RF and microwave</td>
<td>10 pF</td>
<td>American Technical Ceramics</td>
<td>400Z100FT16T</td>
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<td>C19</td>
<td>Ceramic capacitors, C0G (NP0), general-purpose</td>
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<td>Murata</td>
<td>GRM1555C1H102JA01</td>
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<td>AVX</td>
<td>TJC226M025R0100</td>
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<td>C39, C41, C42</td>
<td>PCB test point connectors</td>
<td>Yellow</td>
<td>Components Corporation</td>
<td>TP-104-01-04</td>
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<td>AVX</td>
<td>TJC226M025R0100</td>
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<td>SDIO, TP2</td>
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<td>80 Ω at 100 MHz</td>
<td>Murata</td>
<td>BLM15PX800SN1D</td>
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<td>CV37</td>
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<td>142-0701-801</td>
<td>Cinch Connectivity Solutions</td>
<td>142-0701-801</td>
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<td>E1</td>
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<td>42K243-40M</td>
<td>Rosenberger</td>
<td>02K243-40M</td>
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<tr>
<td>J1, J4, REFP, VSUPPL,</td>
<td>PCB, vertical type receptacle, surface-mount device (SMD) connector</td>
<td>7.4 nH</td>
<td>Coilcraft</td>
<td>0302CS-7N4XJLU</td>
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<td>VTUNE</td>
<td>PCB, single socket connector</td>
<td>Red</td>
<td>Hirose</td>
<td>FXB-120S-SV(21)</td>
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<td>J3</td>
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<td>Black</td>
<td>Deltron</td>
<td>571-0100</td>
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<td>L1, L2, L3, L4</td>
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<td>Multicomp</td>
<td>MC0625W040210R</td>
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<td>R1, R7, R9, R11, R14,</td>
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<td>33.2 kΩ</td>
<td>Vishay</td>
<td>CRCW040233K2FKED</td>
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<td>MC0633GW00000T5E-TC</td>
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<tr>
<td>R20, R32</td>
<td>Precision, thin film, chip resistor</td>
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<td>Vishay</td>
<td>PAT0603E4000BST1</td>
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<td>R2</td>
<td>High frequency, thin film, chip resistor</td>
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<td>FC0402E1008BST1</td>
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<td>R5</td>
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<td>100 kΩ</td>
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<td>R6</td>
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<td>RC0603FR-0791RL</td>
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<td>R74, R79</td>
<td>Single-pole single-throw, momentary switch</td>
<td>91 Ω</td>
<td>Yageo</td>
<td>TT11AGPC104</td>
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<td>RCP OUT</td>
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<td>Keystone Electronics</td>
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<td>PCB test point connectors</td>
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<td>TP3, TP5</td>
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<td>TP4</td>
<td>PCB test point connector</td>
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