

Evaluating the **HMC7044** Dual Loop Clock Jitter Cleaner

FEATURES

- Simple power connection using USB connection and on-board LDO voltage regulators
- LDOs can be bypassed for power measurements
- AC-coupled differential SMA connectors
- SMA connectors for
 - 2 reference Inputs
 - 6 clock outputs
 - 1 VCXO output
- Microsoft Windows®-based evaluation software with simple graphical user interface
- On-board PLL loop filter
- Easy access to digital input/output and diagnostic signals via input/output header (4 GPIOs)
- Status LEDs for diagnostic signals
- USB computer interface

EVALUATION KIT CONTENTS

- EV3HMC7044LP10B** evaluation board
- USB interface board and USB cable
- EK1HMC7044LP10B** user guide

GENERAL DESCRIPTION

This user guide describe the hardware and software of the **HMC7044** evaluation kit. The evaluation board schematic and printed circuit board (PCB) layout artwork can be found on the **EK1HMC7044LP10B** product page at www.analog.com.

The **HMC7044** meets the requirements of multicarrier GSM and LTE base station designs and offers a wide range of clock management and distribution features to simplify baseband and radio card clock tree designs. The high performance dual-loop core of the **HMC7044** enables the base station designer to attenuate the incoming jitter of a primary system reference clock, such as a CPRI source, with the help of the narrow-band configured first PLL loop, which disciplines an external VCXO, and to generate the low phase noise, high frequency clocks with the wider-band second PLL to drive data converter sample clock inputs.

The **EV3HMC7044LP10B** evaluation board is a compact, easy to use platform for evaluating all the features of the **HMC7044**. A 122.88 MHz VCXO is mounted on the evaluation board to provide a complete solution. All inputs and outputs are configured as differential on the evaluation board.

Full specifications on the **HMC7044** are available in the product data sheet, which should be consulted in conjunction with this user guide when working with the evaluation board.

EVALUATION BOARD PHOTOGRAPH

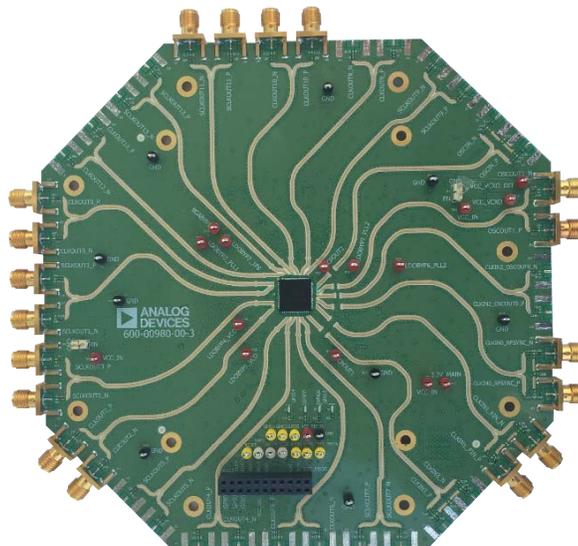


Figure 1.

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REVISION HISTORY

9/15—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The following instructions are for setting up the physical connections to the [EV3HMC7044LP10B](#) evaluation board.

CHECKING JUMPER CONNECTIONS

Remove all jumpers (JP2 and JP3).

SETTING UP THE POWER AND PC CONNECTIONS

Set up the power and PC connections as follows:

1. Install the [HMC7044](#) evaluation software before connecting the evaluation board to the PC for the first time (see the Installing the Software section). Administrative privileges are required for the installation.
2. Connect a 5 V supply voltage to Test Point TP38 of the evaluation board.
3. Connect the USB interface board to the evaluation board, as shown in Figure 2.
4. Connect the USB cable to the USB interface and the PC.
5. The **Found New Hardware Wizard** automatically appears when the USB interface is connected. Select **Install the software automatically** and then click **Next**.
6. The **Found New Hardware Wizard** may appear twice during the installation.

See the Evaluation Board Software section for details on running the [HMC7044](#) board software.

SETTING UP THE SIGNAL CONNECTIONS

After setting up the power and PC connections, use the following procedure to set up signal connections:

1. Connect a signal generator to the CLKIN0_RFSYNC_P SMA Connector J11. By default, the reference inputs on the evaluation board are ac-coupled. Terminate the CLKIN0_RFSYNC_N SMA Connector J10 with a 50 Ω termination. An amplitude setting of 6 dBm from the signal generator is sufficient.
2. Connect an oscilloscope, spectrum analyzer, or other lab equipment to any output of the CLKOUTx_P or CLKOUTx_N SMA connectors. Place a 50 Ω termination on all unused differential output pairs.

BYPASSING THE 5 V LDO POWER SUPPLY

The evaluation board contains three on-board, low dropout regulators (LDOs) to regulate 5 V to 3.3 V supply domain. The evaluation board can be configured to bypass linear regulators, which is useful for measuring [HMC7044](#) power consumption. See the evaluation board schematics provided on the [EK1HMC7044LP10B](#) product page at www.analog.com.

Bypass the 5 V two on-board LDOs for the [HMC7044](#) as follows:

1. Remove the on-board LDOs (U2 and U4).
2. Populate R241, FB10, C105, C154, and C159 for VCC1_VCO.
3. Remove R245 and FB20.
4. Populate R12 (to isolate the SPI interface board current consumption from the [HMC7044](#)).

Connect a bench 3.3 V power supply to each of the supply pins on the 3.3 V main header (TP15).

Note that it is very important to not have the 5 V supply connected to TP15 of the evaluation board.

Connect a bench 5.0 V power supply to TP38 for the on-board LDO of the VCXO supply, VCC_VCXO.

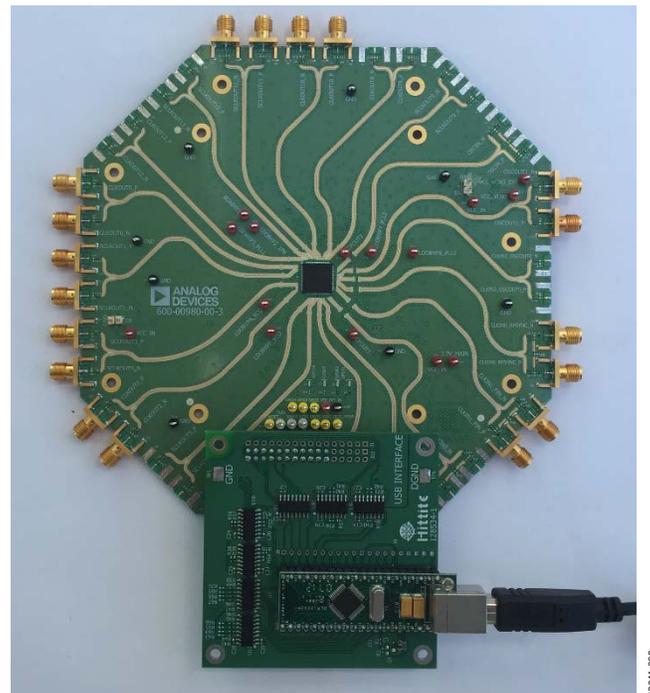


Figure 2. [HMC7044](#) Evaluation Kit Setup

EVALUATION BOARD SOFTWARE SETUP

Follow the instructions included in this section to set up the [HMC7044](#) evaluation software.

INSTALLING THE SOFTWARE

Do not connect the evaluation board until the software installation is completed.

1. Download the installer from [HMC7044](#) product page at www.analog.com.
2. Double-click **setup.exe** from the installer file. Follow the installation instructions. The default location for the evaluation software is **C:\Program Files (x86)\Analog Devices\Jitter Attenuator**.
3. After the installation completes, the user is prompted to install the drivers for the USB interface.

STARTING THE SOFTWARE

After the evaluation software is installed, run the software as follows:

1. Power up and connect the evaluation board to the PC.
2. Double-click **HMC7044 GUI** to run the [HMC7044](#) evaluation software.
3. If the evaluation board was found, the main window of the evaluation board software appears directly. Proceed to the Evaluation Board Software Operation section for more details about using the software.
4. If the evaluation board was not found, a dialog box appears to select either [HMC7044](#) offline mode or [HMC7043](#) offline mode (see Figure 4). Offline mode is useful for viewing and generating register setup files.



Figure 3. Select USB Device Window—Evaluation Board Not Found (Offline Mode)

5. If multiple [HMC7044](#) evaluation boards are connected to the same PC, a hardware selection dialog box appears (see Figure 4). The text in this window is either a serial number, **OFFLINE HMC7044**, or **OFFLINE HMC7043**. Select the serial number and click **OK**.

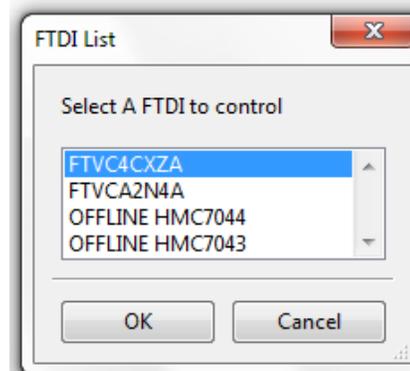


Figure 4. Select USB Device Window—Multiple Evaluation Boards Found

6. If the evaluation software cannot detect the evaluation board, restart the power supply and connect/disconnect the USB cable.

EVALUATION BOARD SOFTWARE OPERATION

The main window of the [HMC7044](#) evaluation board software comprises seven subsection tabs that correspond to the major functional blocks of the [HMC7044](#) (see Figure 7). These subsections, most of which have their own tab, are outlined in this section. From the main window, the tab for each functional block can be accessed by clicking the appropriate tab.

The [HMC7044](#) evaluation software directly communicates with the [HMC7044](#). When a widget value is changed, the new value is written to the register instantly.

MENU BAR OF MAIN WINDOW

File Menu

The **File** menu allows the user to load a previously saved [HMC7044](#) configuration file or to save a new [HMC7044](#) setup file. A setup file (.py) is a text file that contains the [HMC7044](#) register configuration file.

To load a previously saved configuration file, select **Load Config** from the **File** menu. Alternatively, to save a new configuration file, select **Save Config** from the **File** menu.

The toolbar also offers shortcuts for **Save Config** and **Load Config**.



Figure 5. **Save Config** Shortcut



Figure 6. **Load Config** Shortcut

To exit the evaluation software, select **Exit** from the **File** menu. Note that saving the current state helps to continue the setup in the future. However, the user must save the setup before exiting; the software does not automatically check to ensure that the existing setup is saved.

View Menu

The **Log** window, accessed by selecting **Log Window** from the **View** menu, allows the user to follow every read or write actions in the GUI.

Help Menu

Selecting **Help** from the **Help** menu opens the **About** window, which contains information such as the revision number, region information, and contact information.

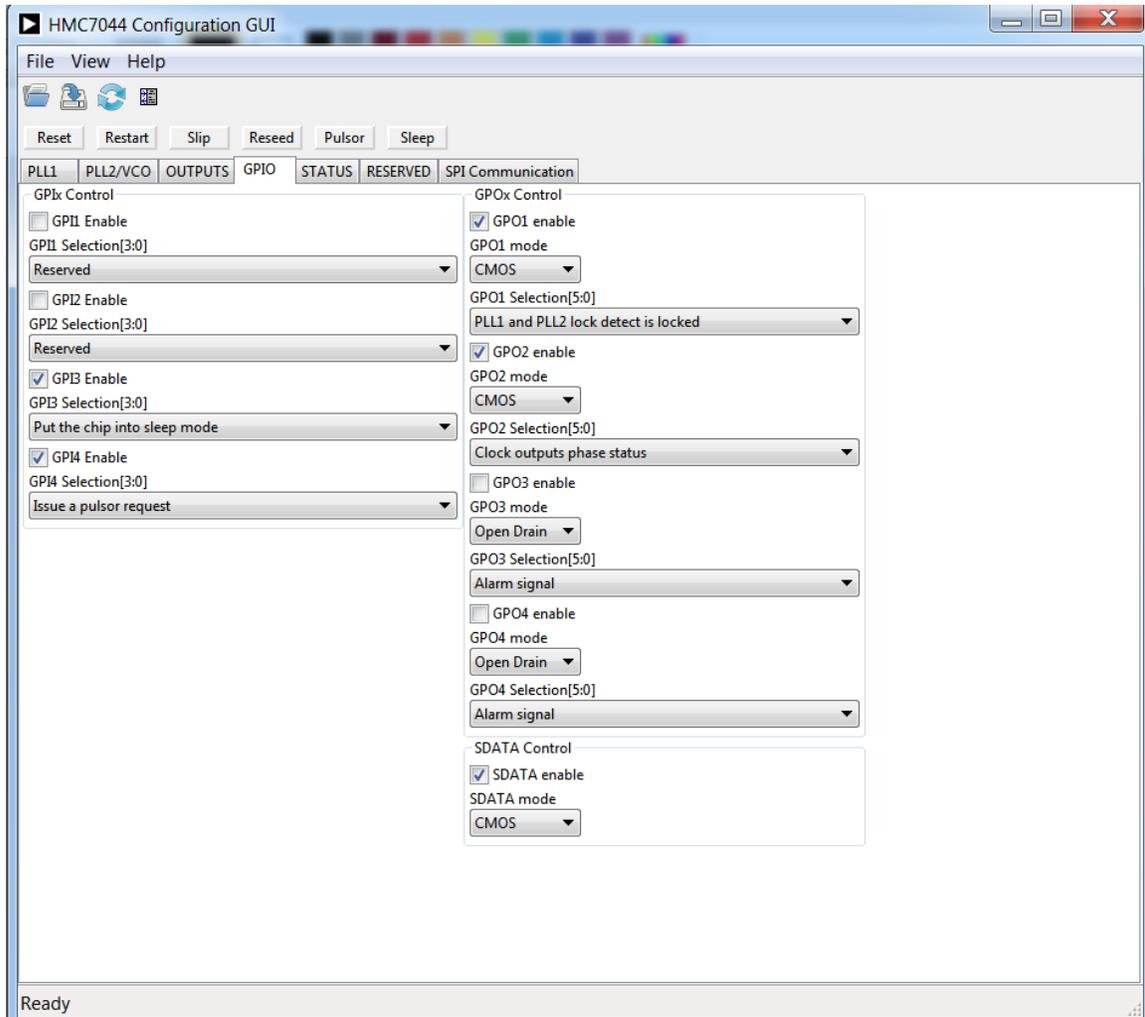


Figure 7. **GPIO** Tab of [HMC7044](#) Evaluation Software GUI

USING THE SOFTWARE TO CONTROL THE FUNCTIONAL BLOCKS OF THE HMC7044

Register W/R

The update icon issues a GUI update command by reading all registers and setting every widget according to read values.



Figure 8. Update Icon

GPIO Controls

The GPIO tab allows the user to control general-purpose input/output to monitor the alarms/status indicators to determine the health of the system.

Four GPIO configurations can be controlled from this tab (see Figure 7).

PLL1 Controls

The PLL1 tab in the main window (see Figure 9) allows the user to configure the PLL1 parameters.

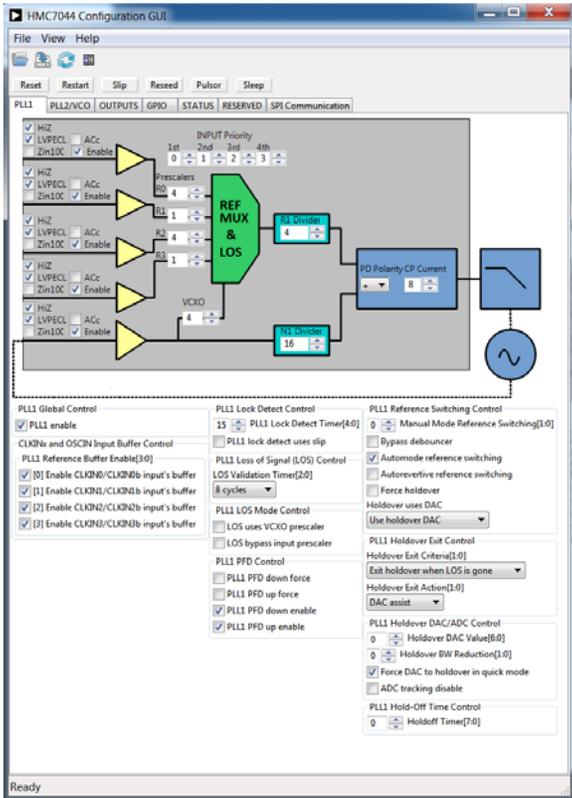


Figure 9. PLL1 Tab of HMC7044 Evaluation Software GUI

The PLL1 input buffer controls are located on the left side of the PLL1 tab (see Figure 10). Enable/disable, termination type, ac coupling, and dc coupling options can be controlled.

The PLL1 input/VCXO prescalers are shown in Figure 11. Divide ratios of these five prescalers are controllable from this section. The priority table of PLL1 references are also located in the INPUT Priority section of this tab.

The PLL1 reference and feedback divider ratios, PFD polarity, and charge pump current setting controls are shown in Figure 12.

Additional control bits of PLL1 are located at the bottom of the PLL1 tab, as shown in Figure 13. See the HMC7044 datasheet for further details on these bits.

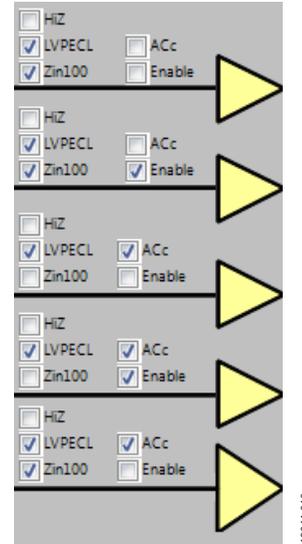


Figure 10. PLL1 Input Buffers

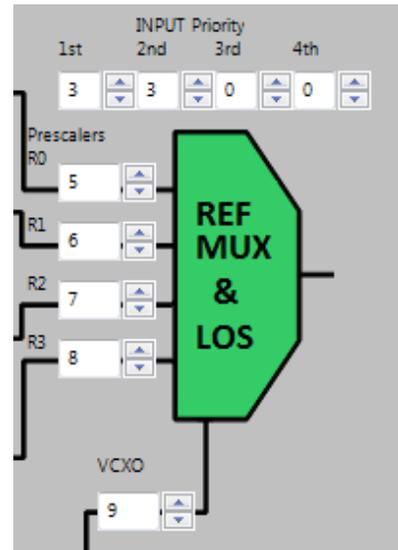


Figure 11. PLL1 Input/VCXO Prescalers and Reference MUX

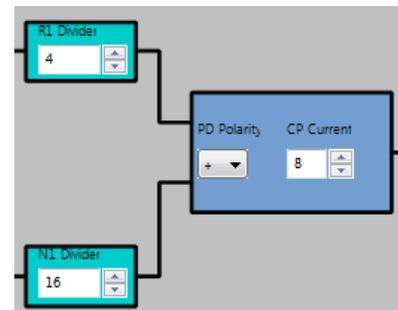


Figure 12. PLL1 Reference and Feedback Divider and Charge Pump

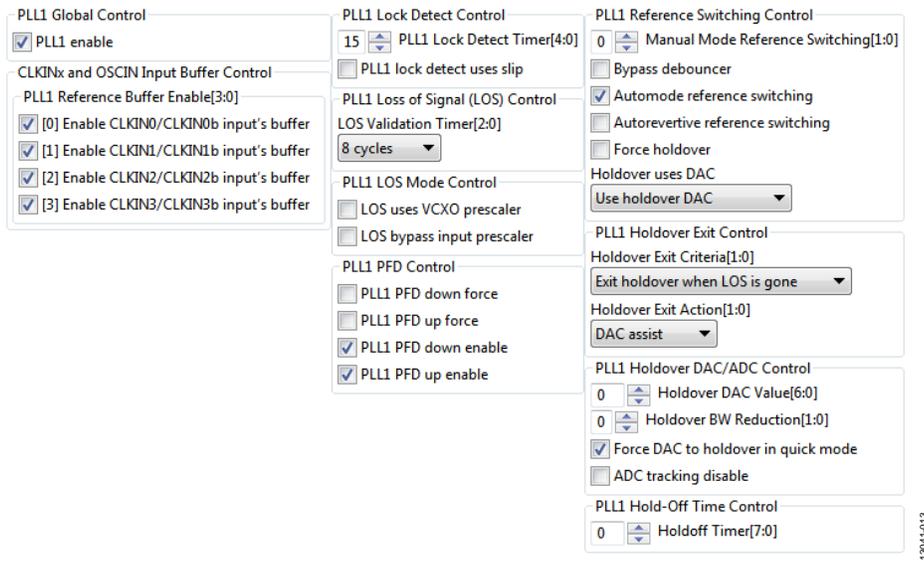


Figure 13. PLL1 Additional Control Bits

PLL 2 CONTROLS

The PLL 2 tab in the main window (see Figure 14) allows the user to configure the PLL2 parameters.

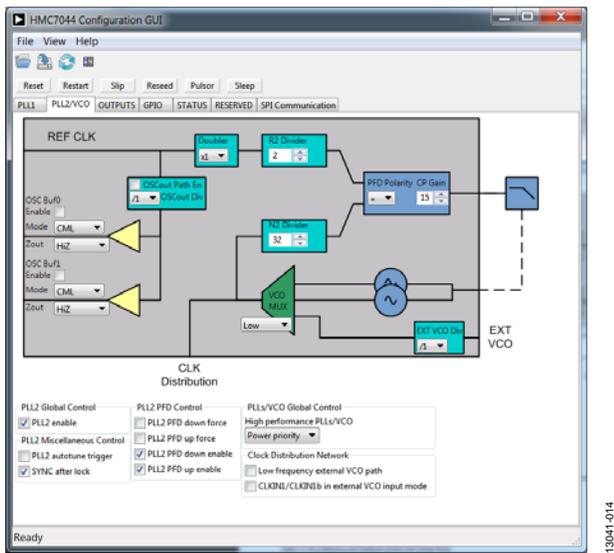


Figure 14. PLL2 Tab of HMC7044 Evaluation Software GUI

The PLL2 reference and feedback divider ratios, PFD polarity, and charge pump current setting controls are shown in Figure 15.

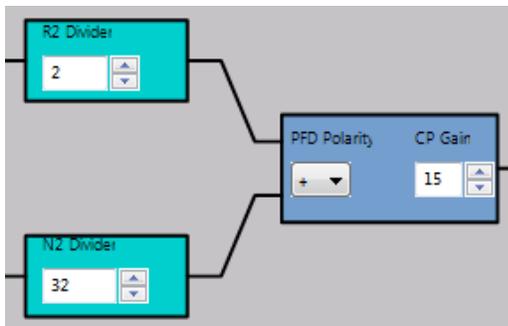


Figure 15. PLL2 Reference and Feedback Divider and Charge Pump

The PLL2 VCO MUX for selecting internal or external VCO is shown in Figure 16.

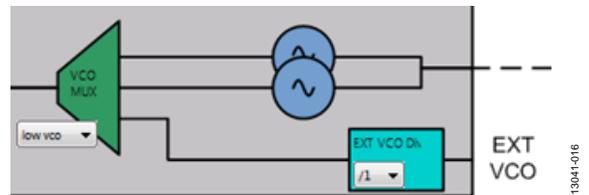


Figure 16. PLL2 Internal External VCO selection

The PLL2 input/OSCOUTx/OSCOUTx divider is shown in Figure 17. The divide ratio of these outputs are controllable from this section.

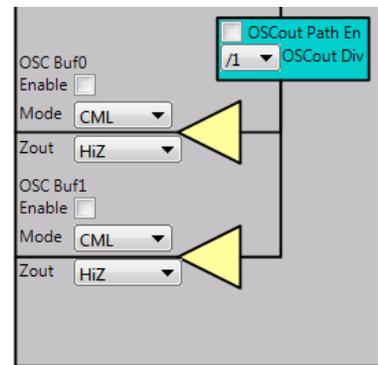


Figure 17. OSCOUTx/OSCOUTx Path

Additional control bits of the PLL2 are located at the bottom of the PLL2 tab, as shown in Figure 18. See the HMC7044 data sheet for further details on these bits.

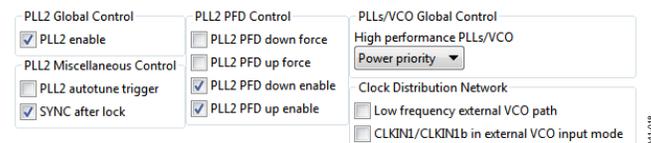


Figure 18. PLL2 Additional Control Bits

OUTPUT CHANNEL CONTROLS

The channel divider controls shown in Figure 19 are accessed via the **OUTPUTS** tab. It is usually sufficient to change only the divide ratio, because the evaluation software and the **HMC7044** output duty cycle remains at 50%.

The phase offset can be varied by three different methods, as shown in Figure 20. Two of them are based on digital delay. One is slip-based delay, which provides unlimited one full VCO cycle delay. To perform slip, channel multislip mask be checked, as shown in Figure 20. Enter the number of VCO cycle value, and click **Slip**.

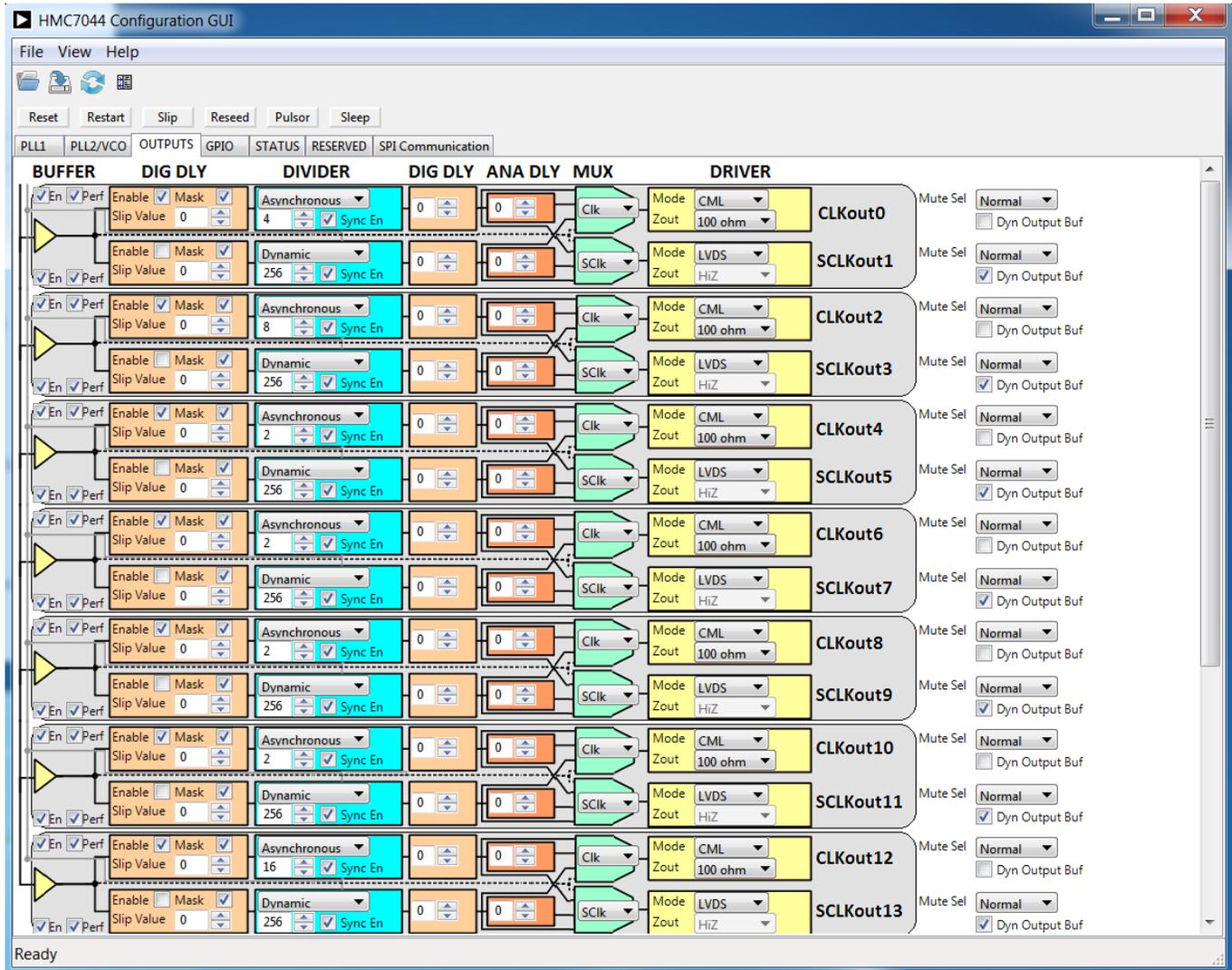


Figure 19. Output Clock Driver Tab of HMC7044 Evaluation Software GUI

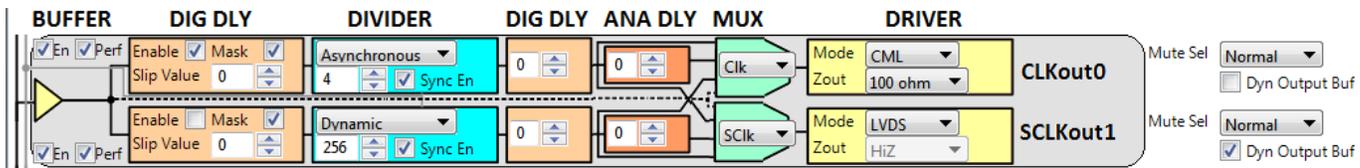


Figure 20. Example Output Channel—Configurable Blocks

The output termination selection shown in Figure 21 is accessed by clicking any of the drop-down lists under **DRIVER** in the **OUTPUTS** tab (see Figure 19). It is important to power down unused outputs on the evaluation board because they can be a major source of unwanted spurs.

Even numbered outputs (CLKOUTx/CLKOUTx pins) are ac-coupled with 150 Ω to ground for each leg on the board by default. Odd numbered outputs (SCLKOUTx/SCLKOUTx pins) are ac-coupled with 100 Ω to VCC internally; no termination resistors are on the board by default. This termination scheme is

ideal for CML drivers. However, this scheme degrades the CMOS driver performance. Improved CMOS driver performance is achieved by removing the termination resistors. For LVDS drivers, differential 100 Ω resistor must be populated on the board.

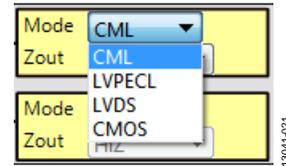


Figure 21. Output Termination Selection

QUICK START GUIDE TO THE HMC7044

The HMC7044 can be initialized from SPI settings.

To load the provided configuration file, do the following:

1. Follow the instructions provided in the Evaluation Board Software Setup section.
2. Connect a signal generator to the CLKIN0_RFSYNC_P SMA Connector J11. By default, the reference inputs on the evaluation board are ac-coupled. Terminate the CLKIN0_RFSYNC_N SMA Connector J10 with a 50 Ω termination. An amplitude setting of 6 dBm from a signal generator is sufficient, and the frequency must be 122.88 MHz.
3. Connect a 5 V supply voltage to Test Point TP38 of the evaluation board.
4. Provided with the installer is a setup file named **HMC7044_983MHz_122p88MHz_VCXO_DoublerON.py**, located in the **Configuration Files** directory. Load this configuration file from the **File** menu in the main software window.
5. Click **Restart**.
6. Connect an oscilloscope, spectrum analyzer, or other lab equipment to any output of the CLKOUTx_P or CLKOUTx_N SMA connectors. Place a 50 Ω termination on all unused differential output pairs.



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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