
ADV7511

**Low-Power HDMI® Transmitter
with Audio Return Channel**

HARDWARE USER'S GUIDE

- Revision D -

July 2011

REVISION HISTORY

2/10Rev 0

5/10 Rev A

Section	Change Description
	Throughout document S/PDIF to SPDIF for consistency
Section 4:	Table 1 – under DIGITAL OUTPUTS, listed SPDIF_OUT referenced to 3.3V MVDD
Section 5:	Figure 6 - Changed DVDD_3V to MVDD
Section 5:	Table 3 – Add description to SPDIF_OUT showing it to be 3.3V logic
Section 6.1.3	Edited to add mention of AES3 support
Section 6.1.3.3	Expanded description of MCLK internal generation
Section 6.2.1	Edited to indicate that SPDIF_OUT is 3.3V logic level.
Section 6.8	Moved Power Supply Domain figure to this section. Edited description to add PVDD, BGVDD and PLVDD.
Section 6.8.2	Edited to explain SPDIF high power and low power
Section 7.4, Section 7.5	Added text to show that both pins require pull up.
Section 7.7	Figure 26 – edited to correct CEC pin name.

Rev B 8/10

Section	Change Description
Front page	Add ® after HDMI; remove reference to HDMI revision
Last page	Add statement regarding I2C, Philips, NXT and HDMI

Rev C 3/11

Section	Change Description
All document	Removed ADI Confidential reference
Table 1	Added footnote to setup and hold times

Rev D 7/11

Section	Change Description
Figure 19	Corrected Mux select bit table

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SECTION 1: INTRODUCTION

1.1 Scope and Organization

This document is intended to help the hardware designer understand what is necessary to design for the ADV7511 and maintain the highest levels of performance. The *ADV7511 Hardware User's Guide* (HUG) provides guidelines to design the schematics and board layout. Included are sections on the 100-lead LQFP package and an overview of the functional blocks (including a brief description for each block) to provide an understanding of the ADV7511 functional and performance capabilities. The *ADV7511 Programming Guide* (PG) is available as a separate document and should be used to gain a complete understanding on how to configure the ADV7511 within a system application.

It is divided into the following sections:

[Section 2: Reference Documents](#) is a list of other references, which will be helpful when designing with the ADV7511 HDMI Transmitter.

[Section 3: Block Diagram](#) gives an overall functional view of the HDMI transmitter.

[Section 4: Specifications](#) give all pertinent data such as: timing, power and testing.

[Section 5: Pin and Package Information](#) give the mechanical details of the interface.

[Section 6: Functional Description](#) serves to elaborate on input, output and internal operations.

[Section 7: PCB Layout Recommendations](#) are an aid to low noise operation.

1.1.1 Links

There are many links in this document to help with navigation. Use a mouse click to follow a link, and use the Alt key + left arrow key to return. Active links can be identified by the dotted blue underline.

1.1.2 Symbols

Symbols are used to indicate internal and external document references as follows:

- ▶ Indicates a linked reference to another section of this document.
- ▷ Indicates a reference to another document, either an ADI document or an external specification.

1.1.3 Format Standards

In this document, ADI has chosen to represent data in the following ways:

- 0xNN** Hexadecimal (base-16) numbers are represented using the “C” language notation, preceded by 0x.
- 0bNN** Binary (base-2) numbers are represented using “C” language notation, preceded by 0b.
- NN** Decimal (base-10) numbers are represented using no additional prefixes or suffixes.
- Bit** Bits are numbered in little-endian format; i.e., the least-significant bit of a byte or word is referred to as bit 0.

1.2 Overview

The ADV7511 is a high speed High Definition Multimedia Interface (HDMI) transmitter that is capable of supporting an input data rate up to 165MHz (1080p @ 60Hz, UXGA @ 60Hz) and an output data rate up to 225MHz. Deep Color to 36 bits per pixel is supported to 1080p at 60Hz. Careful hardware design (schematics and PCB layout) is recommended to optimize the performance and to ensure HDMI compliance.

▸ The *ADV7511 Programming Guide* and *ADV7511 Software Driver User Guide* are also available if required.

1.3 Hardware Features

- HDMI v1.4 features supported
 - HEAC (ARC)
 - 3D video
 - Advanced Colorimetry
 - sYCC601
 - Adobe RGB
 - Adobe YCC601
- Supports Deep Color
- Operation up to 225MHz (TMDS link frequency)
- Integrated CEC support with 3 message buffers
- Supports x.v.Color™ (Gamut Metadata)
- Internal HDCP key storage
- Interrupt (INT) output pin eliminates constant I2C monitoring
- Supports I2S, SPDIF, DSD, DST and HBR audio input formats
- No audio Master Clock (MCLK) required for SPDIF
- Requires 1.8V and 3.3V supply
- EDID buffered on chip
- Color Space Converter (CSC) with video range clipping
- 100-lead LQFP package
- 0°C to +70°C temperature range

1.4 Supported Input Formats

- 36, 30, or 24 bit RGB 4:4:4 (separate syncs)
- 36, 30, or 24 bit YCbCr 4:4:4 (separate syncs)
- 24, 20, or 16 bit YCbCr 4:2:2 (embedded or separate syncs)
- 12, 10, or 8 bit YCbCr 4:2:2 (2x pixel clock with embedded or separate syncs)
- 12, 10, or 8 bit YCbCr 4:2:2 (DDR with embedded or separate syncs)
- 12 bit RGB 4:4:4 (DDR with separate syncs)
- 12 bit YCbCr 4:4:4 (DDR with separate syncs)

1.5 Supported Output Formats

- 36, 30, or 24 bit RGB 4:4:4
- 36, 30, or 24 bit YCbCr 4:4:4
- 24 bit YCbCr 4:2:2

SECTION 2: REFERENCE DOCUMENTS

2.1 ADI Documents

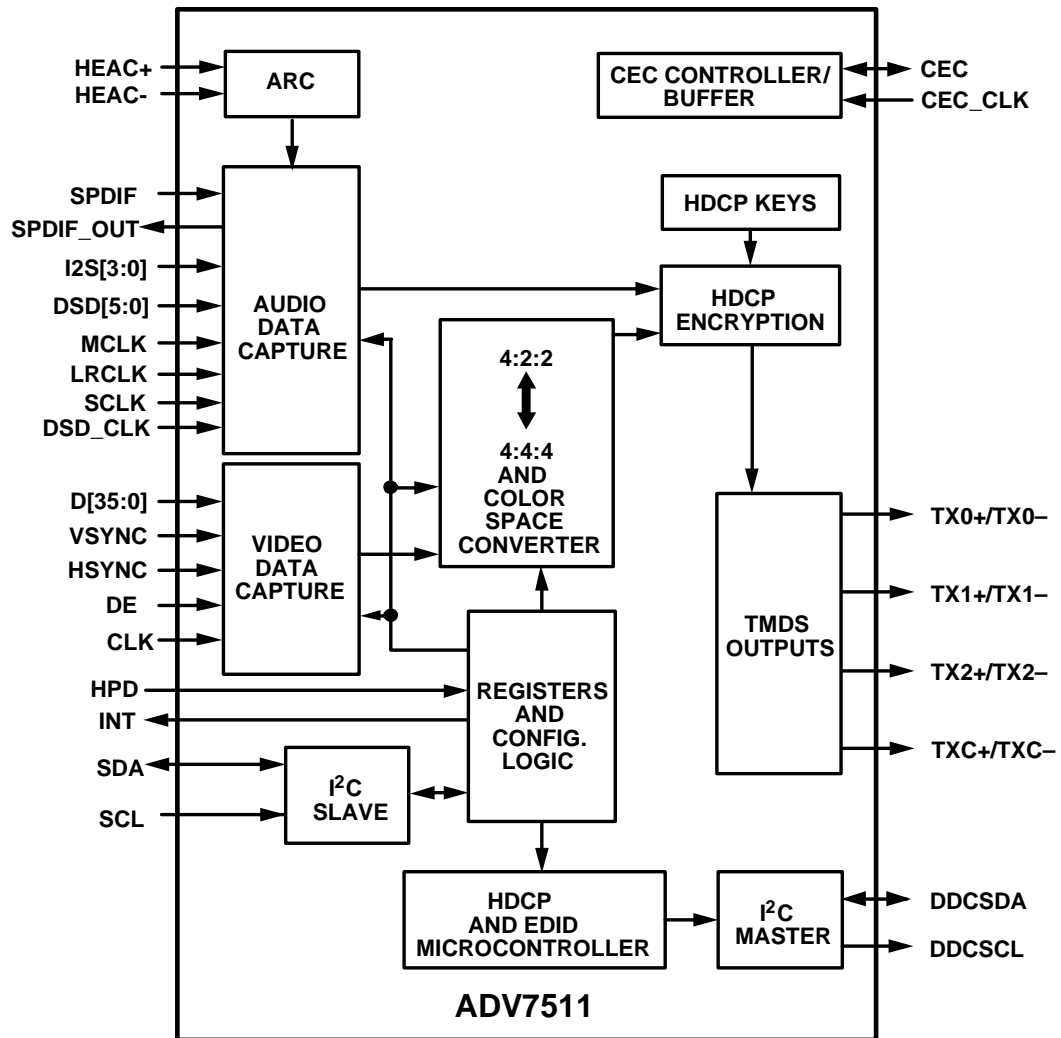
- ADV7511 Data Sheet
- ADV7511 Programming Guide
- AN-810 - EDID/HDCP Controller Application Note

2.2 Industry Specifications

- EIA/CEA-861-E
- HDMI Specification 1.4
- HDCP 1.4

SECTION 3: BLOCK DIAGRAM

Figure 1 ADV7511 Functional Block Diagram



SECTION 4: SPECIFICATIONS

Table 1 Electrical Specifications

Parameter	Conditions	ADV7511KSTZ/ADV7511KSTZ-P					
		Temp	Test Level ¹	Min	Typ	Max	Unit
DIGITAL INPUTS							
Data Inputs – Video, Audio and CEC_CLK							
Input Voltage, High (V _{IH})		Full	VI	1.35		3.5	V
Input Voltage, Low (V _{IL})		Full	VI	-0.3		0.7	V
Input Capacitance		25°C	VIII		1.0	1.5	pF
I2C Lines (DDCSDA, DDCSCL, SDA, SCL)							
Input Voltage, High (V _{IH})		Full	VI	1.19		5.5	V
Input Voltage, Low (V _{IL})		Full	VI	-0.3		0.8	V
CEC							
Input Voltage, High (V _{IH})		Full	VI	2.0			V
Input Voltage, Low (V _{IL})		Full	VI			0.8	V
Output Voltage, High (V _{IH})		Full	VI	2.5		3.63	V
Output Voltage, Low (V _{IL})		Full	VI	-0.3		0.6	V
HPD							
Input Voltage, High (V _{IH})		Full	VI	1.3		5.5	V
Input Voltage, Low (V _{IL})		Full	VI	-0.3		0.8	V
DIGITAL OUTPUTS							
SPDIF_OUT							
Output Voltage, High (V _{OH})	Load = 5pF	Full	VI	0.8*MVdd			V
Output Voltage, Low (V _{OL})	Load = 5pF	Full	VI			0.2*MVdd	V
THERMAL CHARACTERISTICS							
Thermal Resistance							
θ _{JC} Junction-to-Case		Full	V		20		°C/W
θ _{JA} Junction-to-Ambient		Full	V		43		°C/W
Ambient Temperature		Full	V	0	+25	+70	°C
DC SPECIFICATIONS							
Input Leakage Current, I _{IL}		25°C	VI	-1		+1	μA
POWER SUPPLY							
1.8V Supply Voltage (DVdd, AVdd, PVdd, PLVdd, BGVdd)		Full	IV	1.71	1.8	1.90	V
1.8V Supply Voltage Noise Limit							
DVdd – HDMI Digital Core		Full	V			64	mV RMS
AVdd – HDMI Analog Core	Refer to ►Section 7.1	Full	V				mV RMS
PLVdd – HDMI PLL – Analog	Refer to ►Section 7.1	Full	V				mV RMS
PVdd – HDMI PLL - Digital		Full	V			64	mV RMS
BGVdd - Band-gap		Full	V			64	mV RMS
3.3V Supply Voltage (MVdd)		Full		3.15	3.3	3.45	V
Power-Down Current – level 1	Refer to the ADV7511 Programming Guide	25°C	IV			20	mA
Power-Down Current – level 2	Refer to the ADV7511 Programming Guide	25°C	IV			300	μA

Parameter	Conditions	ADV7511KSTZ/ADV7511KSTZ-P					
		Temp	Test Level ¹	Min	Typ	Max	Unit
Transmitter Total Power 1.8V power = 325mW 3.3V power = 1mW	1080p, 36 bit, typical random pattern	Full	VI			326	mW
AC SPECIFICATIONS							
TMD5 Output Clock Frequency		25°C	IV	20		225	MHz
TMD5 Output Clock Duty Cycle		25°C	IV	48		52	%
Input Video Clock Frequency		Full				165	MHz
Input Video Data Setup Time – t_{VSU}^2		Full	IV	1			nS
Input Video Data Hold Time – t_{VHLD}^2		Full	IV	0.7			nS
TMD5 Differential Swing		25°C	VII	800	1000	1200	mV
Differential Output Timing							
Low-to-High Transition Time		25°C	VII	75	95		pS
High-to-Low Transition Time		25°C	VII	75	95		pS
V _{SYNC} and H _{SYNC} Delay from DE Falling Edge		25°C	IV		1		UI ³
V _{SYNC} and H _{SYNC} Delay to DE Rising Edge		25°C	IV		1		UI
AUDIO AC TIMING (see ► Figure 3 to ► Figure 5)							
SCLK Duty Cycle See ► Table 18							
When N/2 = even number		Full	IV	40	50	60	%
When N/2 = odd number		Full	IV	49	50	51	%
I ² S[3:0], SPDIF, DSD[5:0] Setup – t_{ASU}		Full	IV	2			nS
I ² S[3:0], SPDIF, DSD[5:0] Hold Time – $t_{AHL D}$		Full	IV	2			nS
LRCLK Setup Time – t_{ASU}		Full	IV	2			nS
LRCLK Hold Time – $t_{AHL D}$		Full	IV	2			nS
CEC							
CEC_CLK Frequency		Full	VIII	3	12 ⁴	100	MHz
CEC_CLK Accuracy		Full	VIII	-2		+2	%
I2C Interface (see ► Figure 21)							
SCL Clock Frequency		Full				400	kHz
SDA Setup Time – t_{DSU}		Full		100			nS
SDA Hold Time – t_{DHO}		Full		100			nS
Setup for Start – t_{STASU}		Full		0.6			uS
Hold Time for Start – t_{STAH}		Full		0.6			uS
Setup for Stop – t_{STOSU}		Full		0.6			uS

1. See Explanation of Test Levels section.
2. Measured at 0.9V. Setup and hold times can be altered by +/-1.2ns in 400ps steps.
3. UI = unit interval.
4. 12MHz crystal oscillator for default register settings.
I2C data rates of 100KHz and 400KHz supported.

Figure 2 Timing for Video Data Interface

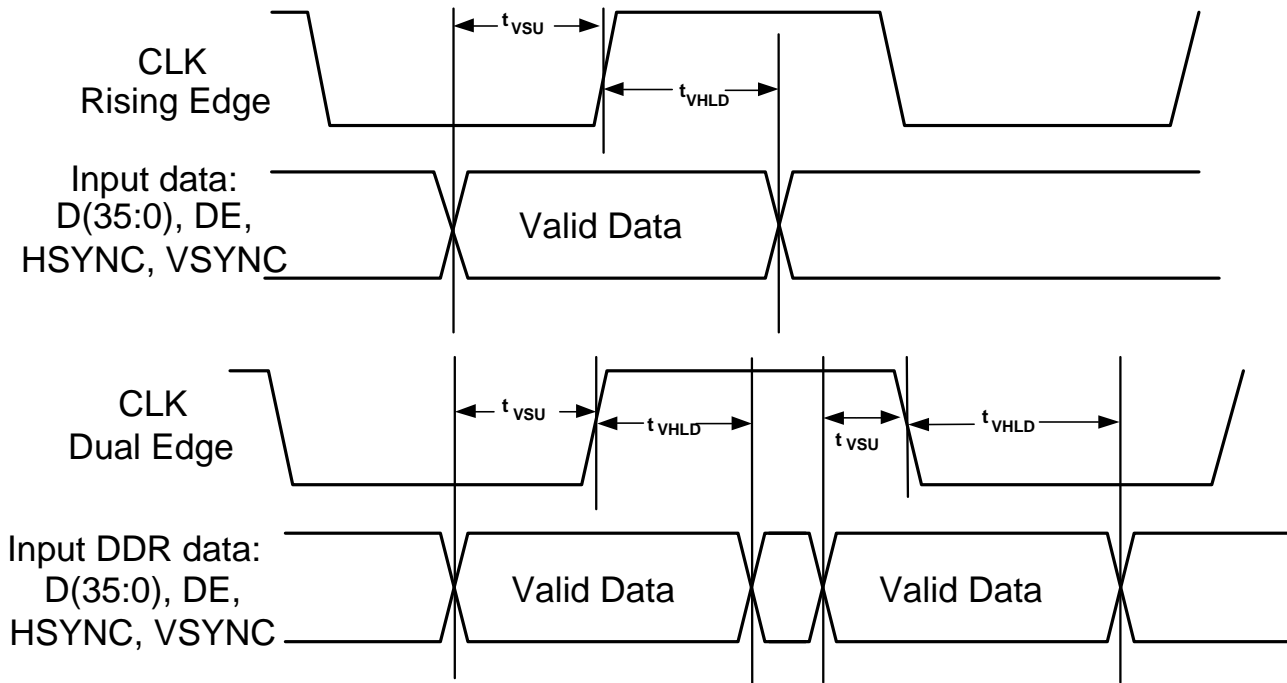


Figure 3 Timing for I2S Audio Interface

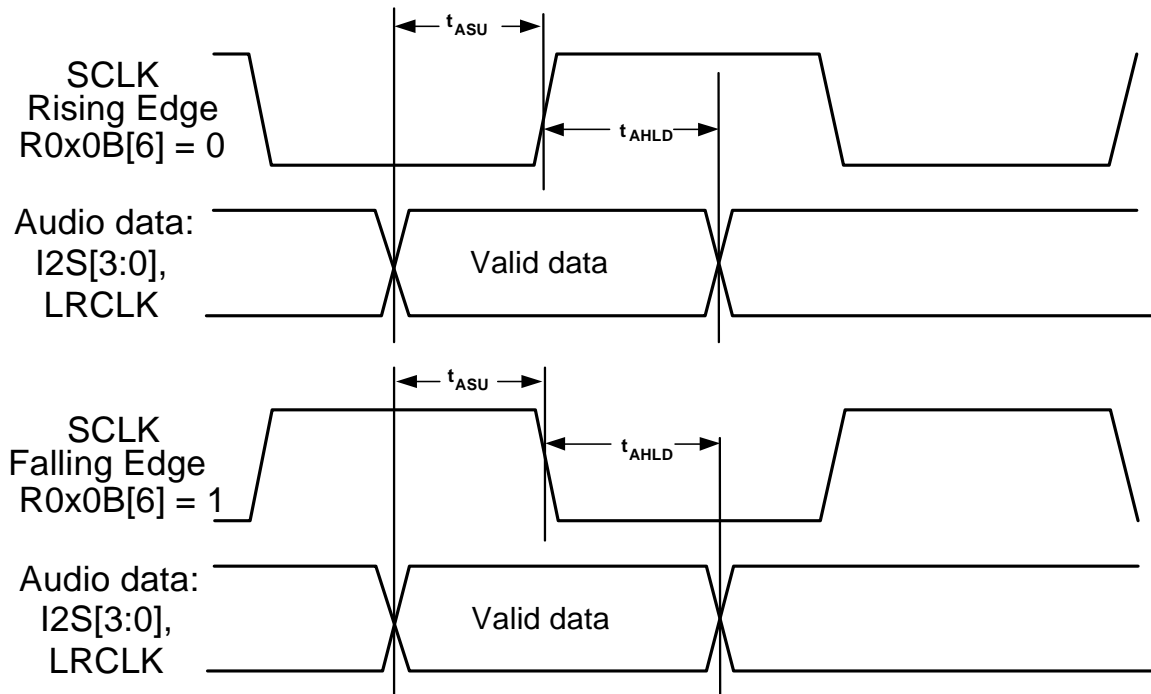


Figure 4 Timing for SPDIF Audio Interface

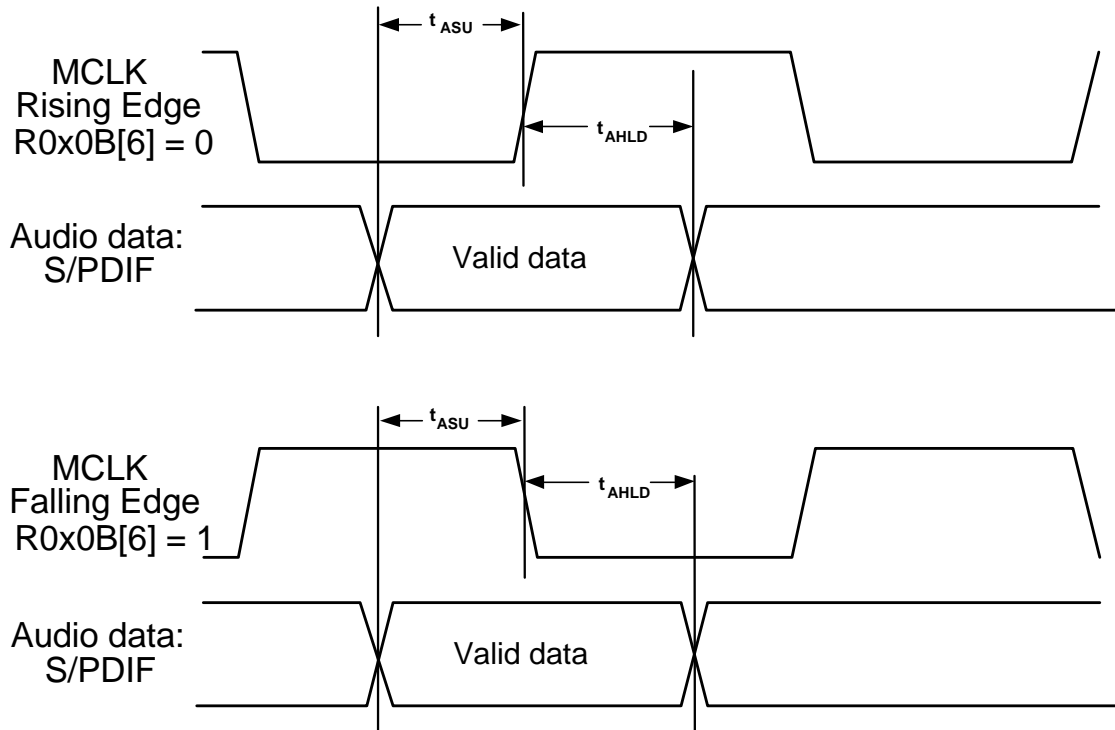


Figure 5 Timing for DSD Audio Interface

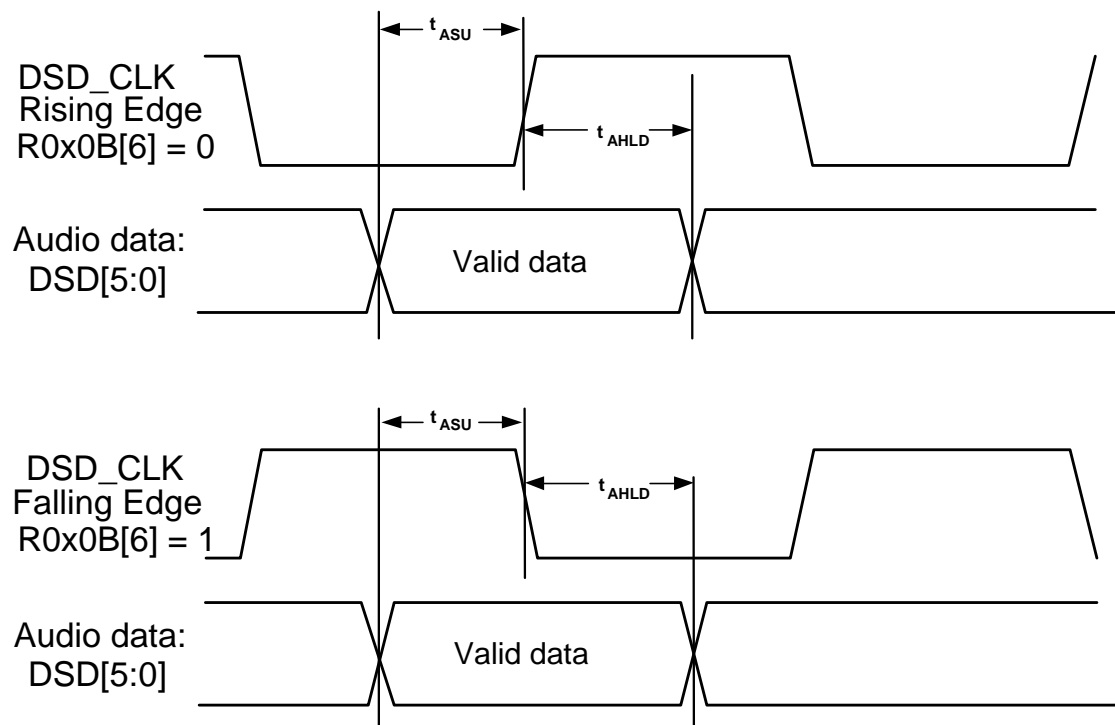


Table 2 Absolute Maximum Ratings

Parameter	Rating
Digital Inputs – I2C, HPD and CEC	5.5V to -0.3V
Digital Inputs – video/audio inputs	3.63V to -0.3V
Digital Output Current	20 mA
Operating Temperature Range	-40°C to +100°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage ratings assume that all power supplies are at nominal levels.

4.1 Explanation of Test Levels

I.	100% production tested.
II.	100% production tested at 25°C and sample tested at specified temperatures.
III.	Sample tested only.
IV.	Parameter is guaranteed by design and characterization testing.
V.	Parameter is a typical value only.
VI.	100% production tested at 25°C; guaranteed by design and characterization testing.
VII.	Limits defined by HDMI specification; guaranteed by design and characterization testing.
VIII.	Parameter is guaranteed by design.

4.2 ESD Caution



ESD (electrostatic discharge) sensitive device.
 Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SECTION 5: PIN AND PACKAGE INFORMATION

This section shows the pinout of the ADV7511 100-lead LQFP package. This section also contains a brief description of the different pins as well as the mechanical drawings

Figure 6 100-lead LQFP configuration (top view - not to scale)

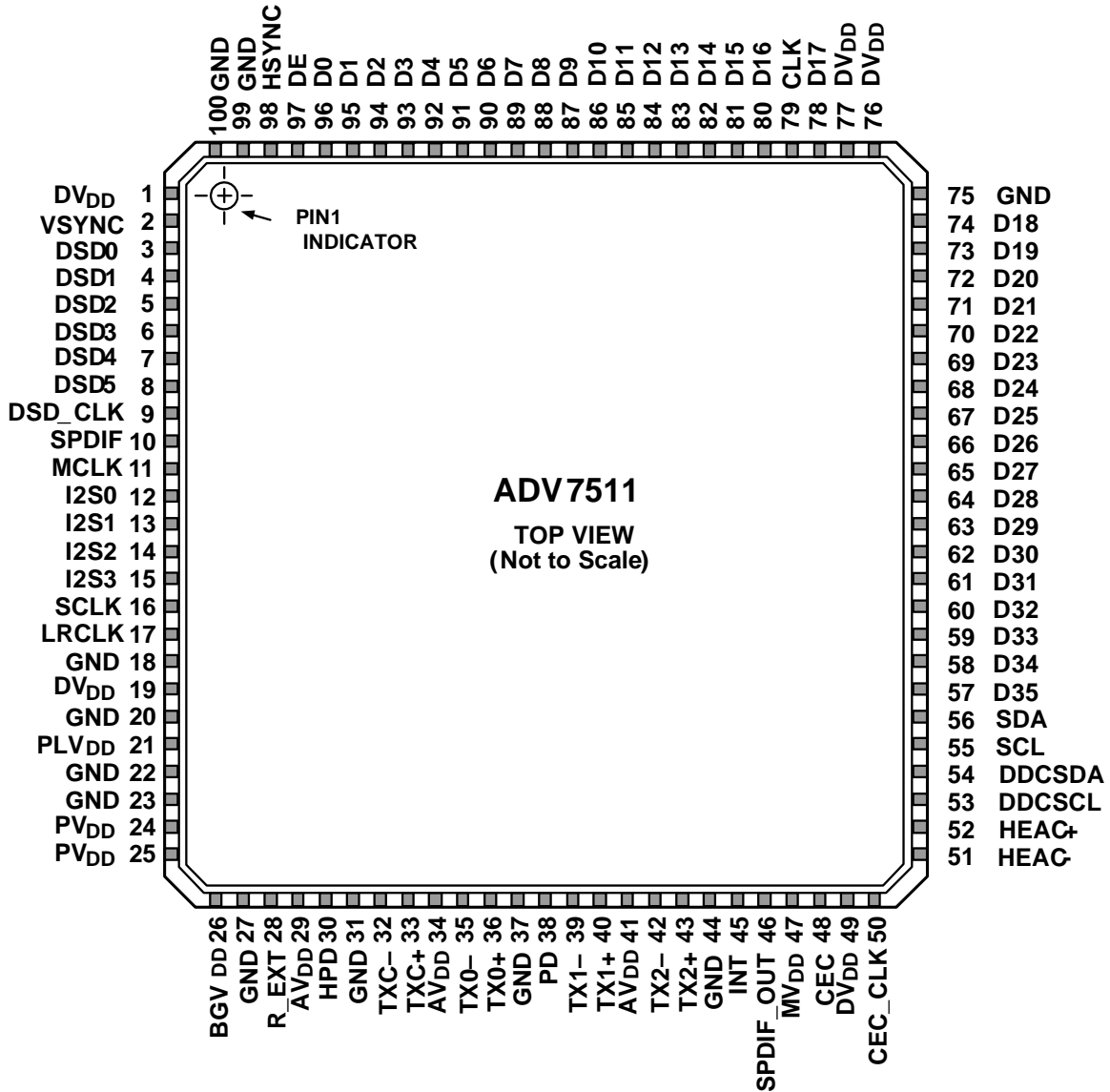


Table 3 Complete Pinout List ADV7511

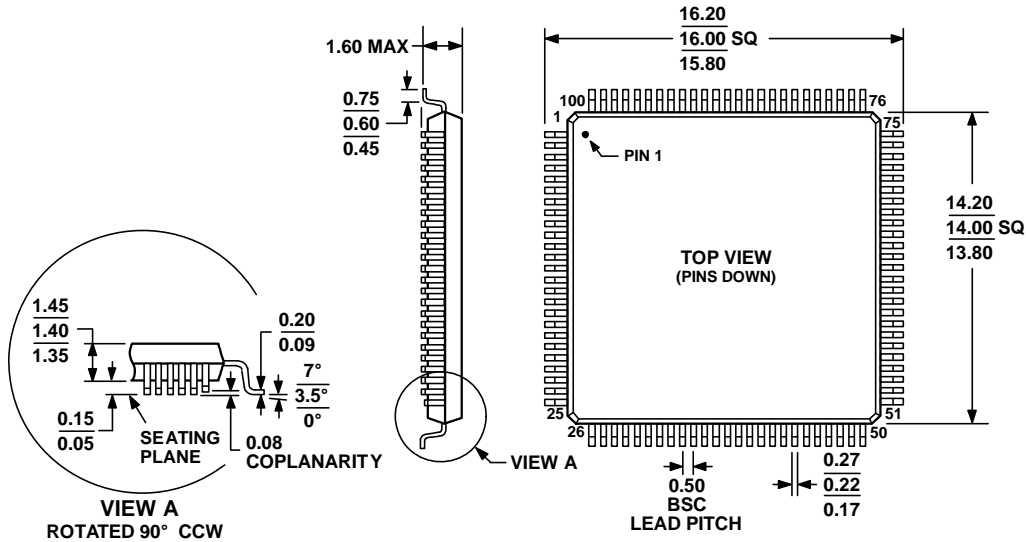
Pin No.	Mnemonic	Type ¹	Description
57-74, 78, 80-96	D[35:0]	I	Video Data Input. Digital input in RGB or YCbCr format. Supports typical CMOS logic levels from 1.8V up to 3.3V. See ► Figure 2 for timing details.
79	CLK	I	Video Clock Input. Supports typical CMOS logic levels from 1.8V up to 3.3V.
97	DE	I	Data Enable signal input for Digital Video. Supports typical CMOS logic levels from 1.8V up to 3.3V.
98	HSYNC	I	Horizontal Sync Input. Supports typical CMOS logic levels from 1.8V up to 3.3V.
2	VSYNC	I	Vertical Sync Input. Supports typical CMOS logic levels from 1.8V up to 3.3V.
28	R_EXT	I	Sets internal reference currents. Place 887 Ω resistor (1% tolerance) between this pin and ground.
51	HEAC-	I	HEAC- is one of a pair of differential lines for the ARC (Audio Return Channel)
52	HEAC+	I	HEAC+ is one of a pair of differential lines for the ARC (Audio Return Channel)
30	HPD	I	Hot Plug Detect signal input. This indicates to the interface whether the sink is connected. 1.8V to 5.0 V CMOS logic level.
10	SPDIF	I	SPDIF (Sony/Philips Digital Interface) Audio Input. This pin is typically used as the audio input from a Sony/Philips digital interface. Supports typical CMOS logic levels from 1.8V up to 3.3V. See ► Figure 4 for timing details.
46	SPDIF_OUT	O	SPDIF Audio Output from ARC receiver. 3.3V CMOS logic levels supported.
11	MCLK	I	Audio Reference Clock input. $128 \times N \times f_s$ with $N = 1, 2, 3, \text{ or } 4$. Set to $128 \times$ sampling frequency (f_s), $256 \times f_s$, $384 \times f_s$, or $512 \times f_s$. Supports typical CMOS logic levels from 1.8V up to 3.3V.
15-12	I ² S[3:0]	I	I ² S Audio Data Inputs. These represent the eight channels of audio (two per input) available through I ² S. Supports typical CMOS logic levels from 1.8V up to 3.3V. See Figure 3 for timing details.
16	SCLK	I	I ² S Audio Clock input. Supports typical CMOS logic levels from 1.8V up to 3.3V.
17	LRCLK	I	Left/Right Channel signal input. Supports typical CMOS logic levels from 1.8V up to 3.3V.
8-3	DSD[5:0]	I	DSD audio data inputs. See ► Figure 5 for timing details.
9	DSD_CLK	I	DSD Clock input. This is a 2.8224MHz clock for the DSD audio inputs.
38	PD/AD	I	Power-Down Control and I ² C Address Selection. The I ² C address and the PD polarity are set by the PD/AD pin state when the supplies are applied to the ADV7511. Supports typical CMOS logic levels from 1.8V up to 3.3V.
32, 33	TxC-/TxC+	O	Differential TMDS Clock Output. Differential clock output at pixel clock rate; TMDS logic level.
42, 43	Tx2-/Tx2+	O	Differential TMDS Output Channel 2. Differential output of the red data at $10 \times$ the pixel clock rate; TMDS logic level.
39, 40	Tx1-/Tx1+	O	Differential TMDS Output Channel 1. Differential output of the green data at $10 \times$ the pixel clock rate; TMDS logic level.
35, 36	Tx0-/Tx0+	O	Differential TMDS Output Channel 0. Differential output of the blue data at $10 \times$ the pixel clock rate; TMDS logic level.
45	INT	O	Interrupt signal output. CMOS logic level. A 2 k Ω pull-up resistor (10%) to interrupt the microcontroller IO supply is recommended.
29, 34, 41	AVDD	P	1.8V Power Supply for TMDS Outputs.
1, 19, 49, 76, 77	DVDD	P	1.8V Power Supply for Digital and I/O Power Supply. These pins supply power to the digital logic and I/Os. They should be filtered and as quiet as possible.
24, 25	PVDD	P	1.8V PLL Power Supply. These pins provide power to the digital portion of the clock PLL. The designer should provide quiet, noise-free power to these pins.
21	PLVDD	P	1.8V PLL Power Supply. The most sensitive portion of the ADV7511 is the clock generation circuitry. These pins provide power to the analog portion of the clock PLL (VCO). The designer should provide quiet, noise-free power to these pins.

26	BGVDD	P	Band Gap Vdd.
47	MVDD	P	3.3V Power Supply.
18, 20, 22, 23, 27, 31, 37, 44, 75, 99, 100	GND	P	Ground. The ground return for all circuitry on-chip. It is recommended that the ADV7511 be assembled on a single, solid ground plane with careful attention given to ground current paths.
56	SDA	C	Serial Port Data I/O. This pin serves as the serial port data I/O slave for register access. Supports CMOS logic levels from 1.8V to 3.3V.
55	SCL	C	Serial Port Data Clock input. This pin serves as the serial port data clock slave for register access. Supports CMOS logic levels from 1.8V to 3.3V.
54	DDCSDA	C	Serial Port Data I/O to Sink. This pin serves as the master to the DDC bus. Tolerant of 5 V CMOS logic levels.
53	DDCSCL	C	Serial Port Data Clock to Sink. This pin serves as the master clock for the DDC bus. Tolerant of 5 V CMOS logic levels.
50	CEC_CLK	I	CEC clock. From 3MHz to 100Mhz. Supports CMOS logic levels from 1.8V to 5V.
48	CEC	I/O	CEC data signal. Supports CMOS logic levels from 1.8V to 5V.

1. I = input, O = output, P = power supply, C = control

5.1 Mechanical Drawings and Outline Dimensions

Figure 7 100-lead Low-Profile Quad Flat Pack [LQFP]



COMPLIANT TO JEDEC STANDARDS MS-026-BED
 14 mm x 14 mm x 1.4 mm
 (ST-100)
 Dimensions shown in millimeters

A
6
1
6

SECTION 6: FUNCTIONAL DESCRIPTION

6.1 Input Connections

6.1.1 Unused Inputs

Any input data signals which are not used should be connected to ground.

6.1.2 Video Data Capture Block

The ADV7511 can accept video data from as few as eight pins (either YCbCr 4:2:2 double data rate [DDR] or YCbCr 4:2:2 with 2x pixel clock) to as many as 36 pins (RGB 4:4:4 or YCbCr 4:4:4). In addition it can accept HSYNC, VSYNC and DE (Data Enable). The ADV7511 can detect all of the 59 video formats defined in the EIA/CEA-861D specification. Either separate HSYNC, VSYNC, and DE, or embedded syncs in the style of the ITU BT.656, SMPTE 274M, and SMPTE 296M specifications are accepted. If less than 36 input pins are used, the alignment of the data can be defined as left-justified (all data begins from D35), right-justified (all data ends at D0), or center-justified. In the case of center justification, the channel data is left-justified in their respective 12-bit fields. For example a center-justified 24-bit RGB signal would have R[7:0] mapped to D[35:28]; G[7:0] mapped to D[23:16]; and B[7:0] mapped to D[11:4]. For timing details for video capture, see [Figure 2](#). For complete details on how to set these, refer to the ADV7511 Programming Guide.

The ADV7511 can accept HSYNC, VSYNC and DE (Data Enable) signals separately or as an embedded data (ITU 656 based) on the data inputs. If using separate syncs and DE is not available, the DE signal can be generated internally in the ADV7511.

The tables in section 6.1.2.1 define how the many different formats are accepted on the input data lines.

6.1.2.1 Video Input Connections

The following table is a summary of the input options which are shown in detail in [Table 5](#) through [Table 16](#).

Table 4 Input ID Selection

Input ID	Bits per Color	Pin Assignment Table	Maximum Input Clock	Format Name	Sync Type
0	8, 10	▶Table 5	165.0 MHz	RGB 4:4:4, YCbCr 4:4:4	Separate syncs
	12	▶Table 5	150.0 MHz	RGB 4:4:4, YCbCr 4:4:4	Separate syncs
1	8, 10, 12	▶Table 6- ▶Table 8	165.0 MHz	YCbCr 4:2:2	Separate syncs
2	8, 10, 12		165.0 MHz	YCbCr 4:2:2	Embedded syncs
3	8, 10, 12	▶Table 9- ▶Table 11	82.5 MHz	YCbCr 4:2:2 2X clock	Separate syncs
4	8, 10, 12		82.5 MHz	YCbCr 4:2:2 2X clock	Embedded syncs
5	8, 10, 12	▶Table 12- ▶Table 13	82.5 MHz	RGB 4:4:4, YCbCr 4:4:4 DDR	Separate syncs
6	8, 10, 12	▶Table 14- ▶Table 16	82.5 MHz	YCbCr 4:2:2 DDR	Separate syncs
7	8, 10, 12	▶Table 9- ▶Table 11	82.5 MHz	YCbCr 4:2:2 DDR	Separate syncs
8	8, 10, 12		82.5 MHz	YCbCr 4:2:2 DDR	Embedded syncs

Table 5 Normal RGB or YCbCr 4:4:4 (36, 30, or 24 bits) with Separate Syncs; Input ID = 0

Mode	Format	Input Data D[35:0]																																						
		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00			
36 bit	RGB	R[11:0]											G[11:0]											B[11:0]																
	YCrCb	Cr[11:0]											Y[11:0]											Cb[11:0]																
30 bit	RGB	R[9:0]															G[9:0]												B[9:0]											
	YCrCb	Cr[9:0]															Y[9:0]												Cb[9:0]											
24 bit	RGB	R[7:0]													G[7:0]												B[7:0]													
	YCrCb	Cr[7:0]													Y[7:0]												Cb[7:0]													
Pins D[35:0]		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00			

An input format of RGB 4:4:4 or YCbCr 4:4:4 can be selected by setting the input ID (R0x15 [3:0]) to 0x0. There is no need to set the Input Style (R0x16[3:2]) or channel alignment (R0x48[4:3]). For timing details see the [ADV7511 Hardware User's Guide](#).

Table 6 YCbCr 4:2:2 Formats (24, 20, or 16 bits) Input Data Mapping: R0x48[4:3] = '10' (left justified) Input ID = 1 or 2

Mode	Pixel	Input Data D[35:0]																																				
		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
Style 1																																						
24 bit	1 st	Cb[11:4]									Y[11:4]						Cb[3:0]			Y[3:0]																		
	2 nd	Cr[11:4]									Y[11:4]						Cr[3:0]			Y[3:0]																		
20 bit	1 st	Cb[9:2]									Y[9:2]						Cb[1:0]		Y[1:0]																			
	2 nd	Cr[9:2]									Y[9:2]						Cr[1:0]		Y[1:0]																			
16 bit	1 st	Cb[7:0]									Y[7:0]																											
	2 nd	Cr[7:0]									Y[7:0]																											
Style 2																																						
24 bit	1 st	Cb[11:0]											Y[11:0]																									
	2 nd	Cr[11:0]											Y[11:0]																									
20 bit	1 st	Cb[9:0]									Y[9:0]																											
	2 nd	Cr[9:0]									Y[9:0]																											
16 bit	1 st	Cb[7:0]									Y[7:0]																											
	2 nd	Cr[7:0]									Y[7:0]																											
Style 3																																						
24 bit	1 st	Y[11:0]											Cb[11:0]																									
	2 nd	Y[11:0]											Cr[11:0]																									
20 bit	1 st	Y[9:0]									Cb[9:0]																											
	2 nd	Y[9:0]									Cr[9:0]																											
16 bit	1 st	Y[7:0]									Cb[7:0]																											
	2 nd	Y[7:0]									Cr[7:0]																											
Pins D[35:0]		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	

Input ID = 1: An input with **YCbCr 4:2:2 with separate syncs** can be selected by setting the Input ID (R0x15[3:0]) to 0x1. The data bit width (24, 20, or 16 bits) must be set with R0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2].

Input ID = 2: An input with **YCbCr 4:2:2 with embedded syncs** (SAV [Start of Active Video] and EAV [End of Active Video]) can be selected by setting the Input ID (R0x15[3:0]) to 0x2. The data bit width (24 = 12 bits, 20 = 10 bits, or 16 = 8 bits) must be set with R0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The only difference between Input ID 1 and Input ID 2 is that the syncs on ID 2 are embedded in the data much like an ITU 656 style bus running at 1X clock and double width.

**Table 7 YCbCr 4:2:2 Formats (24, 20, or 16 bits) Input Data Mapping:
R0x48[4:3] = '01' (right justified) Input ID = 1 or 2**

Mode	Pixel	Input Data D[35:0]																																			
		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Style 1																																					
24 bit	1 st												Cb[11:4]				Y[11:4]				Cb[3:0]			Y[3:0]													
	2 nd												Cr[11:4]				Y[11:4]				Cr[3:0]			Y[3:0]													
20 bit	1 st												Cb[9:2]				Y[9:2]				Cb [1:0]				Y [1:0]												
	2 nd												Cr[9:2]				Y[9:2]				Cr [1:0]				Y [1:0]												
16 bit	1 st												Cb[7:0]				Y[7:0]																				
	2 nd												Cr[7:0]				Y[7:0]																				
Style 2																																					
24 bit	1 st												Cb[11:0]				Y[11:0]																				
	2 nd												Cr[11:0]				Y[11:0]																				
20 bit	1 st												Cb[9:0]				Y[9:0]																				
	2 nd												Cr[9:0]				Y[9:0]																				
16 bit	1 st												Y[7:0]				Cb[7:0]																				
	2 nd												Y[7:0]				Cr[7:0]																				
Style 3																																					
24 bit	1 st												Y[11:0]											Cb[11:0]													
	2 nd												Y[11:0]											Cr[11:0]													
20 bit	1 st												Y[9:0]				Cb[9:0]																				
	2 nd												Y[9:0]				Cr[9:0]																				
16 bit	1 st												Y[7:0]				Cb[7:0]																				
	2 nd												Y[7:0]				Cr[7:0]																				
Pins D[35:0]		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Input ID = 1: An input with YCbCr 4:2:2 with separate syncs can be selected by setting the Input ID (R0x15[3:0]) to 0x1. The data bit width (24, 20, or 16 bits) must be set with R0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2].																																					
Input ID = 2: An input with YCbCr 4:2:2 with embedded syncs (SAV and EAV) can be selected by setting the Input ID (R0x15[3:0]) to 0x2. The data bit width (24 = 12 bits, 20 = 10 bits, or 16 = 8 bits) must be set with R0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The only difference between Input ID 1 and Input ID 2 is that the syncs on ID 2 are embedded in the data much like an ITU 656 style bus running at 1X clock and double width.																																					

**Table 8 YCbCr 4:2:2 Formats (24, 20, or 16 bits) Input Data Mapping:
R0x48[4:3] = '00' (evenly distributed) Input ID = 1 or 2**

Mode	Pixel	Input Data D[35:0]																																			
		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Style 1																																					
24 bit	1 st	Cb[11:4]											Y[11:4]											Cb[3:0]			Y[3:0]										
	2 nd	Cr[11:4]											Y[11:4]											Cr[3:0]			Y[3:0]										
20 bit	1 st	Cb[9:2]											Y[9:2]											Cb[1:0]		Y[1:0]											
	2 nd	Cr[9:2]											Y[9:2]											Cr[1:0]		Y[1:0]											
16 bit	1 st	Cb[7:0]											Y[7:0]																								
	2 nd	Cr[7:0]											Y[7:0]																								
Style 2																																					
24 bit	1 st	Cb[11:4]											Cb[3:0]			Y[11:8]								Y[7:0]													
	2 nd	Cr[11:4]											Cr[3:0]			Y[11:8]								Y[7:0]													
20 bit	1 st	Cb[9:2]											Cb[1:0]		Y[9:4]								Y[3:0]														
	2 nd	Cr[9:2]											Cr[1:0]		Y[9:4]								Y[3:0]														
16 bit	1 st	Cb[7:0]											Y[7:0]																								
	2 nd	Cr[7:0]											Y[7:0]																								
Style 3																																					
24 bit	1 st	Y[11:4]											Y[3:0]			Cb[11:8]								Cb[7:0]													
	2 nd	Y[11:4]											Y[3:0]			Cr[11:8]								Cr[7:0]													
20 bit	1 st	Y[9:2]											Y[1:0]		Cb[9:4]								Cb[3:0]														
	2 nd	Y[9:2]											Y[1:0]		Cr[9:4]								Cr[3:0]														
16 bit	1 st	Y[7:0]											Cb[7:0]																								
	2 nd	Y[7:0]											Cr[7:0]																								
Pins D[35:0]		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Input ID = 1: An input with YCbCr 4:2:2 with separate syncs can be selected by setting the Input ID (R0x15[3:0]) to 0x1. The data bit width (24, 20, or 16 bits) must be set with R0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2].																																					
Input ID = 2: An input with YCbCr 4:2:2 with embedded syncs (SAV and EAV) can be selected by setting the Input ID (R0x15[3:0]) to 0x2. The data bit width (24 = 12 bits, 20 = 10 bits, or 16 = 8 bits) must be set with R0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The only difference between Input ID 1 and Input ID 2 is that the syncs on ID 2 are embedded in the data much like an ITU 656 style bus running at 1X clock and double width.																																					

**Table 10 YCbCr 4:2:2 Formats (12, 10, or 8 bits) Input Data Mapping:
R0x48[4:3] = '01' (right justified) Input ID = 3, 4, 7, or 8**

Mode	Pixel	Edge	Input Data D[35:0]																																			
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Style 1																																						
12 bit	1	1															Cb [11:4]								[3:0]													
		2															Y[11:4]								[3:0]													
	2	1															Cr [11:4]								[3:0]													
		2															Y[11:4]								[3:0]													
10 bit	1	1															Cb [9:2]							[1:0]														
		2															Y[9:2]							[1:0]														
	2	1															Cr [9:2]							[1:0]														
		2															Y[9:2]							[1:0]														
8 bit	1	1															Cb [7:0]																					
		2															Y[7:0]																					
	2	1															Cr [7:0]																					
		2															Y[7:0]																					
Style 2																																						
12 bit	1	1															Cb [11:0]																					
		2															Y[11:0]																					
	2	1															Cr [11:0]																					
		2															Y[11:0]																					
10 bit	1	1																			Cb [9:0]																	
		2																			Y[9:0]																	
	2	1																			Cr [9:0]																	
		2																			Y[9:0]																	
8 bit	1	1																			Cb [7:0]																	
		2																			Y[7:0]																	
	2	1																			Cr [7:0]																	
		2																			Y[7:0]																	
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Input ID = 3: An input with **YCbCr 4:2:2 data and separate syncs** can be selected by setting the Input ID (R0x15[3:0]) to 0x3. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The two input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. Pixel 1 is the first pixel of the 4:2:2 word and should be where DE starts. **This mode requires an input clock 2X the pixel rate.** For timing details, see the [ADV7511 Hardware User's Guide](#) and [Figure 8](#).

Input ID = 4: An input with **YCbCr 4:2:2 and embedded syncs** (ITU 656 based) can be selected by setting the Input ID (R0x15[3:0]) to 0x4. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The two input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The order of data input is the order in the table. For example, data is accepted as: Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3... Pixel 1 is the first pixel of the 4:2:2 word and should be where DE starts. **This mode requires an input clock 2X the pixel rate.** For timing details, see the [ADV7511 Hardware User's Guide](#) and [Figure 8](#).

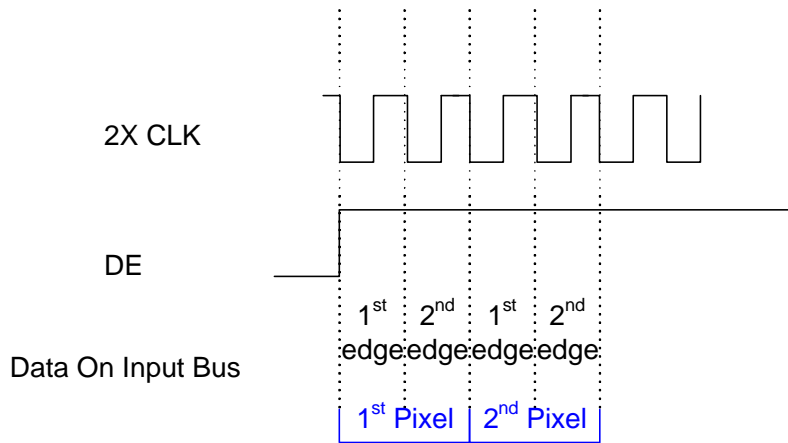
Input ID=7: This input format is the same as input ID 3 with the exception that the clock is not 2X the pixel rate, but is double data rate (DDR) and the Input ID (R0x15[3:0]) is set to 0x7. For timing details, see the [ADV7511 Hardware User's Guide](#) and [Figure 9](#) and [Figure 10](#). The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge.

Input ID=8: This input format is the same as input ID 4 with the exception that the clock is not 2X the pixel rate, but is double data rate (DDR) and the Input ID (R0x15[3:0]) is set to 0x8. For timing details, see the [ADV7511 Hardware User's Guide](#) and [Figure 9](#) and [Figure 10](#). The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge.

**Table 11 YCbCr 4:2:2 Formats (12, 10, or 8 bits) Input Data Mapping:
R0x48[4:3] = '00' (evenly distributed) Input ID = 3, 4, 7, or 8**

Mode	Pixel	Edge	Input Data D[35:0]																																			
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Style 1																																						
12 bit	1	1												Cb [11:4]															[3:0]									
		2												Y[11:4]															[3:0]									
	2	1												Cr[11:4]															[3:0]									
		2												Y[11:4]															[3:0]									
10 bit	1	1												Cb [9:2]														[1:0]										
		2												Y[9:2]														[1:0]										
	2	1												Cr[9:2]														[1:0]										
		2												Y[9:2]														[1:0]										
8 bit	1	1												Cb [7:0]																								
		2												Y[7:0]																								
	2	1												Cr[7:0]																								
		2												Y[7:0]																								
Style 2																																						
12 bit	1	1												Cb [11:8]															Cb [7:0]									
		2												Y[11:8]															Y[7:0]									
	2	1												Cr[11:8]															Cr[7:0]									
		2												Y[11:8]															Y[7:0]									
10 bit	1	1												Cb [9:8]														Cb [7:0]										
		2												Y [9:8]														Y[7:0]										
	2	1												Cr [9:8]														Cr[7:0]										
		2												Y [9:8]														Y[7:0]										
8 bit	1	1																										Cb [7:0]										
		2																										Y[7:0]										
	2	1																										Cr[7:0]										
		2																										Y[7:0]										
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
<p>Input ID = 3: An input with YCbCr 4:2:2 data and separate syncs can be selected by setting the Input ID (R0x15[3:0]) to 0x3. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The two input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. Pixel 1 is the first pixel of the 4:2:2 word and should be where DE starts. This mode requires an input clock 2X the pixel rate. For timing details, see the ADV7511 Hardware User's Guide and Figure 8.</p>																																						
<p>Input ID = 4: An input with YCbCr 4:2:2 and embedded syncs (ITU 656 based) can be selected by setting the Input ID (R0x15[3:0]) to 0x4. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The two input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The order of data input is the order in the table. For example, data is accepted as: Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3... Pixel 1 is the first pixel of the 4:2:2 word and should be where DE starts. This mode requires an input clock 2X the pixel rate. For timing details, see the ADV7511 Hardware User's Guide and Figure 8.</p>																																						
<p>Input ID=7: This input format is the same as input ID 3 with the exception that the clock is not 2X the pixel rate, but is double data rate (DDR) and the Input ID (R0x15[3:0]) is set to 0x7. For timing details, see the ADV7511 Hardware User's Guide and Figure 9 and Figure 10. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge.</p>																																						
<p>Input ID=8: This input format is the same as input ID 4 with the exception that the clock is not 2X the pixel rate, but is double data rate (DDR) and the Input ID (R0x15[3:0]) is set to 0x8. For timing details, see the ADV7511 Hardware User's Guide and Figure 9 and Figure 10. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge.</p>																																						

Figure 8 2X Clock timing



**Table 12 RGB or YCbCr 4:4:4 (12, 10 or 8 bits) DDR with Separate Syncs:
Input ID = 5, left aligned (R0x48[5] = 1)**

Mode	Pixel	Edge	Input Data Mapping Input ID = 5																																
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03
			Style 1																																
12 bit	1	1	G[5:0]						B[11:0]																										
		2	R[11:0]						G[11:6]																										
	2	1	Y[5:0]						Cb[9:0]																										
		2	Cr[11:0]						Y[11:6]																										
10 bit	1	1	G[4:0]				B[9:0]																												
		2	R[9:0]				G[9:5]																												
	2	1	Y[4:0]				Cb[9:0]																												
		2	Cr[9:0]				Y[9:5]																												
8 bit	1	1	G[3:0]			B[7:0]																													
		2	R[7:0]			G[7:4]																													
	2	1	Y[3:0]			Cb[7:0]																													
		2	Cr[7:0]			Y[7:4]																													
			Style 2																																
12 bit	1	1	R[11:0]						G[11:6]																										
		2	G[4:0]						B[11:0]																										
	2	1	Cr[11:0]						Y[11:6]																										
		2	Y[5:0]						Cb[11:0]																										
10 bit	1	1	R[9:0]				G[9:5]																												
		2	G[4:0]				B[9:0]																												
	2	1	Cr[9:0]				Y[9:5]																												
		2	Y[4:0]				Cb[9:0]																												
8 bit	1	1	R[7:0]			G[7:4]																													
		2	G[3:0]			B[7:0]																													
	2	1	Cr[7:0]			Y[7:4]																													
		2	Y[3:0]			Cb[7:0]																													
			Style 3																																
12 bit	1	1	Y[11:0]						Cb[11:6]																										
	2	Cb[5:0]						Cr[11:0]																											
10 bit	1	1	Y[9:0]				Cb[9:5]																												
	2	Cb[4:0]				Cr[9:0]																													
8 bit	1	1	Y[7:0]			Cb[7:4]																													
	2	Cb[3:0]			Cr[7:0]																														

Input ID=5: An input format of **RGB 4:4:4 DDR** or **YCbCr 4:4:4 DDR** can be selected by setting the input ID (R0x15 [3:0]) to 0x5. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:4:4 word and should be where DE starts.

**Table 13 RGB or YCbCr 4:4:4 (12 bits) DDR with Separate Syncs:
Input ID = 5, right aligned (R0x48[5] = 0)**

Mode	Pixel	Edge	Input Data Mapping Input ID = 5																																			
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
			Style 1																																			
12 bit	1	1																G[5:0]					B[11:0]															
		2																R[11:0]						G[11:6]														
	2	1																Y[5:0]					Cb[9:0]															
		2																Cr[11:0]						Y[11:6]														
10 bit	1	1																G[4:0]				B[9:0]																
		2																R[9:0]					G[9:5]															
	2	1																Y[4:0]				Cb[9:0]																
		2																Cr[9:0]					Y[9:5]															
8 bit	1	1																G[3:0]			B[7:0]																	
		2																R[7:0]				G[7:4]																
	2	1																Y[3:0]			Cb[7:0]																	
		2																Cr[7:0]				Y[7:4]																
			Style 2																																			
12 bit	1	1																R[11:0]						G[11:6]														
		2																G[4:0]				B[11:0]																
	2	1																Cr[11:0]						Y[11:6]														
		2																Y[5:0]					Cb[11:0]															
10 bit	1	1																R[9:0]					G[9:5]															
		2																G[4:0]				B[9:0]																
	2	1																Cr[9:0]					Y[9:5]															
		2																Y[4:0]				Cb[9:0]																
8 bit	1	1																R[7:0]				G[7:4]																
		2																G[3:0]			B[7:0]																	
	2	1																Cr[7:0]				Y[7:4]																
		2																Y[3:0]			Cb[7:0]																	
			Style 3																																			
12 bit	1	1																Y[11:0]						Cb[11:6]														
		2																Cb[5:0]					Cr[11:0]															
10 bit	1	1																Y[9:0]					Cb[9:5]															
		2																Cb[4:0]				Cr[9:0]																
8 bit	1	1																Y[7:0]				Cb[7:4]																
		2																Cb[3:0]			Cr[7:0]																	
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Input ID=5: An input format of **RGB 4:4:4 DDR or YCbCr 4:4:4 DDR** can be selected by setting the input ID (R0x15 [3:0]) to 0x5. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:4:4 word and should be where DE starts.

**Table 14 YCbCr 4:2:2 (12, 10, or 8 bits) DDR with Separate Syncs:
Input ID = 6, right justified (R0x48[4:3] = '01')**

Mode	Pixel	Edge	Input Data Mapping Input ID = 6																																			
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
YCbCr			Style 1																																			
12bit	1	1												Y[7:4]			Cb[3:0]			Y[3:0]																		
		2												Cb[11:4]						Y[11:8]																		
	2	1												Y[7:4]			Cr[3:0]			Y[3:0]																		
		2												Cr[11:4]						Y[11:8]																		
10bit	1	1												Y[5:4]		Cb[3:0]		Y[3:0]																				
		2												Cb[9:4]			Y[9:6]																					
	2	1												Y[5:4]		Cr[3:0]		Y[3:0]																				
		2												Cr[9:4]			Y[9:6]																					
8bit	1	1												Cb[3:0]			Y[3:0]																					
		2												Cb[7:4]		Y[7:4]																						
	2	1												Cr[3:0]			Y[3:0]																					
		2												Cr[7:4]		Y[7:4]																						
			Style 2																																			
12bit	1	1												Y[11:0]																								
		2												Cb[11:0]																								
	2	1												Y[11:0]																								
		2												Cr[11:0]																								
10bit	1	1												Y[9:0]																								
		2												Cb[9:0]																								
	2	1												Y[9:0]																								
		2												Cr[9:0]																								
8bit	1	1												Y[7:0]																								
		2												Cb[7:0]																								
	2	1												Y[7:0]																								
		2												Cr[7:0]																								
			Style 3																																			
12bit	1	1												Cb[11:0]																								
		2												Y[11:0]																								
	2	1												Cr[11:0]																								
		2												Y[11:0]																								
10bit	1	1												Cb[9:0]																								
		2												Y[9:0]																								
	2	1												Cr[9:0]																								
		2												Y[9:0]																								
8bit	1	1												Cb[7:0]																								
		2												Y[7:0]																								
	2	1												Cr[7:0]																								
		2												Y[7:0]																								
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

An input format of YCbCr 4:2:2 DDR can be selected by setting the input ID (R0x15 [3:0]) to 0x6. The three different input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The Data Input Edge is defined in R0x16 [1]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:2:2 word and should be where DE starts.

**Table 16 YCbCr 4:2:2 (12, 10, or 8 bits) DDR with Separate Syncs:
Input ID = 6, evenly distributed (R0x48[4:3] = '00')**

Mode	Pixel	Edge	Input Data Mapping Input ID = 6																																			
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
YCbCr			Style 1																																			
12bit	1	1	Y[7:4]										Cb[3:0]										Y[3:0]															
		2	Cb[11:8]										Cb[7:4]										Y[11:8]															
	2	1	Y[7:4]										Cr[3:0]										Y[3:0]															
		2	Cr[11:8]										Cr[7:4]										Y[11:8]															
10bit	1	1	Y[5:4]					Cb[3:2]					Cb[1:0]					Y[3:2]					Y[1:0]															
		2	Cb[9:6]					Cb[5:4]					Y[9:8]					Y[7:6]																				
	2	1	Y[5:4]					Cr[3:2]					Cr[1:0]					Y[3:2]					Y[1:0]															
		2	Cr[9:6]					Cr[5:4]					Y[9:6]					Y[5:4]																				
8bit	1	1	Cb[3:0]										Y[3:0]																									
		2	Cb[7:4]										Y[7:4]																									
	2	1	Cr[3:0]										Y[3:0]																									
		2	Cr[7:4]										Y[7:4]																									
			Style 2																																			
12bit	1	1	Y[11:8]										Y[7:4]										Y[3:0]															
		2	Cb[11:8]										Cb[7:4]										Cb[3:0]															
	2	1	Y[11:8]										Y[7:4]										Y[3:0]															
		2	Cr[11:8]										Cr[7:4]										Cr[3:0]															
10bit	1	1	Y[9:6]					Y[5:2]					Y[1:0]																									
		2	Cb[9:6]					Cb[5:2]					Cb[1:0]																									
	2	1	Y[9:6]					Y[5:2]					Y[1:0]																									
		2	Cr[9:6]					Cr[5:2]					Cr[1:0]																									
8bit	1	1	Y[7:0]										Y[7:0]																									
		2	Cb[7:0]										Cb[7:0]																									
	2	1	Y[7:0]										Y[7:0]																									
		2	Cr[7:0]										Cr[7:0]																									
			Style 3																																			
12bit	1	1	Cb[11:8]										Cb[7:4]										Cb[3:0]															
		2	Y[11:0]										Y[7:4]										Y[3:0]															
	2	1	Cr[11:0]										Cr[7:4]										Cr[3:0]															
		2	Y[11:0]										Y[7:4]										Y[3:0]															
10bit	1	1	Cb[9:6]					Cb[5:2]					Cb[1:0]																									
		2	Y[9:6]					Y[5:2]					Y[1:0]																									
	2	1	Cr[9:6]					Cr[5:2]					Cr[1:0]																									
		2	Y[9:6]					Y[5:2]					Y[1:0]																									
8bit	1	1	Cb[7:4]										Cb[3:0]																									
		2	Y[7:4]										Y[3:0]																									
	2	1	Cr[7:4]										Cr[3:0]																									
		2	Y[7:4]										Y[3:0]																									
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

An input format of YCbCr 4:2:2 DDR can be selected by setting the input ID (R0x15 [3:0]) to 0x6. The three different input pin assignment styles are shown in the table. The Input Style can be set in R0x16[3:2]. The data bit width (12, 10, or 8 bits) must be set with R0x16 [5:4]. The Data Input Edge is defined in R0x16 [1]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in R0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:2:2 word and should be where DE starts.

Figure 9 DDR DE timing - Register 0x16[1] = 1

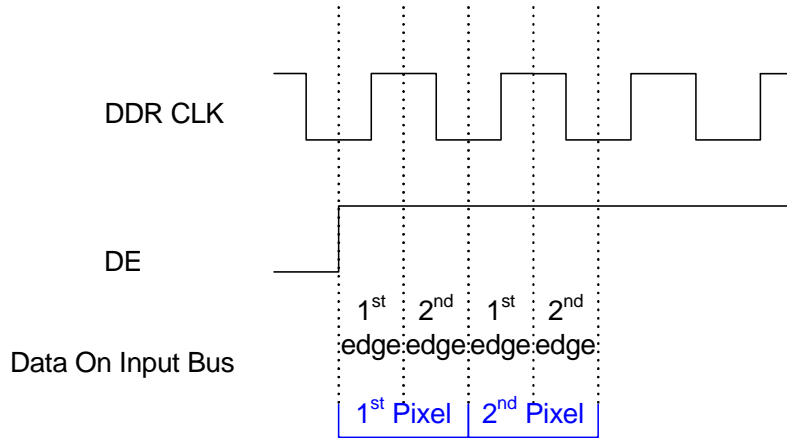
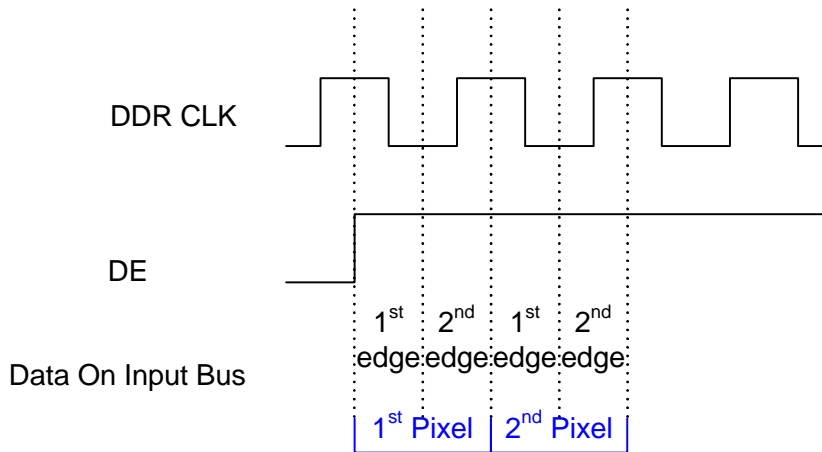


Figure 10 DDR DE timing - Register 0x16[1] = 0



6.1.3 Audio Data Capture Block

The ADV7511 supports multiple audio interfaces and formats: I2S, SPDIF, DSD, DST, and HBR. The ADV7511 supports audio input frequencies of 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz, and higher (with use of HBR). The MCLK signal is optional unless specifically listed in ► [Table 17](#). The I2S audio inputs can support standard I2S, left-justified serial audio, right-justified serial audio and AES3 stream formats. The Audio Data Capture Block captures the audio samples and converts them into audio packets which are sent through the HDMI link (if the ADV7511 is set in HDMI mode). Please refer to the ADV7511 Programming Guide for more information.

6.1.3.1 Supported Audio Input Format and Implementation

ADV7511 is capable of receiving audio data for packetization and transmission over the HDMI interface in any of the following formats:

- Inter IC Sound (I2S)
- Sony/Philips Digital Interface (SPDIF)
- Direct Stream Digital audio (DSD)
- Direct Stream Transfer (DST)
- High Bit-Rate (HBR)

Table 17 illustrates the many audio input and output options that are available with the ADV7511. Unless specifically listed as a clock requirement, the MCLK is optional.

Table 17 Audio input format summary

Input				Output			
Audio Select	Audio Mode	I2S Format	Data Input Pins	Clock(s)	Encoding	Format	Output Packet Type
R0x0A[6:4]	R0x0A[4:3]	R0x0C[1:0]					
000	**	00	I2S[3:0]	SCLK & LRCLK	Normal	Standard I2S	Audio Sample Packet
000	**	01	I2S[3:0]	SCLK & LRCLK	Normal	Right Justified	Audio Sample Packet
000	**	10	I2S[3:0]	SCLK & LRCLK	Normal	Left Justified	Audio Sample Packet
000	**	11	I2S[3:0]	SCLK & LRCLK	Normal	AES3 Direct	Audio Sample Packet
001	00	**	SPDIF	MCLK	Bi-Phase Mark	IEC60958 or IEC61937	Audio Sample Packet
010	0*	**	DSD[5:0] & I2S[4:3]	DSD_CLK	Normal	DSD	One Bit Audio Sample Packet
010	1*	**	DSD[5:0] & I2S[4:3]	DSD_CLK	SDIF-3	DSD	One Bit Audio Sample Packet
011	00	**	I2S[3:0]	SCLK & LRCLK	Bi-Phase Mark	IEC61937	HBR Audio Stream Packet
011	01	00	I2S[3:0]	SCLK & LRCLK	Normal	Standard I2S	HBR Audio Stream Packet
011	01	01	I2S[3:0]	SCLK & LRCLK	Normal	Right Justified	HBR Audio Stream Packet
011	01	10	I2S[3:0]	SCLK & LRCLK	Normal	Left Justified	HBR Audio Stream Packet
011	01	11	I2S[3:0]	SCLK & LRCLK	Normal	AES3 Direct	HBR Audio Stream Packet
011	10	**	SPDIF	MCLK	Bi-Phase Mark	IEC61937	HBR Audio Stream Packet
011	11	00	SPDIF	MCLK	Normal	Standard I2S	HBR Audio Stream Packet
011	11	01	SPDIF	MCLK	Normal	Right Justified	HBR Audio Stream Packet
011	11	10	SPDIF	MCLK	Normal	Left Justified	HBR Audio Stream Packet
011	11	11	SPDIF	MCLK	Normal	IEC61937	HBR Audio Stream Packet
100	*0	**	DSD[5:4]	DSD_CLK	Normal	DST Normal	DST Audio Packet
100	01	**	DSD[5:4]	DSD_CLK	Normal	DST 2X	DST Audio Packet
100	11	**	DSD[5:4]	DSD_CLK	Normal	DST 1X (DDR)	DST Audio Packet

6.1.3.2 **Inter-IC Sound (I2S) Audio**

The ADV7511 can accommodate from two to eight channels of I2S audio at up to a 192KHz sampling rate. The ADV7511 supports standard I2S, left-justified serial audio, right-justified serial audio and AES3 stream formats via R0x0C[1:0] and sample word lengths between 16 bits and 24 bits (R0x14[3:0]).

If the I2S data changes on the rising clock edge it is recommended that it be latched into the ADV7511 on the falling edge. If the I2S data changes on the falling clock edge, it is recommended that it be latched into the ADV7511 on the rising edge. This can be specified by programming register R0x0B[6]. 0 = latch on the rising clock edge; 1 = latch on the falling clock edge. For more information see the following figures:

- ▶ [Figure 11](#) –▶ [Figure 14](#) for format information
- ▶ [Figure 3](#) for timing information
- ▶ Please refer to the *ADV7511 Programming Guide* for more information about configuring the audio.

The accurate transmission of audio depends upon an accurate SCLK and can be a function of the duty cycle of the SCLK. ▶[Table 18](#) specifies this duty cycle dependency. ‘N’ and ‘CTS’ values are used to reconstruct the audio data and if the ‘N’ value is an odd number, the SCLK duty cycle must be within the range of 49 – 51%; if the ‘N’ value is an even number and the audio is in a 32 bit format the SCLK duty cycle requirements can be in a much wider range of 40 – 60%. For the case of 16 bit audio format, ‘N’ values which are not divisible by 4 restrict the duty cycle to 49-51% where an ‘N’ value which is evenly divisible by 4 may have a duty cycle from 40% - 60%.

Table 18 SCLK Duty Cycle

N value	SCLK DC requirement (16 bit audio)	SCLK DC requirement (32 bit audio)
N is odd	Not supported	49-51%
N is a even but not a multiple of 4	49-51%	40-60%
N is even & a multiple of 4	40-60%	40-60%

Figure 11 I2S Standard Audio – Data width 16 to 24 bits per channel

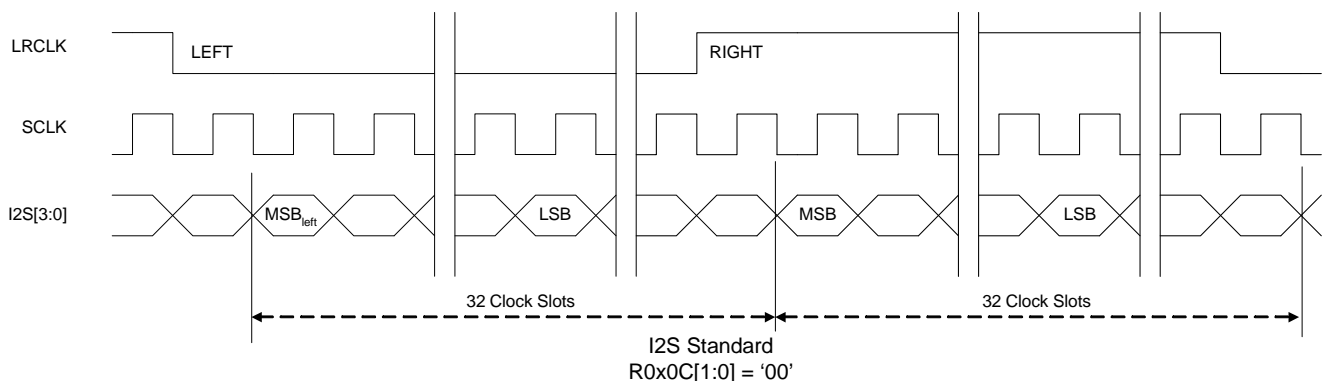


Figure 12 I2S Standard Audio – 16-bit samples only

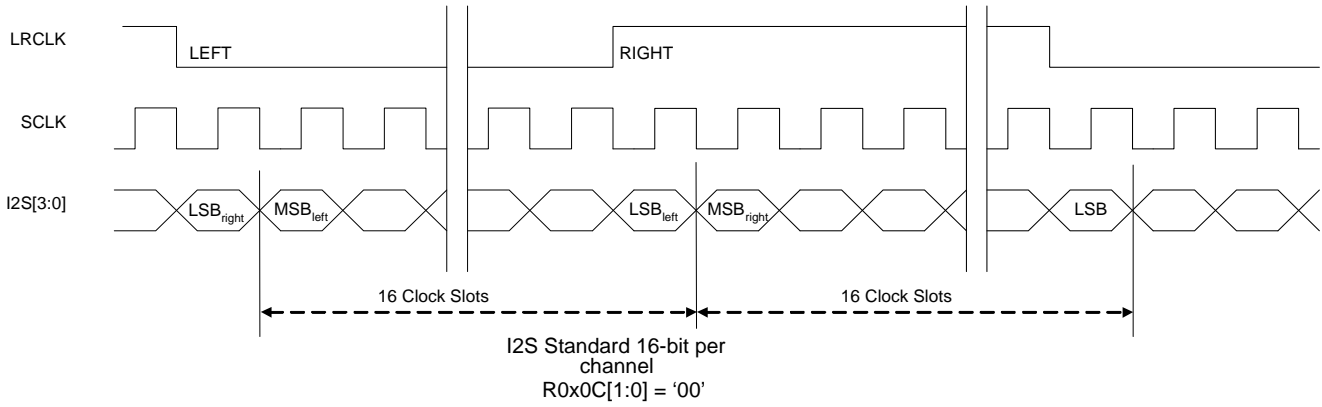


Figure 13 Serial Audio – Right-Justified

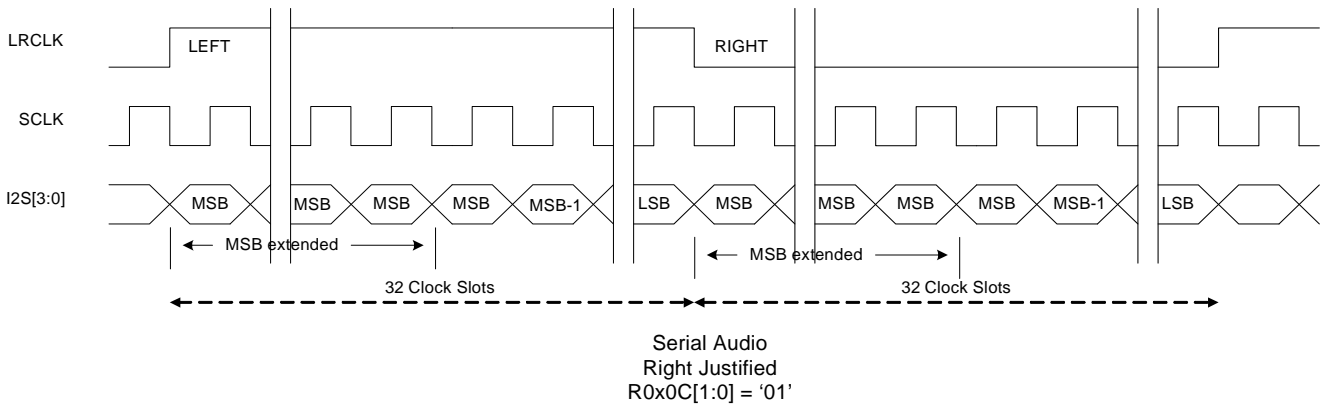


Figure 14 Serial Audio – Left-Justified

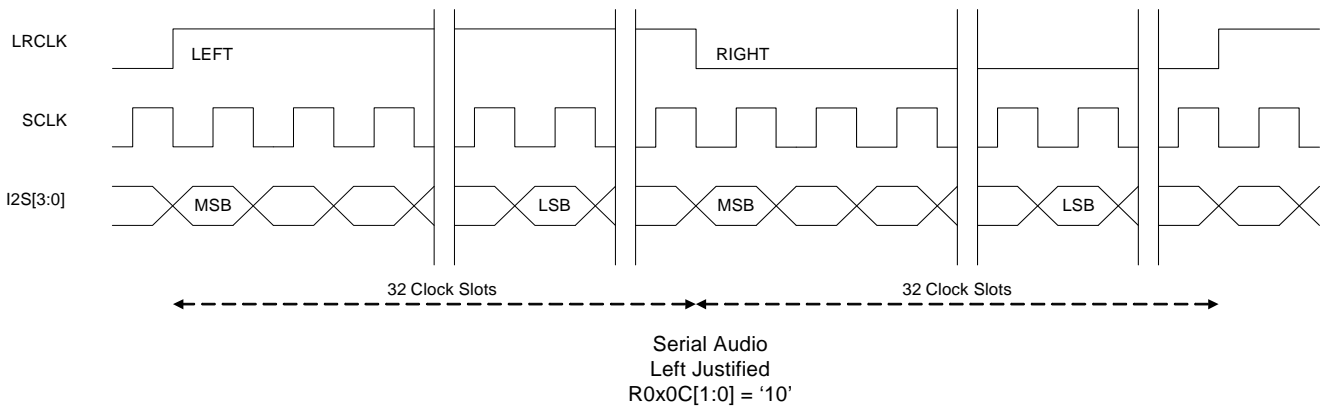
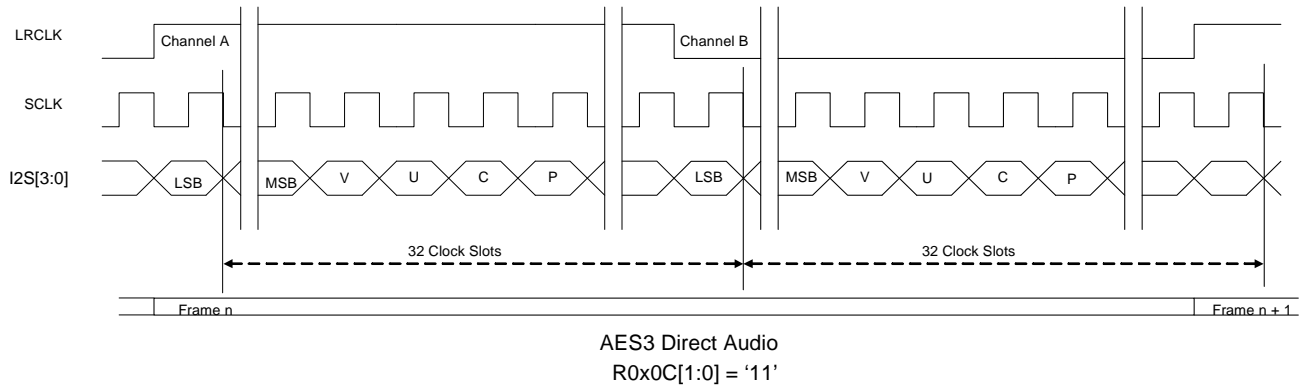


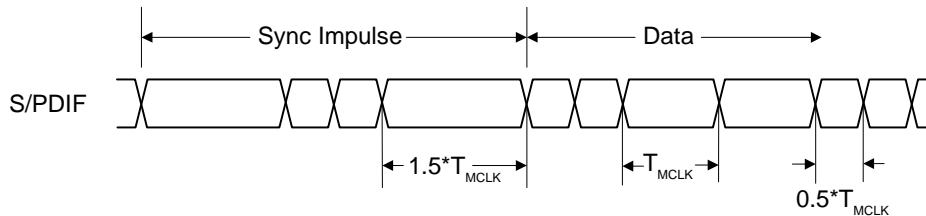
Figure 15 AES3 Direct Audio



6.1.3.3 **Sony/Philips Digital Interface (SPDIF)**

The ADV7511 is capable of accepting two-channel linear pulse code modulation (LPCM) and encoded audio up to a 192KHz sampling rate via the SPDIF. SPDIF audio input is selected by setting R0x0A[4] = '1'. The ADV7511 is capable of accepting SPDIF with or without an MCLK input. When no MCLK is present the ADV7511 generates its own MCLK internally based on the SPDIF information to sample the data and determine the CTS value. For timing information see ►Figure 4.

Figure 16 SPDIF Data Timing



6.1.3.4 **DSD Audio**

Direct Stream Digital (DSD) Audio uses the One Bit Audio packets to transfer data across the Transition Minimized Differential Signaling (TMDS) link. Up to eight channels of DSD data can be input onto eight data lines (DSD[5:0] plus I2S3 and I2S2 if channels 7 and 8 are required) clocked by the DSD_CLK at 2.8224MHz. For timing information see ►Figure 5.

6.1.3.5 **HBR Audio**

High Bit-Rate audio uses the HBR audio packets to transfer compressed data at rates greater than 6.144Mbps across the TMDS link. For additional information, refer to IEC61937.

6.1.3.6 **DST Audio**

Direct Stream Transfer audio is compressed DSD audio. This format is sent in frames which are in time slots equal to 1/75 of a second. The DST audio packets will be used to send the data across the TMDS link. Refer to ISO/IEC14496, Part 3 for additional information.

6.1.4 **Hot Plug Detect (HPD) pin**

The Hot Plug Detect (HPD) pin is an input which detects if a DVI or HDMI sink is connected. If the voltage on HPD is greater than 1.2V, then the ADV7511 considers an HDMI/DVI sink is connected. If the voltage is below 1.2V, then the ADV7511 considers no sink is connected. The HPD must be connected to the HDMI connector. A 10K Ω (+/-10%) pull down resistor to ground is recommended: this ensures that 0V is present on the HPD pin when no sink is connected.

6.1.5 **Power Down / I2C Address (PD/AD)**

The Power Down / Address (PD/AD) input pin can be connected to GND or AVDD (through a 2K Ω (+/-10%) resistor or a control signal). The device address and power down polarity are set by the state of the PD/AD pin when the ADV7511 supplies are applied. For example, if the PD/AD pin is low (when the supplies are turned on) then the device address will be 0x72 and the power down will be active high. If the PD/AD pin is high (when the supplies are turned on), the device address will be 0x7A and the power down will be active low. The ADV7511 power state can also be controlled via I2C registers (the PD pin and PD register bit are "or'ed" together). For further information, please refer to the Power Management section of the ADV7511 Programming Guide.

6.1.6 **Input Voltage Tolerance**

The digital inputs (video, audio) on the ADV7511 work with 1.8V and 3.3V signal levels. The I2C ports (DDCSDA/DDCSCL and SDA/SCL) and (Consumer Electronic Control) CEC port work with 1.8V and 3.3V and are tolerant of 5V logic levels.

6.2 **Audio Return Channel (ARC)**

An HDMI v1.4 feature incorporated in the ADV7511 is HEAC (ARC). The Audio Return Channel is part of the HDMI Ethernet Audio return Channel (HEAC). With this capability, the TV can send back audio to the TMDS source for processing and distribution. This audio channel can be sent over a differential pair (common mode component) or on a single line. The differential signals are on the HEAC+ pin and the HEAC- pin. A single mode transmission will be on the HEAC+ line. The ARC allows audio from a display with a tuner to be sent to a receiver over the HDMI cable for better audio reproduction. All HDMI cables will support this feature and use of this can reduce the amount of cables in the system.

The audio data is a stereo L-PCM (IEC 60958-1) stream supporting 32KHz, 44.1KHz or 48KHz sampling. These represent a clock rate of respectively: 4.096MHz, 5.6448MHz and 6.144MHz.

Control of the ARC is initiated by the sink over the CEC lines. The capabilities of the source can be discovered in this fashion with the TMDS sink driving the ARC line(s).

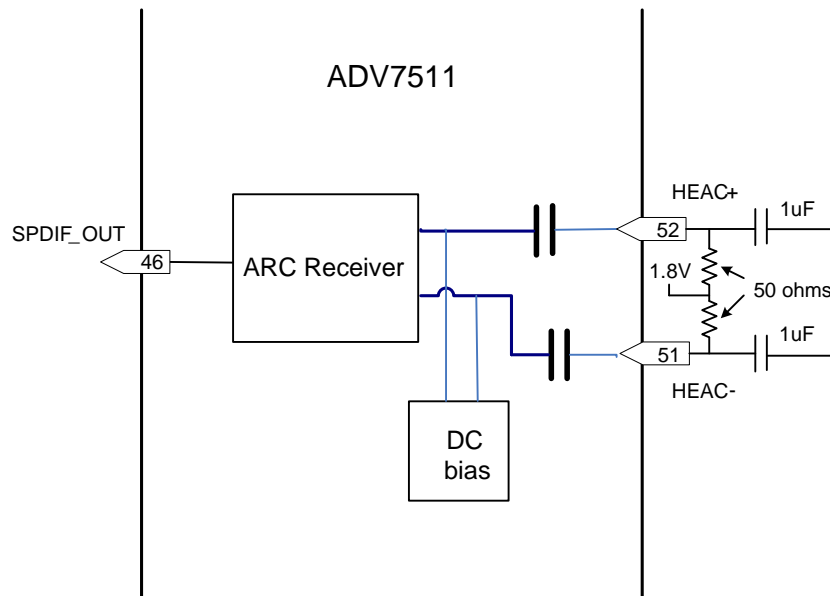
6.2.1 **Unused ARC**

If the ARC function is not to be used, the input pins (51 and 52) should be tied to ground.

6.2.2 ARC Configuration

The ADV7511's ARC receiver accepts single-ended or common mode signals and directs the resulting SPDIF signal to the SPDIF_OUT pin as 3.3V CMOS logic levels. This is illustrated in ►Figure 17. Refer to the *ADV7511 Programming Guide* for more details concerning the setup and operation of the ARC receiver. The HEAC signals should be routed from the HDMI connector as 100 ohm impedance differential traces, decoupled with a 1 μ F capacitor and terminated with a 50 ohm (+/-1%) resistor to 1.8V.

Figure 17 ARC Hardware Configuration



6.3 Output Connections

6.3.1 Output Formats Supported

The ADV7511 supports the following output formats:

- 36 or 30 bit RGB 4:4:4 (Deep Color)
- 24 bit RGB 4:4:4
- 36 or 30 bit YCbCr 4:4:4 (Deep Color)
- 24 bit YCbCr 4:4:4
- 24 bit YCbCr 4:2:2

6.3.2 TMDS Outputs

The three TMDS output data channels have signals which can run up to 2.25GHz. It is highly recommended to match the length of the traces in order to minimize the following:

- Intra-pair skew (skew between + and -)
- Inter-pair skew (skew between Channels 0, 1, and 2 and Clock)

The traces should also have a 50 Ohm transmission line impedance characteristic (100 Ohms differential). This is very important to avoid any reflections, thus outputting the best Eye Diagram. Also minimize the trace length as much as possible to minimize the resistance path. This is generally done by placing the ADV7511 close to the HDMI connector.

6.3.2.1 **ESD Protection**

In order to provide ESD protection to the TMDS differential pairs, it is recommended that low capacitance (<.6pF) varistors are used, such as the Panasonic EZAEG2A device. Please refer to ►[Figure 27](#) for connection of the varistors. These should be placed as close to the TMDS lines as possible.

6.3.2.2 **EMI Prevention**

If it is necessary to reduce the EMI emissions (predominantly at higher frequencies), we recommend use of common mode chokes placed in the TMDS lines as close to the ADV7511 as is possible. Two such options are the Murata DLW21SN670HQ2L (67 ohm) or DLW21SN900SHQ2 (90 ohm).

6.3.3 **Display Data Channel (DDC) pins**

The Display Data Channel (DDCSCL and DDCSDA) pins need to have the minimum amount of capacitance loading to ensure the best signal integrity. The DDCSCL and DDCSDA capacitance loading must be less than 50pF to meet the HDMI compliance specification. The DDCSCL and DDCSDA must be connected to the HDMI connector and a pull-up resistor to 5V is required. The pull-up resistor must have a value between 1.5K Ω and 2K Ω . The Enhanced Display Identification Data (EDID) EEPROM on the HDMI/DVI sink is expected to have an address of 0xA0. It is recommended to match the length of the DDCSCL and DDCSDA lines.

6.3.4 **Interrupt Output (INT)**

The ADV7511 provides the INT (interrupt) pin in order to enable an interrupt driven system design. The interrupt pin is an open drain output. It should be pulled to a logic high level (such as 1.8V or 3.3V depending on the high logic level of the microcontroller) through a resistor (2kOhm to 5kOhm). It should also be connected to the input of the system's microcontroller. Refer to the ADV7511 Programming Guide for additional information.

6.3.5 **PLL Circuit**

The phase-locked loop (PLL) generates the TMDS output clock as well as clocks used internally by the ADV7511 to serialize the data. The PLL filters high-frequency jitter components to minimize the output data clock jitter.

6.4 **Consumer Electronic Control (CEC)**

6.4.1 **Unused Inputs**

If the [CEC](#) function is not used, the CEC and CEC_CLK pins should be connected to ground.

6.4.2 **CEC Function**

The ADV7511 has a Consumer Electronic Control ([CEC](#)) receiver/transmitter function which captures and buffers three (3) command messages and passes them on to the host. CEC is a single-wire, bidirectional interface intended to facilitate the control of any device on an HDMI network, as typified in ► [Figure 18](#), with the remote control unit or on-device control buttons of any other device connected to the network. Defined as an optional feature in the HDMI

specification, it is based on the AV Link function defined in the European SCART (Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs) specification. ► [Table 19](#) describes some typical end-user CEC features.

Figure 18 Typical AII-HDMI Home Theatre

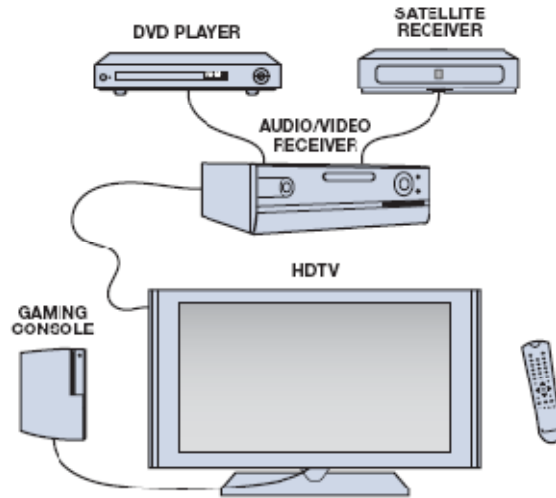


Table 19 Some useful “End-User” CEC Features:

Feature	Description
One-Touch Play	Pushing the “play” button commands a source to play and become the active video source for the TV.
Stand-By	Pushing the “power down” button of any active device commands all devices on the HDMI network to shut down.
One-Touch Record	Pushing the “record” button commands a recording device to power up and record the content currently displayed on the TV.

Many of these end-user features require sending multiple messages over the CEC bus such as “Active Source,” and “Routing Change,” which support the CEC feature “Routing Control.” This feature allows a device to play and become the active source by switching the TV’s source input. If the TV is displaying another source at the time this command is used, it may place the other source into “stand-by” mode, depending on the implementation.

6.5 Video Data Formatting

Following the Input Data Capture are the options for Color Space Conversion (CSC) and for formatting between 4:4:4 and 4:2:2. Taken together these can alter an input stream from: RGB to YCbCr (4:4:4 or 4:2:2), or YCbCr to RGB. Required video control signals such as Hsync, Vsync and Data Enable (DE) can be generated from different input formats and can be adjusted for optimum position.

6.5.1 DE, Hsync and Vsync Generation

When transmitting video data across the TMDS interface, it is necessary to have an Hsync, Vsync, and Data Enable (DE) defined for the image. There are three methods for sync input to the ADV7511. See ► Figure 19 for a block diagram of the sync processing capabilities.

Separate Hsync, Vsync, and DE

For this method, all necessary signals are provided so neither Sync generation nor DE generation is required. If desired, the user can adjust the Hsync and Vsync timing relative to DE (refer to Hsync and Vsync adjustment section). Also, the DE timing can be adjusted relative to Hsync and Vsync.

► Refer to the *ADV7511 Programming Guide* for details on how to adjust the DE and sync timing.

Embedded Syncs (SAV and EAV)

When embedded syncs are provided to the ADV7511 Hsync and Vsync need to be generated internally by the ADV7511 hardware. Registers 0x30 through 0x34 and 0x17[6:5] contain the settings for Hsync and Vsync generation in the embedded sync decoder section. The ADV7511 will use the signal generated by the EAV and SAV as the DE by default, but a new DE can also be generated. Sync adjustment is also available.

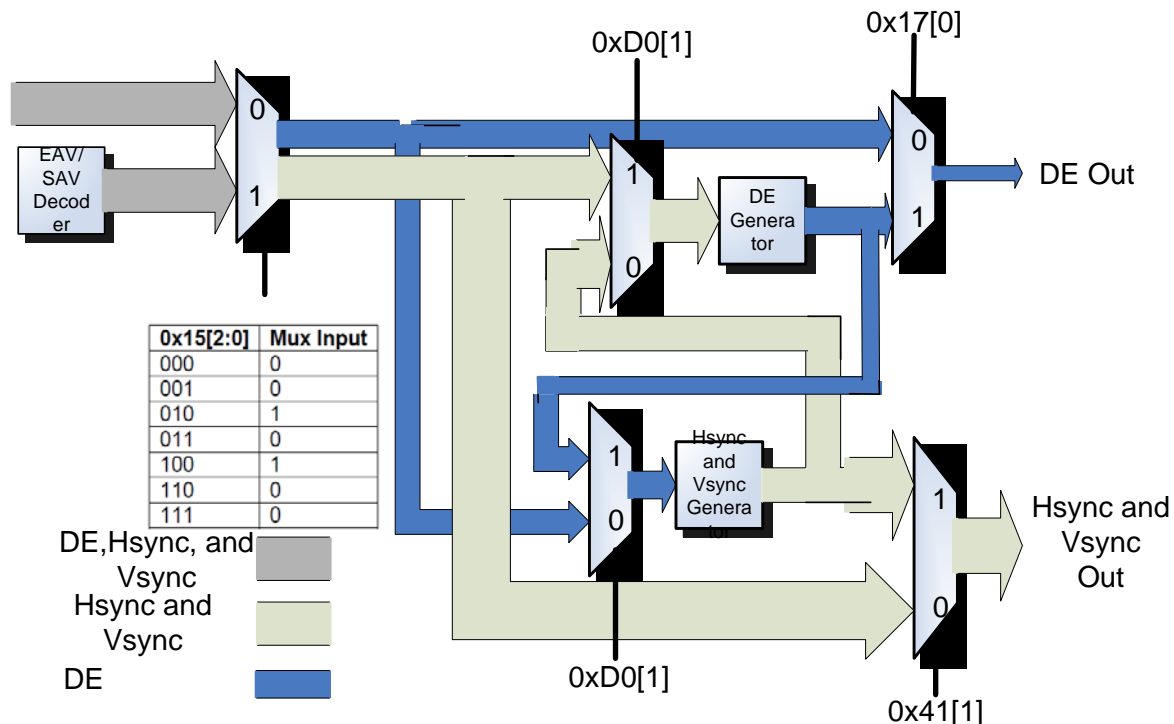
► Refer to the *ADV7511 Programming Guide* for details on how to program the DE and sync generator when embedded syncs are used.

Separate Hsync and Vsync only

This method requires that a DE be generated. Hsync and Vsync can also be adjusted based on the new DE if desired by enabling the Hsync and Vsync generation and setting the order to DE generation then Hsync Vsync Generation.

► Refer to the *ADV7511 Programming Guide* for details on how to generate DE based on the incoming sync signals.

Figure 19 Sync Processing Block Diagram



6.5.2 Color Space Conversion (CSC) Matrix

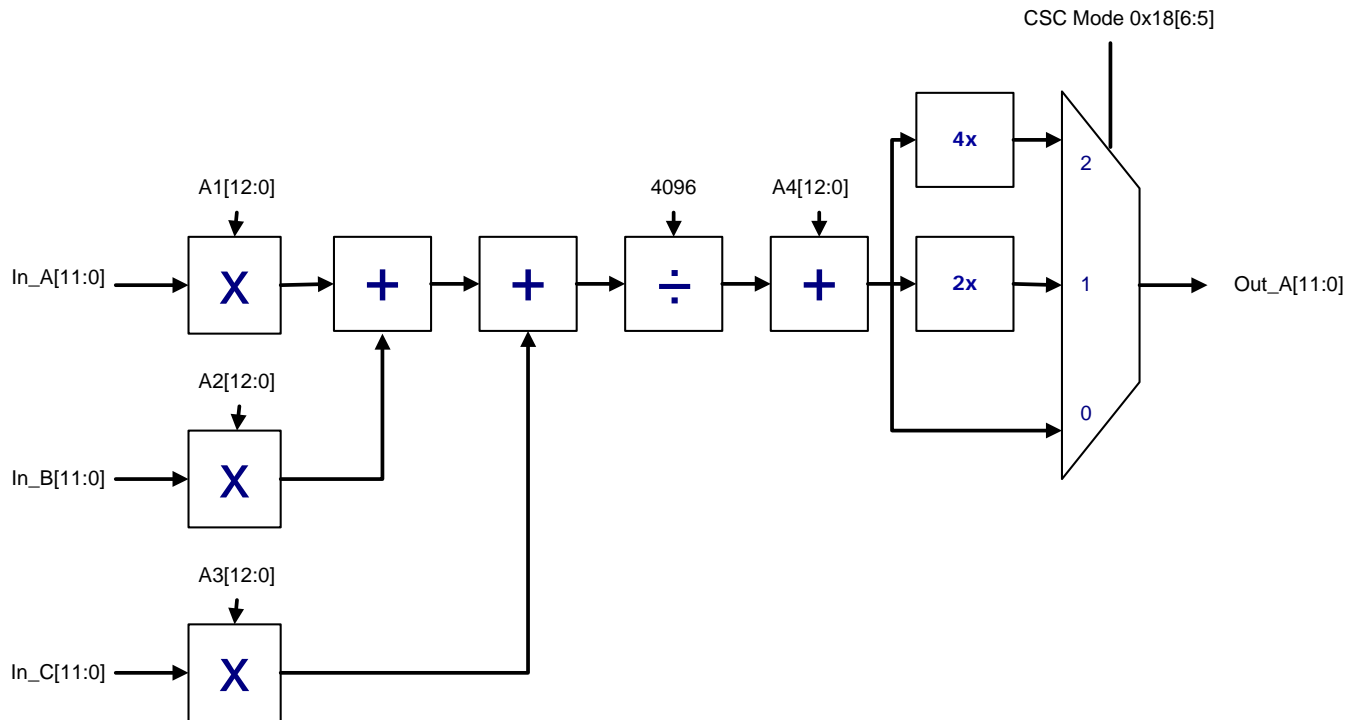
The Color Space Conversion (CSC) matrix in the ADV7511 consists of three identical processing channels (see ►Figure 20). In each channel, the three input values (R,G,B or Y,Cr,Cb - see ►Table 20) are multiplied by three separate coefficients. In each CSC channel, the order of input remains the same – Out_A will have the same input (In_A, In_B, In_C) as Out_B and Out_C. The coefficients will be different for each channel. Also included is an offset value for each row of the matrix and a scaling multiple for all values. Each coefficient is 13 bit 2's complement resolution to ensure the signal integrity is maintained. The CSC is designed to run at speeds up to 165Mhz, supporting resolutions up to 1080p at 60Hz and UXGA at 60Hz. With “any-to-any” color space support, formats such as RGB, YUV, YCbCr, and others are supported by the CSC.

► Please refer to the *ADV7511 Programming Guide* for more information about this block.

Table 20 Channel Assignment for Color Space Converter (CSC)

Input	RGB	YCrCb	Coefficients	Output
In_A	Red	Cr	A1,A2,A3,A4	Out_A
In_B	Green	Y		
In_C	Blue	Cb		
In_A	Red	Cr	B1.B2.B3.B4	Out_B
In_B	Green	Y		
In_C	Blue	Cb		
In_A	Red	Cr	C1,C2,C3,C4	Out_C
In_B	Green	Y		
In_C	Blue	Cb		

Figure 20 Single Channel of CSC (In_A)



6.5.3 4:2:2 to 4:4:4 and 4:4:4 to 4:2:2 Conversion Block

The 4:2:2 to 4:4:4 conversion block can convert 4:2:2 input signals into the 4:4:4 timing format. This is necessary, for instance, if the ADV7511 is set in **DVI** mode and has 4:2:2 format as its video input. The ADV7511 is also capable of performing 4:4:4 to 4:2:2 conversions.

▷ Please refer to Section 4.3.5 of the *ADV7511 Programming Guide* for more information about this block.

6.6 DDC Controller

The ADV7511 DDC Controller performs two main functions: support the system's EDID and handle HDCP.

- The ADV7511 has the ability to read and buffer the sink EDID (one segment of 256 bytes at a time) via the DDC lines. This feature eliminates the requirement for the source controller to interface directly to the sink.
- The ADV7511 DDC controller provides the path through which HDCP content protection authentication and communications occur. The ADV7511 has internal HDCP key storage (eliminating the need for an external EEPROM) and a built-in micro-controller to handle HDCP transmitter states, including handling down-stream HDCP repeaters. This provides content protection for video which prevents unauthorized digital copying. Refer to Section ▶ [6.8.2](#) for power consumption of HDCP.

▷ Please refer to Section 4.5 of the *ADV7511 Programming Guide* for more information about this block.

6.7 Inter-IC Communications (I2C)

6.7.1 Two-Wire Serial Control Port

The ADV7511's registers must be programmed through the SDA and SCL pins using the Inter IC (IIC or I2C) protocol. The SDA/SCL programming address is 0x72 or 0x7A based on whether the PD/AD pin is pulled high (I2C address = 0x7A) or pulled low (I2C address = 0x72). When initially powered up, there is a 200ms period before the device is ready to be addressed.

▷ The *ADV7511 Programming Guide* provides the information necessary for programming the transmitter.

Up to two ADV7511 devices can be connected to the two-wire serial interface, with a unique address for each device.

The two-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The ADV7511 interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal
- Acknowledge (Ack)

When the serial interface is inactive (SCL and SDA are high), communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a seven bit slave address (the first seven bits) and a single R/W bit (the eighth bit). The R/W bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the A2 input pin as shown in Table 21), the ADV7511 acknowledges by bringing SDA low on the 9th SCL pulse. If the addresses do not match, the ADV7511 does not acknowledge.

Table 21 Serial Port Addresses

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Hex Addr.
PD/AD pin Power-up state	A ₆ (MSB)	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	
0	0	1	1	1	0	0	1	0x72
1	0	1	1	1	1	0	1	0x7A

6.7.2 Data Transfer via I2C

For each byte of data read or written, the most significant bit (MSB) is the first bit of the sequence.

If the ADV7511 does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the ADV7511 during a read sequence, the ADV7511 interprets this as end of data. The SDA remains high, so the master can generate a stop signal.

Writing data to specific control registers of the ADV7511 requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations, however, it is reset after a STOP signal. The base address auto-increments by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address does not increment and remains at its maximum value. Any base address higher than the maximum value does not produce an acknowledge signal.

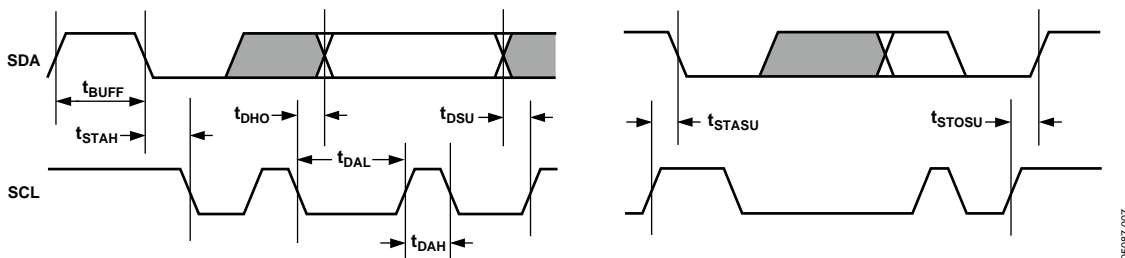
Data are read from the control registers of the ADV7511 in a similar manner. Reading requires two data transfer operations:

1. The base address must be written with the R/\overline{W} bit of the slave address byte low to set up a sequential read operation.
2. Reading (the R/\overline{W} bit of the slave address byte high) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the ADV7511, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high. As in the write sequence, a STOP signal resets the base address.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read/write) between the slave and master without releasing the serial interface lines.

Figure 21 Serial Port Read/Write Timing



6.7.3 Serial Interface Read/Write Examples

Write to one control register:

- Start signal
- Slave address byte (R/\overline{W} bit = low)
- Base address byte
- Data byte to base address
- Stop signal

Write to four consecutive control registers:

- Start signal
- Slave address byte (R/\overline{W} bit = LOW)
- Base address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

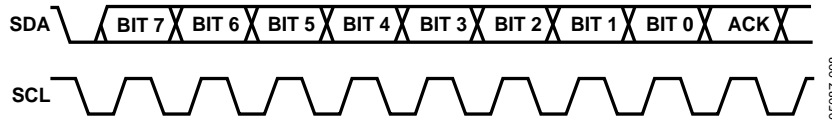
Read from one control register:

- Start signal
- Slave address byte (R/\overline{W} bit = low)
- Base address byte
- Start signal
- Slave address byte (R/\overline{W} bit = high)
- Data byte from base address
- Stop signal

Read from four consecutive control registers:

- Start signal
- Slave address byte (R/\overline{W} bit = low)
- Base address byte
- Start signal
- Slave address byte (R/\overline{W} bit = high)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

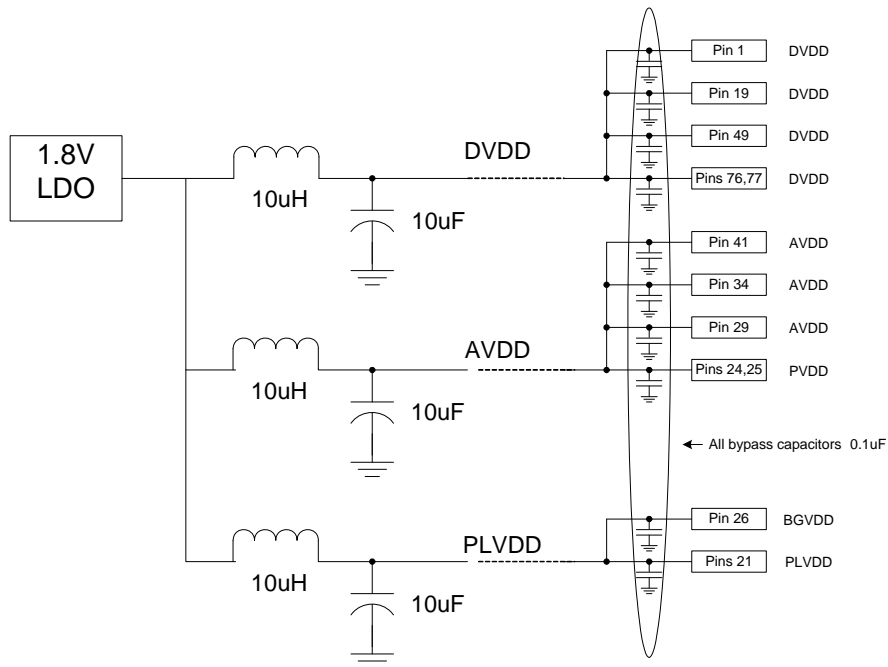
Figure 22 Serial Interface—Typical Byte Transfer



6.8 Power Domains

The AVDD, DVDD, PVDD, BGVDD and PLVDD power domains of the ADV7511 operate off of 1.8 volts. It is recommended that the ADV7511 has its own designated 1.8V linear regulator and that the AVDD, DVDD and PLVDD PCB power domains be segregated using inductors. More detailed recommendations for the PCB can be found in section ► [Section 7](#).

Figure 23 Power Supply Domains



6.8.1 Power Supply Sequencing

There is no required sequence for turning on or turning off the power domains; all should be fully powered up or down within 1 second of the others.

6.8.2 Power Consumption

The power consumption of the ADV7511 will vary depending upon: clock frequency, power supply domain voltages and which functional blocks are being used. In [Section 4](#): the specifications table lists the maximum power as 326mW at 1080p, CSC off. ► [Table 22](#) illustrates the maximum power consumed by individual circuits in the ADV7511. All of these entries are for worst case operations – 1080p output, and 192KHz audio sampling frequency. The SPDIF power

consumption is affected by use of an external or internal MCLK. The high power mode assumes an internally generated MCLK, while the low power mode uses an externally supplied MCLK.

Table 22 Maximum Power Consumption by Circuit – note these values will change after characterization

Functional Block	CSC	HDCP	CEC	SPDIF high power mode	SPDIF Low power mode
Max Power ¹	25mW	30mW	<1mW	40mW ²	10m W ³
Typical Power	16mW	25mW	<1mW		

1. At 1080p video resolution
2. At 192KHz audio sampling rate
3. At 32KHz audio sampling rate

SECTION 7: PCB LAYOUT RECOMMENDATIONS

7.1 Power Supply Filtering

All of the ADV7511 supply domains are 1.8V with the exception of MVDD which is 3.3V and need to remain as noise-free as possible for the best operation. Power supply noise has a frequency component that affects performance, and this is specified in V_{rms} terms. ▶Figure 24 shows the maximum allowable noise for the AVDD and PLVDD supply domains in the ADV7511. The noise limit for all other supply domains are listed in ▶Table 1.

It is recommended to combine the five 1.8 volt power domains of the ADV7511 into 3 separate PCB power domains as shown in ▶Figure 23. An LC filter on the output of the power supply is recommended to attenuate the noise and should be placed as close to the ADV7511 as possible. An effective LC filter for this is a 10 μ H inductor and a 10 μ F capacitor (see▶ Figure 23). This filter scheme will reduce any noise component over 20KHz to effectively 0. Using the recommended LC filter with realistic load and series resistance yields the transfer curve shown in Figure 25.

Each of the power supply pins of the ADV7511 should also have a 0.1 μ F capacitor connected to the ground plane as shown in ▶Figure 23. The capacitor should be placed as close to the supply pin as possible. Adjacent power pins can share a bypass capacitor. The ground pins of the ADV7511 should be connected to the GND plane using vias.

Figure 24 AVDD and PLVDD Max Noise vs. Frequency

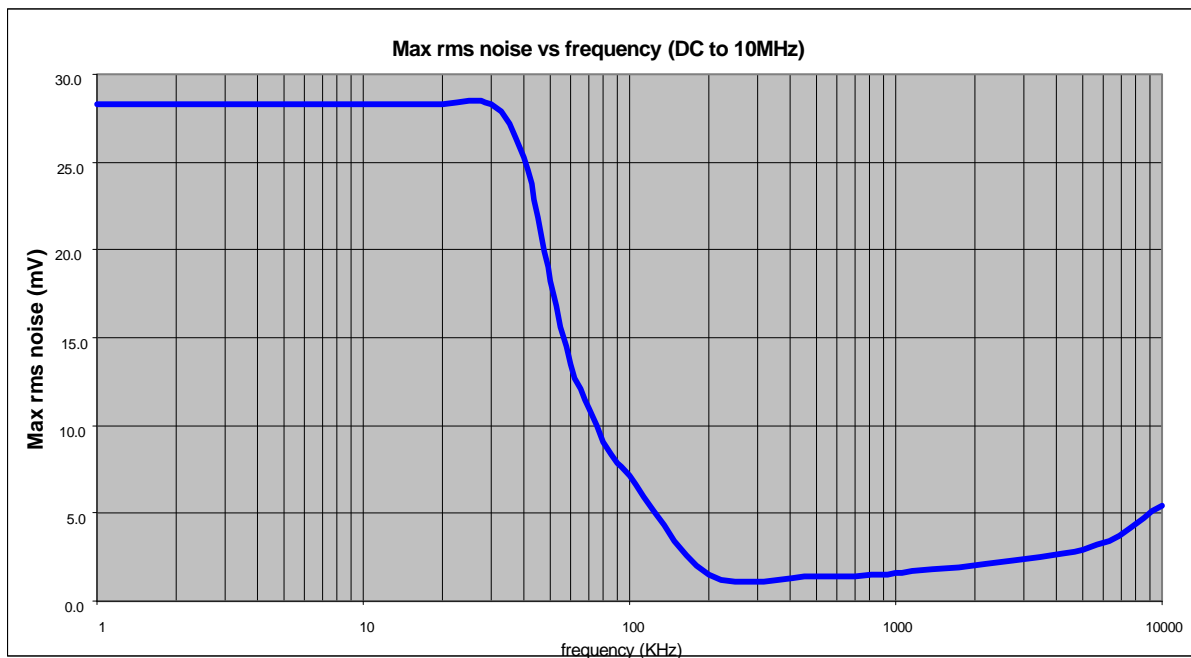
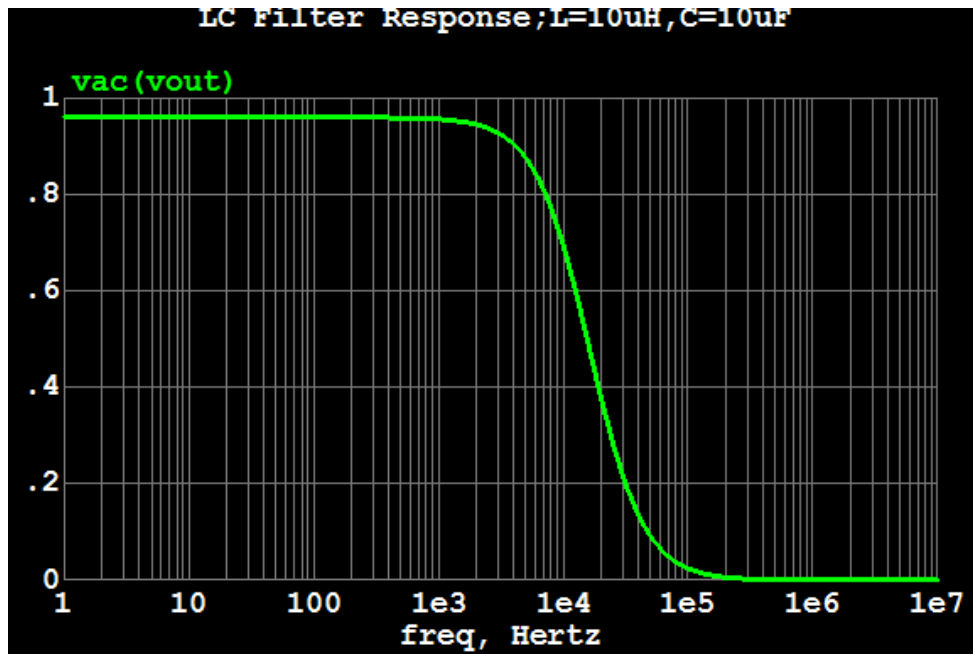


Figure 25 LC Filter Transfer Curve



7.2 Video Clock and Data Inputs

Any noise that is coupled onto the CLK input trace will add jitter to the system. It is recommended to control the impedance of the CLK trace. If possible, using a solid ground or supply reference under the trace is a good way to ensure the impedance remains constant over the entire length of the trace. Therefore, minimize the video input data clock (pin 79) trace length and do not run any digital or other high frequency traces near it. Make sure to match the length of the input data signals to optimize data capture especially for Double Data Rate (DDR) input formats.

7.3 Audio Clock and Data Inputs

The length of the input audio data signals should be matched as closely as possible to optimize audio data capture. It is recommended to add series 50Ω resistors (+/-5%) as close as possible to the source of the audio data and clock signals to minimize impedance mismatch.

7.4 SDA and SCL

The SDA and SCL pins should be connected to an I2C Master. A pull-up resistor of 2KΩ (+/-5%) to 1.8V or 3.3V is recommended for each of these signals. See Figure 27.

7.5 DDCSDA and DDCSCL

The DDCSDA and DDCSCL pins should be connected to the HDMI connector. A pull-up resistor of 1.5KΩ to 2KΩ (+/-5%) to HDMI +5V is required for each of these signals. See Figure 27.

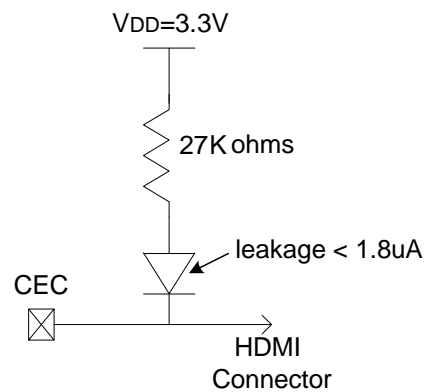
7.6 Current Reference Pin: R_EXT

The external reference resistor should be connected between the R_EXT pin and ground with as short a trace as possible. The external reference resistor must have a value of 887 Ohms (+/-1% tolerance). It is strongly recommended to avoid running any high-speed AC or noisy signals next to the R_EXT line or close to it. Specifically it is recommended that no switching signals – such as LRCLK (including vias) be routed close to the R_EXT pin (28). Low-level TMDS switching noise should have minimal impact on R_EXT.

7.7 CEC Implementation

An external clock is required to drive the CEC_CLK input pin. Default frequency is 12MHz, but any clock between 3 and 100MHz (+/-2%) can be used. ▶[Figure 26](#) illustrates the recommended connection to the CEC line.

Figure 26 CEC external connection

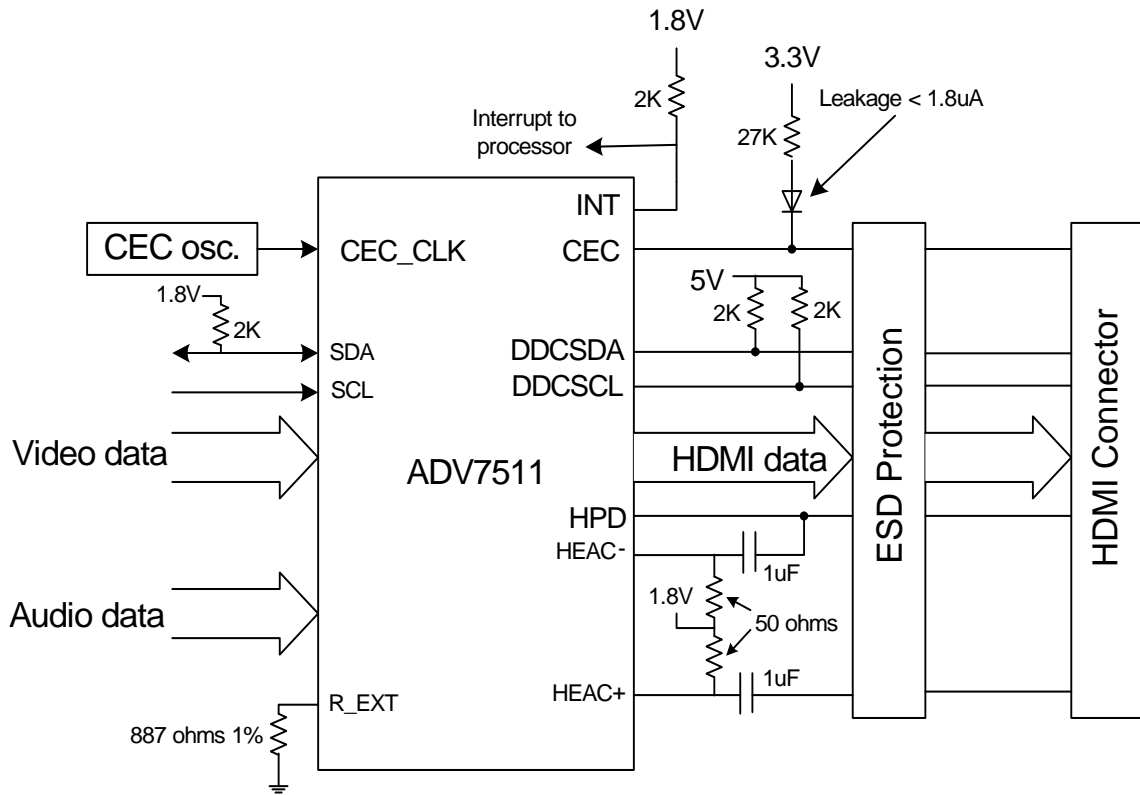


An example schematic is shown in [Figure 27](#). For a complete set of reference schematics and PCB layout example, contact ATV_VideoTX_apps@analog.com.

7.8 HEAC (ARC)

Please refer to [Figure 17](#) for the recommended interface to the HEAC+ and HEAC- pins.

Figure 27 Example Schematic



SECTION 8: GLOSSARY

480i, 480p, 576i, 576p, 720p, 1080i, 1080p	Common video modes. ▷ Refer to CEA-861D for more information.
VGA, SVGA, XGA, SXGA, UXGA	Common graphics modes. ▷ Refer to VESA.org for more information.
ARC	Audio Return Channel
CEC	Consumer Electronics Control is used to unify remotes of differing make to perform a given task with one-button- touch.
CSC	Colorspace Convert is used to convert RGB to YCbCr or YCbCr to RGB . Adjustments can be factored in for differing ranges.
DDC	Display Data Channel is used to communicate between to the source and sink to determine sink capabilities. It is also used as the HDCP key communications channel.
DDR	Double Data Rate clocks capture data on both the rising and falling edge of the clock.
Deep Color	Deep Color™ is a feature of HDMI v.1.3 in which pixel color depths for 444 signals can be greater the 8 bits. Options exist for 10, 12, and 16 bits.
DSD	Direct Stream Digital audio is transmitted in a one-bit delta sigma audio stream.
DST	Direct Stream Transfer is a lossless compression technique for DSD audio
DVI	Digital Visual Interface - uses TMDS to transmit RGB signals.
EDID	Enhanced Display Identification Data is used to store monitor (sink) capabilities in an EEPROM.
HBR	High Bit-Rate audio is used to define sample rates greater than 192Kbits.
HDCP	High-bandwidth Digital Content Protection is a method of protecting content from unauthorized digital copying.
HDMI	High Definition Multimedia Interface is composed of three TMDS differential data channels and one differential clock channel. It is defined to include video streams up to 3.7Gbps as well as audio.
HEAC	HDMI Ethernet and Audio return Channel
HPD	The Hot Plug Detect pin is an input which detects if a DVI or HDMI sink is connected.
I2C, IIC	Inter-IC Communications is a Philips two-wire serial bus for low-speed (up to 400kHz) data.
I2S	Inter-IC Sound is a serial Philips bus designed specifically for audio.
LPCM	Linear Pulse-Code Modulation is a method of encoding audio samples.
LQFP	Low-Profile Quad Flat Pack is the type of package for the ADV7511.
NDA	Non-Disclosure Agreement is used to assure confidentiality of intellectual property.
PLL	Phase-Locked Loop.
RGB	Red Green Blue is the standard definition for three-color graphics and video.
SPDIF	Sony / Philips Digital Interface is a method of presenting audio data in a serial stream.

TMDS	Transition Minimized Differential Signaling is the format used by the three data channels in HDMI . This encodes 8 bits into 10 and serializes them.
x.v.Color™	This is feature of HDMI v.1.3 in which the color gamut may be extended or altered beyond the normal range in order to accommodate a given sink.
YCbCr	This is a common color format for video where the 'Y' component is luminance and the Cr and Cb signals are color difference signals. 4:4:4 defines a Y, Cr, and Cb for each pixel; 4:2:2 defines a Y for each pixel and a sharing of Cr and Cb between 2 sequential pixels. In this manner, compression of 33% is possible.

¹C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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