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Evaluating the ADRF6720, a Wideband Quadrature Modulator with Integrated Fractional-N PLL and VCOs

FEATURES

Full-featured evaluation board for the ADRF6720
On-board USB for SPI control
3.3 V operation
C# software interface for serial port control

EVALUATION KIT CONTENTS

ADRF6720 evaluation board
USB cable

EQUIPMENT NEEDED

Analog signal sources and signal analyzer
Power supplies (5 V/1 A)
PC running Windows® 98 , Windows 2000, Windows ME, Windows XP, Windows Vista, or Windows 7
USB 2.0 port, recommended (USB 1.1 compatible)

SOFTWARE NEEDED

ADRF6720 control software

GENERAL DESCRIPTION

The ADRF6720 is a wideband quadrature modulator with an integrated synthesizer ideally suited for 3G and 4G communication systems. The ADRF6720 consists of a high linearity broadband modulator, an integrated fractional-N phase-locked loop (PLL), and four low phase noise multicore voltage controlled oscillators (VCOs).

The ADRF6720 LO signal can be generated internally via the on-chip integer-N and fractional-N synthesizers, or externally via a high frequency, low phase noise LO signal. The internal integrated synthesizer enables LO coverage from 356.25 MHz to 2855 MHz using the multi-core VCOs. In the case of internal LO generation or external LO input, quadrature signals are generated with a divide-by-2 phase splitter. When the ADRF6720 is operated with an external 1 × LO input, a polyphase filter generates the quadrature inputs to the mixer.

The ADRF6720 offers digital programmability for carrier feedthrough optimization, sideband suppression, HD3/IP3 optimization, and high-side or low-side LO injection.

The ADRF6720 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 40 pin, RoHS-compliant, 6 mm × 6 mm LFCSP package with an exposed paddle. This user guide describes the evaluation board for the ADRF6720, which provides all of the support circuitry required to operate the ADRF6720 in its various configurations and the application software used to interface with the device.

The ADRF6720 data sheet, which provides additional information, should be consulted when working with this evaluation board.

TYPICAL SETUP

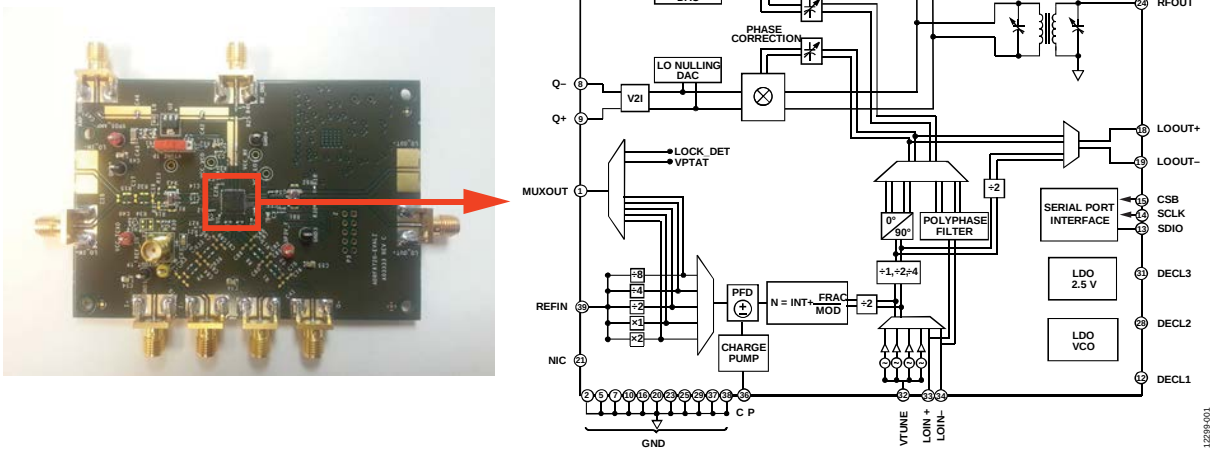

Figure 1.

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REVISION HISTORY

5/14—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

INTRODUCTION

The ADRF6720 evaluation board provides all of the support circuitry required to operate the ADRF6720 in its various modes and configurations. Figure 2 shows the typical bench setup used to evaluate the performance of the ADRF6720.

POWER SUPPLY

The ADRF6720 evaluation board requires a 3.3 V power supply. Connect the 3.3 V power terminals as like Figure 2.

BASEBAND INPUTS

Drive the baseband inputs (I+, I−, Q+, and Q−) from a differential source. Place a shunt 125 Ω external resistor across the I and Q inputs to match the differential 100 Ω impedance interface. The nominal drive level used in the evaluation of the ADRF6720 is 1 V p-p differential (or 500 mV p-p on each pin). All the baseband inputs must be externally dc biased at 0.5 V.

LO INPUT/OUTPUT

The ADRF6720 offers two alternatives for generating the differential LO input signal: externally via a high frequency low phase noise LO signal or internally via the on-chip fractional-N synthesizer. In either case, the differential LO signal can be routed off chip to the SMA connector labeled LO_OUT+ and LO_OUT−.

For internal LO configuration using the on-chip fractional-N synthesizer, apply a low phase noise reference signal to the REFIN connector. The PLL reference input can support a wide frequency range since the divide or multiplication blocks can be used to increase or decrease the reference frequency to the desired value before it is passed to the phase frequency detector (PFD). The integrated synthesizer enables continuous LO coverage from 356.25 MHz to 2855 MHz.

For optimum performance using an external LO source, drive the LO inputs LOIN and LOIP differentially. The ADRF6720 evaluation board integrates footprints for both the Mini-Circuits TC1-1-43A+ balun and the Johanson 2500BL14M050T to satisfy the wide input frequency range of the external LO inputs. Unless an ac-coupled balun/transformer is used to generate the differential LO, the inputs must be ac-coupled. The input impedance of the differential LO signals is 50 Ω.

RF (MODULATOR) OUTPUT

The RF output is available at the RF_OUT SMA connector, which can drive a 50 Ω load.

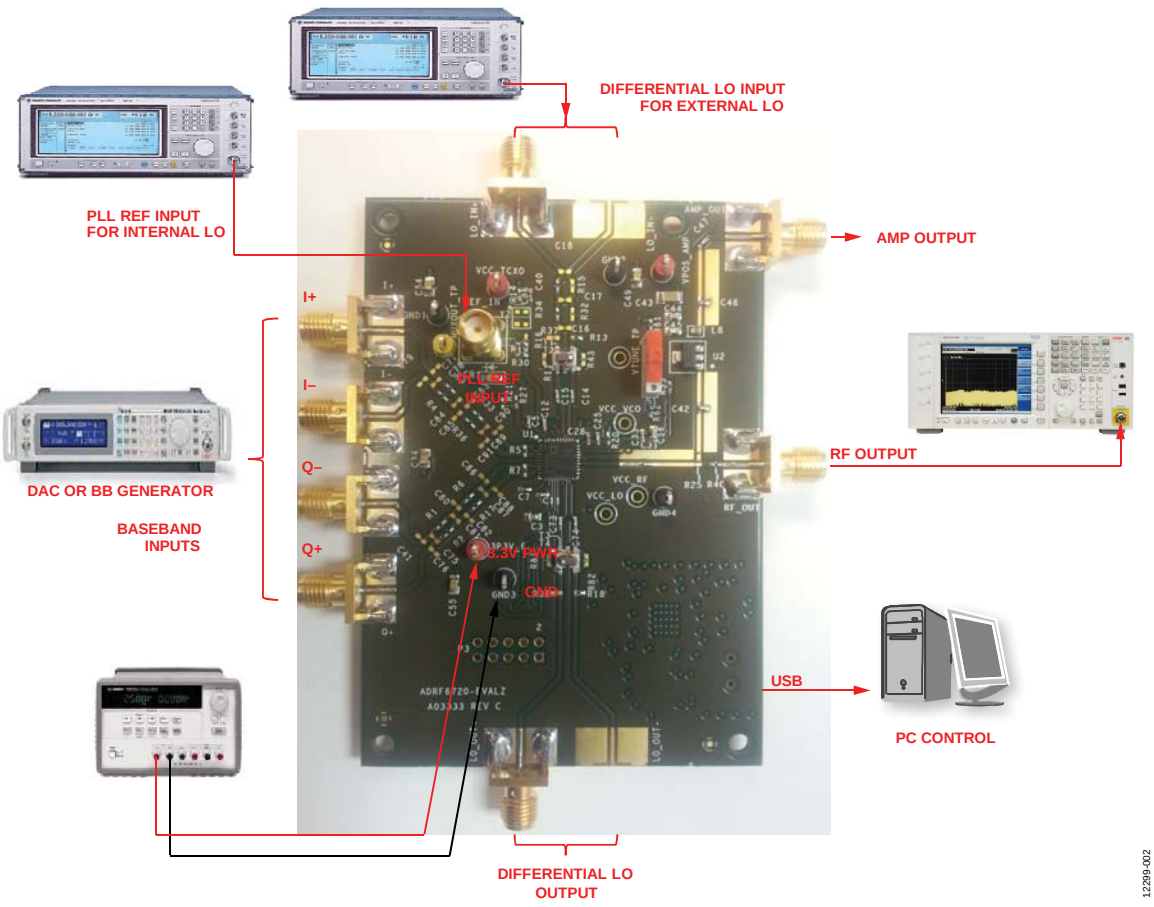

Figure 2. ADRF6720 Typical Measurement Setup

EVALUATION BOARD CONTROL SOFTWARE

The ADRF6720 evaluation board is configured with a USB friendly interface to allow programmability of the ADRF6720 registers.

INSTALLING EVALUATION SOFTWARE AND THE DRIVER

The following instructions describe how to install the ADRF6720 control software, as well as the Cypress Generic USB driver, onto a Windows computer running either a 32 or 64-bit operating system. Install the necessary software before plugging the USB cable to the computer. (The following instructions are specific for Windows XP, Windows Vista, and Windows 7. However, the software is compatible with Windows 98, Windows 2000, and Windows ME.)

1. Extract the **ADRF6720_Control_SW_Rev0_0_3.zip** file.
2. Next, run the file **ADRF6720_Rev0_0_3_install.exe** from the extracted .zip file. An icon should appear on your desktop with the Analog Devices, Inc., logo, titled **ADRF6720_Rev0_0_3**.
3. Once the installer is finished, install the USB driver. Plug the RFG USB adapter into the PC using a USB cable.
4. In Windows XP, right click **My Computer** and select **Properties** > **Device Manager**. Then select the **Hardware** tab and **Device Manager**.
   In Windows Vista, right click **My Computer** and select **Device Manager**.
   In Windows 7, select **Device Manager**.
5. In **Device Manager**, select the last category, **Universal Serial Bus Controllers**. There will be an entry that either has a yellow flag on it (for unknown device) or is labeled **ADF4xxx USB Driver** (if you have installed the previous ADRF6x0x or Analog Devices, Inc., Limerick PLL software). Right click this device and select **update driver**. Browse to select the directory where you unzip. Click **Next** to complete the driver installation successfully.
   In Windows 7, install the USB signed driver. Run **ADI_RFG_Drivers_Win7.exe** in the attached zip file. Windows 7 will then recognize the CyUSB driver as a signed driver.

USING ADRF6720 EVALUATION SOFTWARE

The ADRF6720 evaluation software offers a block diagram view of how the registers affect the major functional blocks of the ADRF6720. The main screen of the evaluation software is shown in Figure 3. Table 1 shows the functionality of the software main screen.

Before reading or writing to the registers, validate the USB connection by reading the USB indicators at the lower left corner of the software. The **DUT to GUI** button reads the register values from the device and updates the user interface. An automatic write to the chip is initiated every time a register value is changed from the user interface.

The PLL synthesizer blocks have some behind the scenes calculations where the user only needs to specify the PLL reference and desired LO frequency and the software calculates and sets the INT, FRAC, and MOD values accordingly. The green boxes require user input while the yellow boxes are read only.

The **Engineering** tab as shown in Figure 4 allows specific reads and writes to the individual registers. The address and data fields must be input in decimal format.

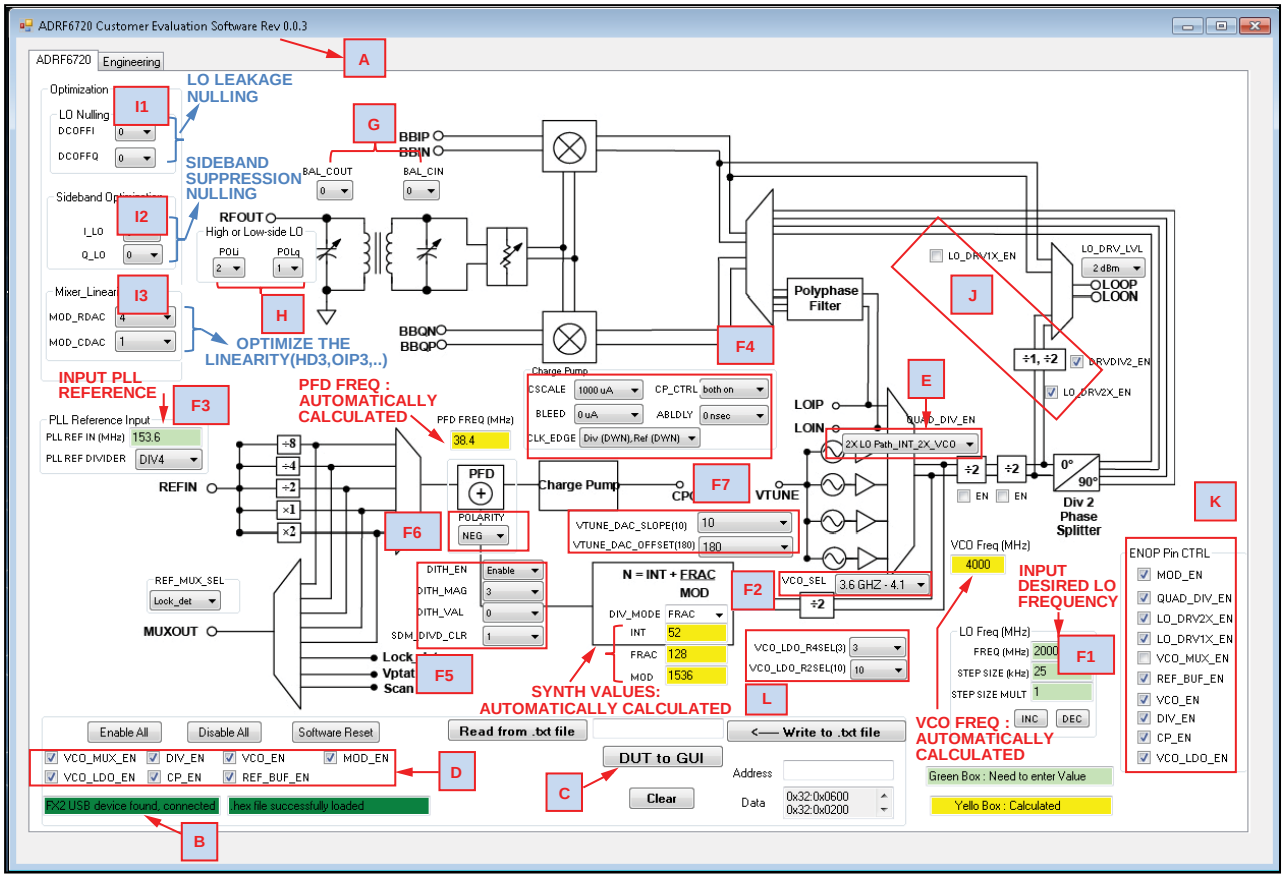

Figure 3. Main Screen of the ADRF6720 Control Software

Table 1. Main Screen Functionality

Label	Function
A	Shows software version.
B	When the USB driver is installed and USB block works correctly, it shows **FX2 USB device found, connected**.
C	**DUT to GUI** button.
D	Set automatically according to Label E selection. External LO: Check **MOD_EN** and uncheck **VCO_LDO_EN**, **CP_EN**, **REF_BUF_EN**, and **VCO_EN**. However, it is okay to enable all. Internal LO: Click **Enable All** to enable all blocks related to internal LO.
E	Sets LO path. External LO: Set to **1XLO Path_EXT_1X_LO** for **Polyphase Filter Path** in quadrature LO generation. Set to **2XLO Path_EXT_2X_LO** with **2× External LO for Div 2 Phase Splitter Path** in quadrature LO generation. Internal LO: Set it at **2XLO Path_INT_2X_VCO** for **Div 2 Phase Splitter Path** in quadrature LO generation Set it at **1XLO Path_INT_1X_VCO** for **Polyphase Filter Path** in quadrature LO generation
F1 to F7	Internal LO related. F1: Sets frequency and step size; press the **Enter** key to update. F2: VCO_SEL and VCO frequency are set up automatically by setting Label F1. VCO frequency is 2× to LO frequency. F3: Sets the PLL reference input and divider; ensures PFD frequency at the 11.4 MHz to 40 MHz. (It can be locked above 40 MHz.) F4: Used to optimize internal LO but not usually necessary to tune. F5: Used to optimize spur performance. F6: Selects **NEG**. F7: Fine tune control of the VTUNE temperature profile. Set VTUNE_DAC_SLOPE to 10 and VTUNE_DAC_OFFSET to 180.
G	Set tunable balun over a frequency band (see Table 2).
H	Set POLi and POLq to control setting for wanted signal at upper side or lower side to LO. POLi = POLq: Low-side LO injection when Q leads I POLi ≠ POLq: High-side LO injection when Q leads I

Label	Function
I	LO leakage, sideband suppression, linearity optimization. I1: DCOFFI, DCOFFQ: control setting for LO leakage nulling. I2: I_LO, Q_LO: control setting for sideband suppression nulling. I3: MOD_RDAC, MOD_CDAC: optimize the linearity (harmonics, IMD) performance.
J	Selects LO output path. LO_DRV1X_EN: Enables 1 × LO output path (after the quadrature divider) and enables LO output driver. LO_DRV2X_EN: Enables 2 × LO output path (before the quadrature divider) and enables LO output driver. DRVDIV2_EN :Select either 2× or 1× the frequency of the LO on 2 × LO output path
K	ENOP MASK: enable/disable individual blocks.
L	Programmable resistors for VCO LDO, set VCO_LDO_R4SEL(3) to 3 and for VCO_LDO_R2SEL(10) to 10.

Table 2. Balun Settings

BAL_CIN	BAL_COUT	Frequency Range (MHz)
0	0	$F_{RF} > 1730$
1	0	$1550 < F_{RF} < 1730$
2	0	$1380 < F_{RF} < 1550$
3	0	$1250 < F_{RF} < 1380$
4	0	$1170 < F_{RF} < 1250$
8	0	$1100 < F_{RF} < 1170$
9	0	$1020 < F_{RF} < 1100$
10	0	$970 < F_{RF} < 1020$
11	0	$930 < F_{RF} < 970$
12	0	$890 < F_{RF} < 930$
13	0	$840 < F_{RF} < 890$
14	0	$820 < F_{RF} < 840$
15	0	$740 < F_{RF} < 820$
15	3	$680 < F_{RF} < 740$

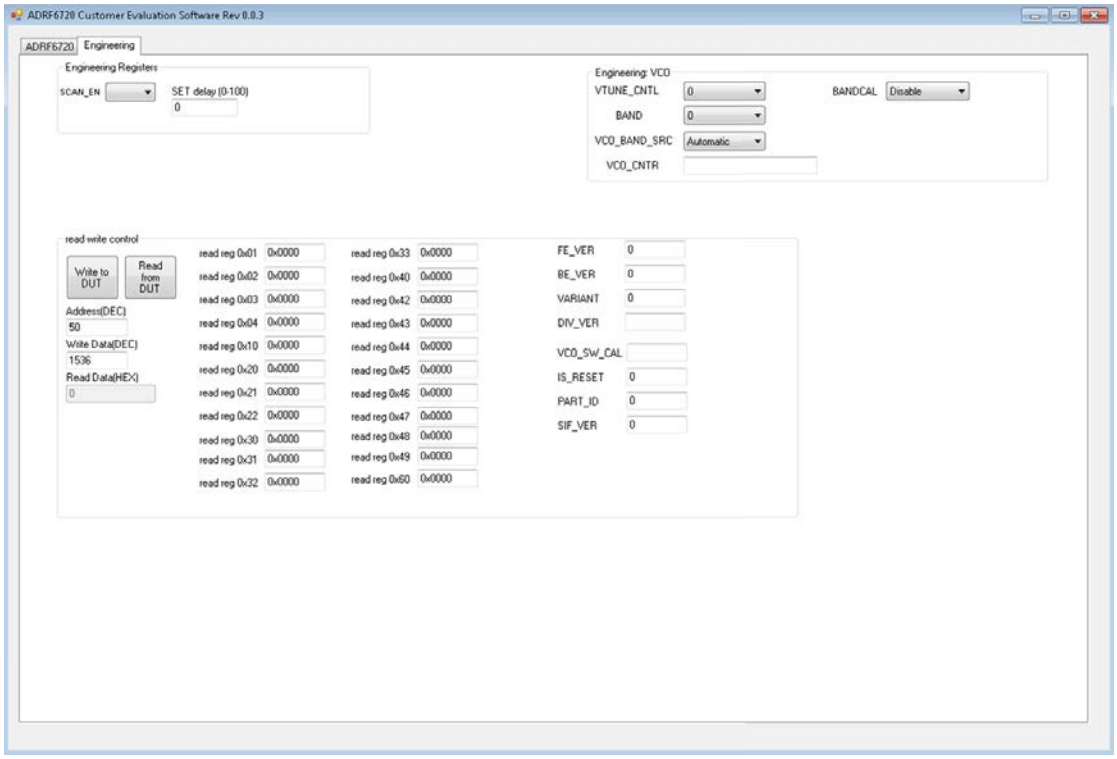

Figure 4. Engineering Tab of the ADRF6720 Control Software

SCHEMATICS AND ARTWORK

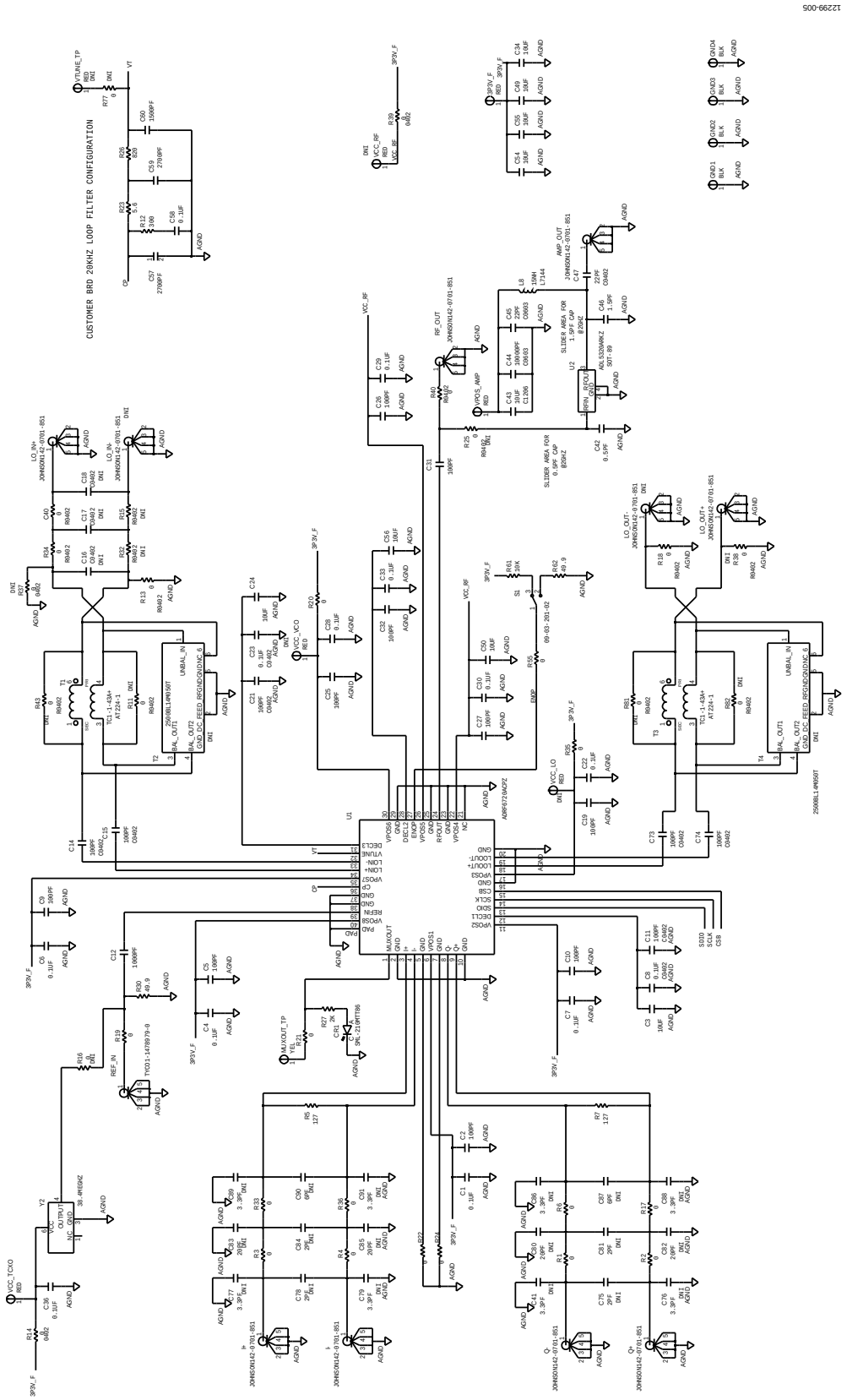

Figure 5. Evaluation Board Schematic

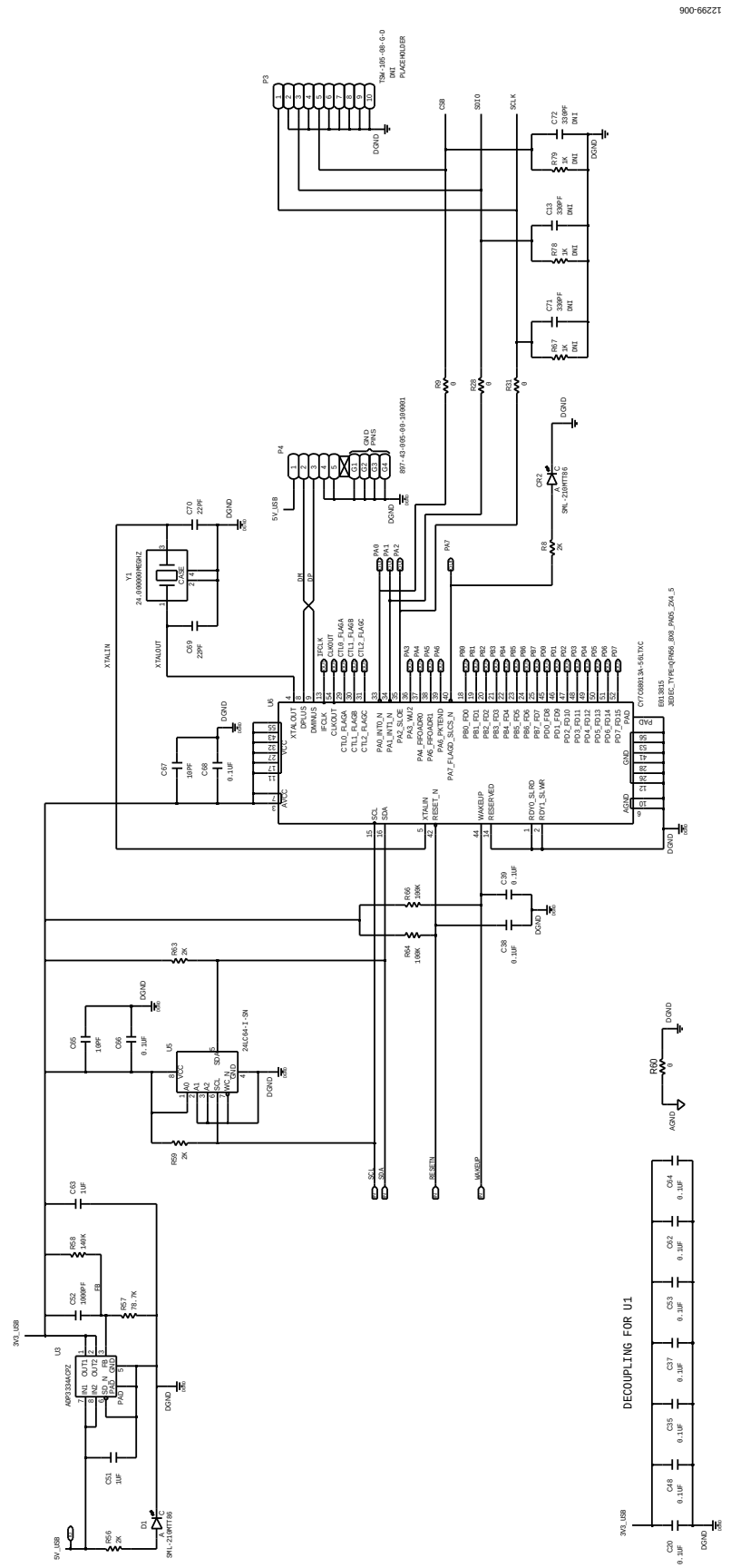

Figure 6. USB Interface Circuitry on the Customer Evaluation Board

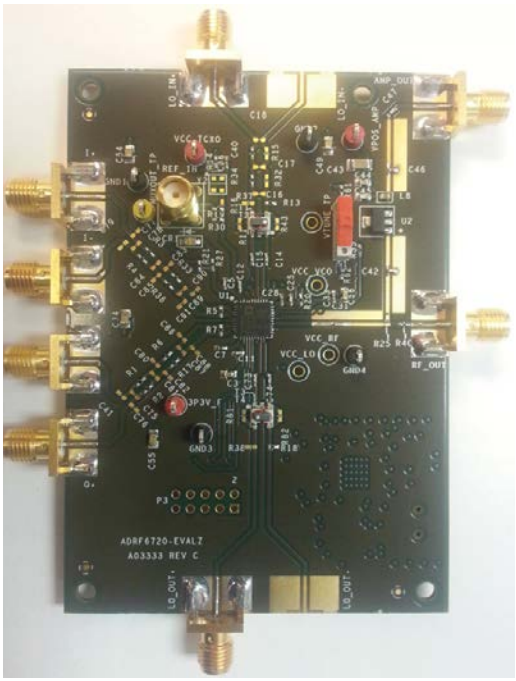

Figure 7. ADRF6720 Evaluation Board Top

Figure 8. ADRF6720 Evaluation Board Bottom

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Qty	Reference Designator	Description	Manufacturer	Part Number
1		PCB (see Table 4)	Analog Devices Supplied	08-20_a03333c
3	3P3V_F, VCC_TCXO, VPOS_AMP	Connector PCB test point red	Components Corporation	TP-104-01-02
4	GND1 to GND4	Connector PCB test point black	Components Corporation	TP-104-01-00
1	MUXOUT_TP	Connector PCB test point yellow	Components Corporation	TP-104-01-04
1	P4	Conn-PCB RECEPT mini-USB Type B SMT	Mill-Max	897-43-005-00-100001
8	I+, I–, Q+, Q–, LO_IN+, RF_OUT, AMP_OUT, LO_OUT+	Conn-PCB COAX SMA end launch	Johnson	142-0701-851
1	REF_IN	Conn-PCB SMA ST	Tyco	1-1478979-0
23	C1, C4, C6 to C8, C20, C22, C23, C28 to C30, C33, C35 to C39, C48, C53, C62, C64, C66, C68	Cap cer X7R C0402, 10%, 16 V 0.1 µF	Murata	GRM155R71C104KA88D
16	C2, C5, C9 to C11, C14, C15, C19, C21, C25 to C27, C31, C32, C73, C74	Cap chip mono cer C0G C0402, 5%, 50 V 100 pF	Murata	GRM1555C1H101JD01D
1	C12	Cap cer C0G C0402, 5%, 50 V 1000 pF	Murata	GRM1555C1H102JA01
4	C3, C24, C50, C56	Cap cer X5R C0603, 20%, 6.3 V 10 µF	Murata	GRM188R60J106ME47D
4	C34, C49, C54, C55	Cap cer monolithic X5R, C0805, 10%, 16 V 10 µF	Murata	GRM21BR61C106KE15L
1	C42	Cap cer C0G, C0402, ±0.5 pF, 25 V 0.5 pF	Kemet	C0402C508D3GACTU
1	C43	Cap cer monolithic X5R, C1206, 10%, 25 V 10 µF	Murata	GRM31CR61E106KA12L
1	C44	Cap monolithic cer X7R, C0603, 10%, 25 V 10000 pF	Murata	GRM188R71E103KA01D
3	C45, C69, C70	Cap cer NP0, C0603, 5%, 50 V 22 PF	Phycomp (Yageo)	CC0603JRNP09BN220
1	C46	Cap cer C0402, 0.25PF, 50 V 1.5 PF	Phycomp (Yageo)	0402CG159C9B200
1	C47	Cap cer C0402, 5%, 50 V 22 PF	Phycomp (Yageo)	0402CG220J9B200
2	C51, C63	Cap mono cer X5R, C0603, 10%, 25 V 1 µF	Murata	GRM188R61E105KA12D
1	C52	Cap cer C0G, C0603, 5%, 100 V 1000 pF	TDK	C1608C0G2A102J
2	C57, C59	Cap cer X7R, C0402, 5%, 50 V 2700 pF	Murata	GRM155R71H272JA01
1	C58	Cap cer X7R, C0603, 5%, 50 V 0.1 µF	Murata	GRM188R71H104JA93D
1	C60	Cap cer X7R, C0402, 5%, 50 V 1500 pF	Murata	GRM155R71H152JA01
2	C65, C67	Cap cer multilayer NP0, C0402, 5%, 50 V 10 pF	Phycomp (Yageo)	CC0402JRNP09BN100
1	L8	Chip inductor L7144, 5% 15 nH	Coilcraft	0603CS-15NXJLU
24	R1 to R4, R6, R9, C40, R13, R14, R17 to R21, R28, R31, R33 to R36, R39, R40, R55, R60	Res film SMD R0402, 5%, 1/16 W 0 Ω	Panasonic	ERJ-2GE0R00X
1	R12	Res film SMD R0402, 5%, 1/16 W 300 Ω	Panasonic	ERJ-2GEJ301X
2	R22, R24	Res film SMD R0603, 1%, 1/16 W 0 Ω	Multicomp	MC0603WG00000T5E-TC
1	R23	Res thick film chip, R0402, 5%, 1/10 W 5.6 Ω	Panasonic	ERJ-2GEJ5R6X
1	R26	Res film SMD R0402, 5%, 1/16 W 820 Ω	Panasonic	ERJ-2GEJ821X
1	R27	Res chip SMD R0402, 5%, 1/16 W 2 kΩ	Yageo	RC0402JR-072KL
1	R30	Res ultra-PREC ultra-reliability MF chip R0402, 0.1%, 1/16 W 49.9 Ω	SUSUMU	RG1005P-49R9-B-T5
2	R5, R7	Res prec thick film chip R0402, 1%, 1/10 W 127 Ω	Panasonic	ERJ-2RKF1270X
4	R8, R56, R59, R63	Res film SMD R0603, 1%, 1/10 W 2 kΩ	Yageo-Phycomp	9C06031A2001FKHFT
1	R57	Res prec thick film chip R0603, 1%, 50 V, 1/10 W 78.7 kΩ	Panasonic	ERJ-3EKF7872V

Qty	Reference Designator	Description	Manufacturer	Part Number
1	R58	Res prec thick film chip R0603, 1%, 50 V, 1/10 W 140 kΩ	Panasonic	ERJ-3EKF1403V
1	R61	Res prec thick film chip R0402, 1%, 1/16 W 10 kΩ	Panasonic	ERJ-2RKF1002X
1	R62	Res prec thick film chip R0402, 1%, 1/16 W 49.9 Ω	Panasonic	ERJ-2RKF49R9X
2	R64, R66	Res PREC thick film chip R0603, 1%, 50 V, 1/10 W 100 kΩ	Panasonic	ERJ-3EKF1003V
1	S1	SW PCB mount slide, SWSECMA0903201	SECMA	09-03-201-02
3	D1, CR1, CR2	LED 570 NM WTR clr LED0805 SMD (green)	ROHM	SML-210MTT86
2	T1, T3	XFMR RF SMT AT224-1	Mini-Circuits	TC1-1-43A+
1	U1	IC-ADI wideband quadrature MOD QFN40_6X6_PAD4_6X4_6	Analog Devices, Inc.	ADRF6720ACPZ
1	U2	IC-ADI 400MHZ-2700MHZ driver RF amp SOT-89, 5 V	Analog Devices, Inc.	ADL5320ARKZ
1	U3	IC-ADI high ACC. low IQ ADJ low drop reg QFN8_3X3_PAD1_75X1_45	Analog Devices, Inc.	ADP3334ACPZ
1	U5	IC 64KBIT EEPROM, SO8	Microchip	24LC64-I-SN
1	U6	IC HS USB peripheral,3 V-3.6 V, QFN56_8X8_PAD5_2X4_5	Cypress Semiconductor	CY7C68013A-56LTXC
1	Y1	IC crystal SMD XTALNX3225 24.000000MEGHZ	NDK	NX3225SA-24.000000MHZ
1	Y2	IC crystal OSC prelim, 3.3 V YSML98W79H35_B 38.4 MHz	Rakon	509540

These components are part of the printed circuit board (PCB) or should not be installed.

Table 4. ADRF6720 Evaluation Board Bill of Materials—Do Not Install

Qty	Reference Designator	Description	Manufacturer[1]	Part No.
3	C13, C71, C72	Cap cer X7R C0402, 10%, 50 V 330 pF	Murata	GRM155R71H331KA01D
3	C16 to C18	Do not install (TBD_C0402) TBD0402	N/A	TBD0402
8	C41, C76, C77, C79, C86, C88, C89, C91	Cap cer C0G SMD C0402, ±0.25 pF, 50 V 3.3 pF	Murata	GJM1555C1H3R3CB01D
4	C75, C78, C81, C84	Cap cer C0G SMD C0402, ±0.25 pF, 50 V 2 pF	Murata	GJM1555C1H2R0CB01D
4	C80,C82,C83,C85	Cap mono cer C0G C0402, 5%, 50 V 20 pF	Murata	GRM1555C1H200JZ01D
2	C87, C90	Cap chip mono cer C0G C0402, ±0.1 pF, 50 V 6 pF	Murata	GRM1555C1H6R0BZ01
2	LO_IN–, LO_OUT–	Conn-PCB coax SMA end launch	Johnson	142-0701-851
1	P3	Conn-PCB HDR ST 10P	Samtec	TSW-105-08-G-D
11	R11, R15, R16, R25, R32, R37, R38, R43, R77, R81, R82	Res film SMD R0402, 5%, 1/16 W 0 Ω	Panasonic	ERJ-2GE0R00X
3	R67, R78, R79	Res prec thick film chip R0402, 1%, 1/10 W 1K	Panasonic	ERJ-2RKF1001X
2	T2, T4	XFMR 2.5 GHz balun, T0603-6P	Johanson Technology	2500BL14M050T
4	VCC_LO, VCC_RF, VCC_VCO, VTUNE_TP	Conn-PCB test point red	Components Corporation	TP-104-01-02

[1] N/A = not applicable.

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG12299-0-5/14(0)

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