Evaluating the ADP1974 Bidirectional Synchronous PWM Controller for Battery Test and Formation

FEATURES
Evaluation board for testing the features of the ADP1974
Standalone open-loop capability
FAULT and COMP inputs compatible with the AD8450-EVALZ
Compatible for testing with full external customer solutions
Input voltage range: 6 V to 60 V
On-board 5 V low dropout (LDO) regulator
Selective buck or boost mode
Adjustable frequency from 50 kHz to 300 kHz
Synchronization output or input with adjustable phase shift
Programmable maximum duty cycle
Maximum internal duty cycle: 97%
Programmable soft start
Peak hiccup current limit protection
Input voltage undervoltage lockout (UVLO) protection
Jumper for enable/shutdown control

GENERAL DESCRIPTION
The ADP1974-EVALZ is an open-loop evaluation board that can be used to test the features of the ADP1974. The ADP1974 is a constant frequency, voltage mode, bidirectional synchronous pulse-width modulation (PWM) controller for buck or boost, dc-to-dc, battery charge and discharge applications. When connected to external, high voltage field effect transistors (FET); a half bridge driver; and an external control device, such as the AD8450-EVALZ, the ADP1974-EVALZ can be used to evaluate the ADP1974 in a complete closed-loop application.

This user guide includes input/output descriptions, setup instructions, the schematic, and the printed circuit board (PCB) layout drawings for the ADP1974-EVALZ evaluation board.

The ADP1974-EVALZ can be used to test internal features such as precision enable, pin selective battery charge or recycle mode operation, internal and external frequency synchronization control with programmable phase shift, PWM duty cycle control, programmable maximum duty cycle, programmable dead time, and programmable peak hiccup current limit. Additional protection features that can be evaluated include soft start, input voltage undervoltage lockout (UVLO), fault signaling, and thermal shutdown (TSD).

Complete specifications for the ADP1974 are available in the ADP1974 data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.
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REVISION HISTORY

10/15—Revision 0: Initial Version
TYPICAL SETUP FOR OPEN-LOOP EVALUATION

- Oscilloscope
- Multimeter
- Use jumpers to configure EN and MODE or connect external power supplies to center pins
- Ground connection for external equipment and system ground
- Power supply $V_{IN} = 6V$ to $60V$
- Power supply $V_{FAULT} = 6V$ to $60V$
- Connect an oscilloscope if sync is configured as an output
- Connect to an external clock signal for synchronization if sync is configured as an output
- Power supply $V_{COMP} = 0V$ to $5V$

Figure 1.
EVALUATION BOARD SETUP PROCEDURES
The ADP1974-EVALZ has many features that are customizable via the resistors and capacitors on the evaluation board. Other features are observable by adjusting the voltages applied to several of the pins. Most features can be initially observed without making any physical changes to the board, with the exception of Rs. If no Rs is added, CL must be shorted to GND for most tests. If testing the current-limit functionality, Rs must be mounted to the evaluation board. The steps in the following sections describe how to use the ADP1974-EVALZ evaluation board.

QUICK START STEPS
To begin using the evaluation board, connect the external equipment as described in the following sections.

GNDx Test Loop
The GND1 and GND2 test loops are the power ground connection for the device via the GND pin and the external bypass capacitors. Connect the ground connections from the external equipment to this bus.

VIN Test Loop
Connect an external power supply from to VIN to GND1 or GND2. The VIN test loop connects the positive input supply voltage to the VIN pin. Connect the power supply to this bus and keep the wires as short as possible to minimize the EMI transmission.

EN Test Bus
The EN test bus is used to enable/disable the ADP1974 via the EN pin. Use one of the following methods to control the ADP1974. Do not leave the EN pin floating.
- Use a jumper to connect the top two pins of the EN test bus. This jumper connects EN to VIN and enables the ADP1974 (see Figure 2).
- Use a jumper to connect the bottom two pins of the EN test bus. This jumper connects EN to GND and disables the ADP1974 (see Figure 3).

VREG Test Point
Connect a multimeter from VREG to GNDx. When VEN ≥ 1.25 V (typical), VREG rises to 5 V (typical).

MODE Test Bus
The MODE test bus is used to set the ADP1974 in buck or boost mode. Do not leave the MODE pin floating.
- Use a jumper to connect the top two pins of the MODE test bus. This jumper connects MODE to VREG and places the ADP1974 in buck/charge mode (see Figure 5).
- Use a jumper to connect the bottom two pins of the MODE test bus. This jumper connects MODE to GND and places the ADP1974 in boost/recycle mode (see Figure 6).
- Alternatively, connect a voltage between 0 V and 5.5 V to the center pin of the MODE test bus for independent control of the MODE pin voltage (see Figure 7). The MODE pin is logic high when VMODE ≥ 1.20 V (typical).
**FAULT Test Point**
Connect FAULT to VIN or apply an external voltage between 0 V and 60 V. If SYNC is configured as an output, when $V_{FAULT} \geq 1.2$ V (typical), a square wave is visible on the SYNC pin operating at the frequency set by $R_{REF}$.

**SYNC Test Point**
If SYNC is configured as an output, connect an oscilloscope to SYNC. The SYNC signal is visible when $V_{EN} \geq 1.25$ V (typical) and $V_{FAULT} \geq 1.2$ V (typical).

If SYNC is configured as an input, connect a signal with $f_{SW}$ between 50 kHz and 300 kHz, with $V_{SYNC(HIGH)} \geq 1.2$ V (typical) and $V_{SYNC(LOW)} \leq 1.05$ V (typical).

**COMP Test Point**
Connect an external power supply to COMP. See Figure 8 for the relationship between $V_{COMP}$ and the switching duty cycle of DH and DL.

![Figure 8. Duty Cycle vs. $V_{COMP}$, $R_{REF} = 100$ kΩ, No Load on DL, DH, or DMAX](image)

**DL and DH Test Point**
Connect the DH and DL pins to an oscilloscope. To observe a signal on DH or DL, enable the ADP1974 via the EN pin by setting $V_{EN} \geq 1.25$ V (typical), $V_{FAULT} \geq 1.2$ V (typical), and $V_{COMP} \geq 0.5$ V (typical).

If $V_{MODE} \leq 1.05$ V (typical), the ADP1974 is in boost/recycle mode, and a square wave is visible on the DL pin. A complementary square wave is visible on the DH pin.

![Figure 9. Signal Diagram for Boost Configuration](image)

**CL Test Point**
Unless testing the current limit, connect CL to GND1 or GND2. If testing the current, see the ADP1974 data sheet for more information about current limits and selecting $R_S$ to set the current limit.

**ADJUSTING THE ADP1974-EVALZ COMPONENTS FOR A SPECIFIC APPLICATION**
For more detailed guidance in selecting the components to customize the features of the ADP1974, consult the ADP1974 data sheet.

**Selecting $R_{REF}$ for a Master Device**
When $V_{SCFG}$ is $\geq 4.53$ V, the ADP1974 operates as a master device. When functioning as a master device, the ADP1974 operates at the frequency set by the external $R_{REF}$ resistor connected between FREQ and ground, and the ADP1974 outputs a clock at the programmed frequency on the SYNC pin.
Figure 11 shows the relationship between the R\textsubscript{FREQ (MASTER)} value and the programmed switching frequency.

![Figure 11. R\textsubscript{FREQ (MASTER)} vs. Switching Frequency (f\textsubscript{SET})](image)

To calculate the R\textsubscript{FREQ (MASTER)} value for a desired master clock synchronization frequency, use the following equation:

$$\text{R}_{\text{FREQ (MASTER)}} (\text{k}\Omega) = \frac{10^4}{f_{\text{SET}} (\text{kHz})}$$  \hspace{1cm} (1)

where:

- \text{R}_{\text{FREQ (MASTER)}} is the resistor in k\Omega to set the frequency for master devices.
- \text{f}_{\text{SET}} is the switching frequency in kHz.

**Selecting R\textsubscript{FREQ} for a Slave Device**

To configure the ADP1974 as a slave device, drive V\text{SCFG} < 4.53 V. When functioning as a slave device, the ADP1974 operates at the frequency of the external clock applied to the SYNC pin. To ensure proper synchronization, select R\text{FREQ} to set the frequency to a value slightly slower than that of the master clock by using the following equation:

$$\text{R}_{\text{FREQ (SLAVE)}} = 1.11 \times \text{R}_{\text{FREQ (MASTER)}}$$  \hspace{1cm} (2)

where:

- \text{R}_{\text{FREQ (SLAVE)}} is the resistor value that appropriately scales the frequency for the slave device, and 1.11 is the \text{R}_{\text{FREQ}} slave to master ratio for synchronization.
- \text{R}_{\text{FREQ (MASTER)}} is the resistor value that corresponds to the frequency of the master clock applied to the SYNC pin.

The frequency of the slave device is set to a frequency slightly lower than that of the master device to allow the digital synchronization loop of the ADP1974 to synchronize to the master clock period. The slave device can synchronize to a master clock frequency running between 2% to 20% higher than the slave clock frequency. Setting \text{R}_{\text{FREQ (SLAVE)}} to 1.11\times larger than \text{R}_{\text{FREQ (MASTER)}} runs the synchronization loop in approximately the center of the adjustment range.

**Phase Shift Resistor (R\text{SCFG})**

If a phase shift from SYNC to DH and DL is desired, select R\text{SCFG} for the desired time delay using Figure 12 as reference.

![Figure 12. R\text{SCFG} vs. Phase Delay, R\text{FREQ} = 100 k\Omega](image)

**Programming the Dead Time (R\text{DT})**

To adjust the dead time on the synchronous DH and DL outputs, connect a resistor (R\text{DT}) from DT to GND and bypass with a 47 pF capacitor. Select R\text{DT} for a given dead time using Figure 13 or calculate R\text{DT} using the following equations. To reach a single equation for R\text{DT}, combine the equations for V\text{DT} and R\text{DT}.

$$V_{\text{DT}} (V) = \frac{I_{\text{DT}} \times (t_{\text{DEAD (ns)}} - 28.51)}{3.76}$$  \hspace{1cm} (3)

$$R_{\text{DT}} = \frac{V_{\text{DT}}}{I_{\text{DT}}}$$  \hspace{1cm} (4)

where:

- V\text{DT} is the DT pin programming voltage.
- I\text{DT} is 20 µA, typical internal current source.
- t\text{DEAD} is the desired dead time in ns.
- R\text{DT} is the resistor value in k\Omega for the desired dead time.

To calculate R\text{DT} for a given t\text{DEAD}, the resulting equation used is

$$R_{\text{DT}} (\text{k}\Omega) = \frac{t_{\text{DEAD (ns)}} - 28.51}{3.76}$$  \hspace{1cm} (5)

![Figure 13. DT Pin Resistance (R\text{DT}) vs. Dead Time (t\text{DEAD})](image)
**Maximum Duty Cycle Resistor (R\text{DMAX})**

To customize the maximum duty cycle of the DH and DL pins for the ADP1974, use Figure 14 to select R\text{DMAX}.

![Figure 14. R\text{DMAX} vs. Duty Cycle, R\text{REQ} = 100 kΩ, V\text{COMP} = 5 V](image)

**Current-Limit Set Resistor (R\text{S})**

If testing the current limit in an application, use the following equation to set the current limit:

\[
I_{PK} (\text{mA}) = \frac{100 \text{ mV}}{R_S}
\]

where:

- \(I_{PK}\) is the desired peak current limit in mA.
- \(R_S\) is the sense resistor used to set the peak current limit in Ω.

When the ADP1974 is configured to operate in buck (charge) mode, the internal current-limit threshold is set to 300 mV (typical) and the negative valley current-limit threshold is set to 450 mV (typical). When the ADP1974 is configured to operate in boost (recycle) mode, the internal current-limit threshold is set to 500 mV (typical). The external resistor (R\text{CL}) is needed to offset the current properly to detect the peak in both buck and boost operation. Set the R\text{CL} value to 20 kΩ. In operation, the equations for setting the peak currents follow.

For buck/charge mode, the equations are

\[
V_{CL(buck)} = (I_{CL}) \times (R_{CL}) - (I_{PK}) \times (R_S)
\]

\[
V_{NC(buck)} = (I_{CL}) \times (R_{CL}) + (I_{VLNEG}) \times (R_S)
\]

For boost/recycle mode, the equation is

\[
V_{CL(boost)} = (I_{CL}) \times (R_{CL}) + (I_{PK}) \times (R_S)
\]

where:

- \(V_{CL(buck)}\) = 300 mV typical.
- \(V_{NC(buck)}\) = 450 mV typical.
- \(V_{CL(boost)}\) = 500 mV typical.
- \(I_{PK}\) = peak inductor current.
- \(I_{VLNEG}\) = valley inductor current.
- \(I_{CL}\) = 20 µA, typical.
- \(R_{CL}\) = 20 kΩ.

**Soft Start Capacitor (C\text{SS})**

The ADP1974-EVALZ comes with a 1 nF capacitor on the evaluation board.

A C\text{SS} capacitor is not required for the ADP1974. When the C\text{SS} capacitor is not used, the internal 5 µA (typical) current source pulls the SS pin voltage to V\text{REG}, and there is no soft start control. Use the following equation to calculate the delay time before switching is enabled (t\text{REG}):

\[
t_{REG} = \frac{0.52}{I_{SS}} \times C_{SS}
\]

where:

- \(I_{SS}\) = 5 µA, typical.
- \(C_{SS}\) = soft start capacitor value.

During soft start, the ADP1974 operates in asynchronous mode, and the synchronous FET is not driven. After the soft start period is completed (SS > 4.5 V), the ADP1974 switches to full synchronous mode.

**APPLICATION SPECIFIC ADP1974 CONTROL**

When integrated in a battery test solution, the ADP1974 can be controlled with external control signals from other devices in the application. The FAULT pin allows an external device to signal the ADP1974 when an external fault occurs. The COMP pin allows an external device to control the PWM output signals on the DH and DL pins. The SYNC and SCFG pins can be used to synchronize the ADP1974 to an external clock signal or to implement the ADP1974 as a master clock. The EN and MODE pins provide logic control to turn the ADP1974 on or off and to transition the system between boost/recycle mode and buck/charge mode.
EVALUATION BOARD HARDWARE
TYPICAL APPLICATION CIRCUIT

Figure 16. ADP1974 Typical Application Circuit

Table 1. Input Pins that Require External Power Supplies or External Control Signals

<table>
<thead>
<tr>
<th>Power Supply</th>
<th>Connector</th>
<th>Voltage Range (V)</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN¹</td>
<td>VIN</td>
<td>6 to 60</td>
<td>Supplies power to the ADP1974 internal control circuitry.</td>
</tr>
<tr>
<td>VEN¹</td>
<td>EN</td>
<td>0 to 60</td>
<td>Supplies logic signal to enable operation of the ADP1974.</td>
</tr>
<tr>
<td>VMODE¹</td>
<td>MODE</td>
<td>0 to 5.5</td>
<td>Supplies logic signal to select boost/recycle mode or buck/charge mode.</td>
</tr>
<tr>
<td>VFAULT²</td>
<td>FAULT</td>
<td>0 to 60</td>
<td>Supplies the signal to indicate when a fault condition has occurred in the application external to the ADP1974.</td>
</tr>
<tr>
<td>VCOMP³</td>
<td>COMP</td>
<td>0.5 to 5.0</td>
<td>Supplies the error signal that is compared internally to the linear ramp to produce the PWM signal.</td>
</tr>
<tr>
<td>VSINC</td>
<td>SYNC</td>
<td>0 to 5.5</td>
<td>Supplies the external synchronization waveform when the ADP1974 is a slave device, and SYNC is configured as an input.</td>
</tr>
</tbody>
</table>

¹ VIN can also be used to supply VEN and VMODE via jumper connections. Alternatively, EN and MODE can be powered with separate power supplies.
² When used with the AD8450, the FAULT signal is supplied by the FAULT pin (Pin 46) of the AD8450.
³ When used with the AD8450, the COMP signal is supplied by the VCTRL pin (Pin 59), the error amplifier output of the AD8450.

Table 2. Output Pins to Observe with Ammeter or Oscilloscope

<table>
<thead>
<tr>
<th>Output Signal</th>
<th>Connector</th>
<th>Signal</th>
<th>Recommended Equipment</th>
<th>Expected Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREG¹</td>
<td>VREG</td>
<td>5 V dc</td>
<td>Ammeter or oscilloscope</td>
<td>When VIN &gt; 6 V, VREG rises to 5 V.</td>
</tr>
<tr>
<td>VDL</td>
<td>DL</td>
<td>0 V to VREG square wave</td>
<td>Oscilloscope</td>
<td>When MODE is logic low, a square wave is visible on DH.</td>
</tr>
<tr>
<td>VDH</td>
<td>DH</td>
<td>0 V to VREG square wave</td>
<td>Oscilloscope</td>
<td>When MODE is logic high, DL is complementary to DH.</td>
</tr>
<tr>
<td>VSINC</td>
<td>SYNC</td>
<td>0 V to VREG square wave</td>
<td>Oscilloscope</td>
<td>When MODE is logic high, a square wave is visible on DL.</td>
</tr>
<tr>
<td>ICL</td>
<td>CL</td>
<td>Magnitude dependent on Rs triangle wave</td>
<td>Oscilloscope</td>
<td>When MODE is logic low, DH is complementary to DL.</td>
</tr>
</tbody>
</table>

¹ VREG provides the logic high signal for the MODE pin when a jumper is placed on the top two pins of the MODE test bus.
Figure 17. ADP1974 Evaluation Board Schematic
# ORDERING INFORMATION

## BILL OF MATERIALS

<table>
<thead>
<tr>
<th>Qty</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Manufacturer(^1)</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U1</td>
<td>ADP1974 buck or boost, PWM controller</td>
<td>Analog Devices, Inc.</td>
<td>ADP1974ARUZ-RL</td>
</tr>
<tr>
<td>2</td>
<td>CDL, CDH</td>
<td>Bypass capacitors for logic DL and DH pins, 1000 pF, 10 V, 0805</td>
<td>Kemet</td>
<td>C0805C102K8RACTU</td>
</tr>
<tr>
<td>2</td>
<td>RD, RDH</td>
<td>Signal integrity resistor, 20 Ω, 0805, ±1%</td>
<td>Vishay Dale</td>
<td>CRCW080520R0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>CVREG</td>
<td>Bypass capacitor for internal LDO, 1 µF, 6.3 V, 0805</td>
<td>TDK Corporation</td>
<td>CGJ4J2X7R0J105K125AA</td>
</tr>
<tr>
<td>1</td>
<td>CVIN1</td>
<td>Input voltage bypass capacitor, 4.7 µF, 100 V, 10%, X7S, 1210</td>
<td>TDK Corporation</td>
<td>C322S752A475K200AB</td>
</tr>
<tr>
<td>1</td>
<td>CVIN2</td>
<td>Input voltage bypass capacitor</td>
<td>Open</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>CSYNC</td>
<td>SYNC pin bypass capacitor, 0.1 µF, 6.3 V, 0805</td>
<td>Kemet</td>
<td>C0805C104K9RACTU</td>
</tr>
<tr>
<td>1</td>
<td>RSYNC</td>
<td>SYNC pin resistor, 1 kΩ, 0805, ±1%</td>
<td>Vishay Dale</td>
<td>CRCW08051K00FKEA</td>
</tr>
<tr>
<td>1</td>
<td>RDT</td>
<td>DT pin resistor, 10 kΩ, 0805, ±1%</td>
<td>Vishay Dale</td>
<td>CRCW080510K0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>RCL</td>
<td>Current-limit offset sense resistor, 20 kΩ, 0805, ±1%</td>
<td>Vishay Dale</td>
<td>CRCW080520K0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>RS</td>
<td>Current-limit set resistor</td>
<td>Open</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>RSCFG</td>
<td>Synchronization pin control resistor</td>
<td>Open</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>CS, CMAX, CDT</td>
<td>SCFG, DMAX, and DT pin bypass capacitors, 47 pF, 50 V, 0805</td>
<td>Kemet</td>
<td>C0805C470J5GACTU</td>
</tr>
<tr>
<td>1</td>
<td>RFREQ</td>
<td>Frequency set resistor, 100 kΩ, 0805, ±1%</td>
<td>Vishay Dale</td>
<td>CRCW0805100K0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>RDMAX</td>
<td>Maximum duty cycle set resistor</td>
<td>Open</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>CSS</td>
<td>External soft start capacitor, 1000 pF</td>
<td>Kemet</td>
<td>C0805C102K8RACTU</td>
</tr>
<tr>
<td>4</td>
<td>VIN, GND1, GND2, CL</td>
<td>Test point loop connectors</td>
<td>Aavid Thermalloy</td>
<td>125800D00000G</td>
</tr>
<tr>
<td>2</td>
<td>EN, MODE</td>
<td>Headers, 0.100 inches, single, straight, 3-pin</td>
<td>Sullins Connector Solutions</td>
<td>PBC03SAAN(^2)</td>
</tr>
<tr>
<td>8</td>
<td>VREG, DH, DL, DHR, DHR, COMP, SYNC, FAULT</td>
<td>PC test point, compact</td>
<td>Keystone Electronics</td>
<td>5007</td>
</tr>
<tr>
<td>2</td>
<td>EN, MODE</td>
<td>Connector, jumper, shorting, gold</td>
<td>Sullins Connector Solutions</td>
<td>SSC02SYAN</td>
</tr>
</tbody>
</table>

\(^1\) Equivalent substitutions may be made for all passive components and connectors.

\(^2\) Alternatively, PBC36SAAN can be purchased and cut as necessary.

## RELATED LINKS

<table>
<thead>
<tr>
<th>Resource</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADP1974</td>
<td>Buck or boost, PWM controller for battery test solutions</td>
</tr>
<tr>
<td>AD8450</td>
<td>Precision analog front end and controller for battery test/formation systems</td>
</tr>
</tbody>
</table>
NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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