Evaluating the ADM1270 High Voltage Input Protection Device

FEATURES

Controls supply voltages from 4 V to 60 V
Gate drive for low voltage drop reverse supply protection
Gate drive for P-channel field effect transistors (FETs)
Inrush current limiting control
Adjustable current limit
Foldback current limiting
Automatic retry or latch-off on current fault
Programmable current-limit timer for safe operating area (SOA)
Power-good and fault outputs
Analog undervoltage (UV) and overvoltage (OV) protection
16-lead, 3 mm × 3 mm LFCSP
16-lead QSOP

EVALUATION KIT CONTENTS

ADM1270CP-EVALZ or ADM1270RQ-EVALZ evaluation board

ADDITIONAL EQUIPMENT NEEDED

DC power supply
Multimeters for voltage and current measurements
Electronic or resistive loads

GENERAL DESCRIPTION

The ADM1270CP-EVALZ and ADM1270RQ-EVALZ evaluation boards are used to demonstrate the functionality of the ADM1270 high voltage input protection device.

Full specifications on the ADM1270 are available in the product data sheet, which should be consulted in conjunction with this user guide when using these evaluation boards.
TABLE OF CONTENTS

Features .............................................................................................. 1
Evaluation Kit Contents..................................................................... 1
Additional Equipment Needed ......................................................... 1
General Description ........................................................................... 1
Revision History ................................................................................. 2
Evaluation Board Hardware .............................................................. 3
   Evaluation Board Configurations .............................................. 3
Configuring the ADM1270 ............................................................. 4
   Powering the ADM1270 ............................................................ 4
   Current Sense Inputs .............................................................. 4
   Current-Limit Reference ......................................................... 4
   Setting the Current Limit (ISET) ............................................... 4
Foldback............................................................................................. 5
Timer .................................................................................................. 5
   Timer_Off .................................................................................. 6
Hot Swap Retry Duty Cycle ............................................................ 7
Gate and RPFG Clamps .................................................................. 7
Fast Response to Severe Overcurrent ............................................ 7
Undervoltage and Overvoltage ....................................................... 7
Enable Input ..................................................................................... 7
Power Good .................................................................................... 8
Evaluation Board Schematics and Artwork ..................................... 9
Ordering Information ....................................................................... 12
Bill of Materials ............................................................................. 12

REVISION HISTORY

4/16—Rev. 0 to Rev. A
   Change to Setting the Current Limit (ISET) Section................. 5

12/14—Revision 0: Initial Version
EVALUATION BOARD HARDWARE

EVALUATION BOARD CONFIGURATIONS

The ADM1270CP-EVALZ and ADM1270RQ-EVALZ evaluation boards arrive supplied with different components depending on which version is ordered.

<table>
<thead>
<tr>
<th>Component</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>High voltage protection device</td>
<td>ADM1270CP or ADM1270RQ high voltage protection device</td>
</tr>
<tr>
<td>C1</td>
<td>VCAP bypass capacitor</td>
<td>1 μF, VCAP bypass capacitor</td>
</tr>
<tr>
<td>C2</td>
<td>TIMER capacitor</td>
<td>100 nF, CTIMER, sets an SOA overcurrent (OC) fault delay, nominally 100 ms</td>
</tr>
<tr>
<td>C3</td>
<td>TIMER_OFF capacitor</td>
<td>100 nF, CTIMER_OFF, sets an initial timing cycle delay and the SOA off time delay, nominally 200 ms</td>
</tr>
<tr>
<td>R1</td>
<td>OVLO/UVLO resistor divider</td>
<td>332 kΩ, sets UV threshold, nominally 8.7 V</td>
</tr>
<tr>
<td>R2</td>
<td>OVLO/UVLO resistor divider</td>
<td>33.2 kΩ, sets OV/UV thresholds with R1 and R3</td>
</tr>
<tr>
<td>R3</td>
<td>OVLO/UVLO resistor divider</td>
<td>10 kΩ, sets OV threshold, nominally 37.5 V</td>
</tr>
<tr>
<td>R4</td>
<td>OC current-limit threshold</td>
<td>100 kΩ, sets OC threshold with R5, nominally 450 mA when R6 = 100 mΩ</td>
</tr>
<tr>
<td>R5</td>
<td>OC current-limit threshold</td>
<td>100 kΩ, sets OC threshold with R4, nominally 450 mA when R6 = 100 mΩ</td>
</tr>
<tr>
<td>R6</td>
<td>Current sense resistor</td>
<td>100 mΩ, current sense resistor for OC protection</td>
</tr>
<tr>
<td>R7</td>
<td>OC foldback divider</td>
<td>4.75 kΩ, sets foldback threshold with R8, nominally 13.2 V</td>
</tr>
<tr>
<td>R8</td>
<td>OC foldback divider</td>
<td>332 kΩ, sets foldback threshold with R7, nominally 13.2 V</td>
</tr>
<tr>
<td>R9</td>
<td>Power-good (PG) threshold</td>
<td>20 kΩ, sets power-good threshold, nominally 18 V</td>
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<tr>
<td>R10</td>
<td>FAULT pull up</td>
<td>332 kΩ, FAULT pin pull up</td>
</tr>
<tr>
<td>R11</td>
<td>PWRGD pull up</td>
<td>332 kΩ, PWRGD pin pull up</td>
</tr>
<tr>
<td>R12</td>
<td>ENABLE pull down</td>
<td>332 kΩ, ENABLE pin pull down</td>
</tr>
<tr>
<td>Q1A, Q1B</td>
<td>Protection FET</td>
<td>FDS9958 dual P-channel metal-oxide semiconductor field effect transistor (MOSFET), −60 V/−2.9 A, 105 mΩ</td>
</tr>
<tr>
<td>Q2, Q4</td>
<td>Protection FET</td>
<td>DPAK FET (optional)</td>
</tr>
<tr>
<td>Q3, Q5</td>
<td>Protection FET</td>
<td>DPAK FET (optional)</td>
</tr>
<tr>
<td>J1</td>
<td>Jumper</td>
<td>Connects ENABLE to VIN for automatic startup</td>
</tr>
<tr>
<td>J2</td>
<td>Jumper</td>
<td>Connect this pin directly to the ENABLE pin for automatic retry after shutdown</td>
</tr>
</tbody>
</table>

Component varies depending on the evaluation board ordered.
CONFIGURING THE ADM1270

POWERING THE ADM1270

A supply voltage from 4 V to 60 V is required to power the ADM1270 via the VCC/SENSE+ pin. The VCC/SENSE+ pin provides the majority of the bias current for the device; the remainder of the current needed to control the gate drive and to best regulate the gate to source voltage (VGS) is supplied by the SENSE− pin.

CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external current sense resistor, RSENSE (see Figure 1). An internal current sense amplifier provides a gain of 40 to the voltage drop detected across RSENSE. The result is compared to an internal reference and is used by the hot swap control logic to detect an overcurrent condition.

CURRENT-LIMIT REFERENCE

The current-limit reference voltage determines the load current at which the ADM1270 limits the current during an overcurrent event. This reference voltage is compared to the amplified current sense voltage to determine when the current-limit threshold is reached.

An internal current-limit reference selector block continuously compares the current-limit (ISET) and foldback (FLB) voltages to determine which voltage is the lowest at any given time; the lowest voltage is used as the current-limit reference. This behavior ensures that the programmed current limit, ISET, is used in normal operation, and that the foldback feature reduces the current limit when required during startup and/or fault conditions.

The FLB voltage varies during different modes of operation and, therefore, is clamped to a minimum level of 200 mV. This behavior prevents zero current flow due to the current limit being set too low. Figure 3 provides an example of how the FLB and ISET voltages interact during startup as the ADM1270 turns on the FET and charges the load capacitance. Depending on how the foldback feature is configured, the transition point varies to ensure that the FET operates within the correct limits.

SETTING THE CURRENT LIMIT (ISET)

The maximum current limit is partially determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor value decreases for a given current sense voltage. Choosing an appropriate current sense resistor can be difficult due to the limited selection of low value resistors. The ADM1270 provides an adjustable current sense voltage limit to handle this issue. The device allows the user to program the required current sense voltage limit from 12.5 mV to 62.5 mV.
The default value is 50 mV and is achieved by connecting the ISET pin directly to the VCAP pin. This circuit configuration configures the device to use an internal 2 V reference, which results in 50 mV at the sense inputs (see Figure 4).

![Figure 4. Fixed 50 mV Current Sense Limit](image)

To program the sense voltage from 12.5 mV to 62.5 mV, an external resistor divider sets the reference voltage on the ISET pin (see Figure 5).

![Figure 5. Adjustable 12.5 mV to 62.5 mV Current Sense Limit](image)

FOLDBACK

Foldback is a method to actively reduce the current limit as the voltage drop across the FET increases. This technique keeps the power dissipation in the FET at a minimum during power-up, overcurrent, or short-circuit events. It also reduces the need to oversized the FET to accommodate worst-case conditions, resulting in board size and cost savings.

Assuming that the supply voltage remains constant and within tolerance, the ADM1270 detects the voltage drop across the FET by sensing output voltage through a resistor divider. The device, therefore, relies on the principle that the drain of the FET is at the maximum expected supply voltage, and that the magnitude of the output voltage is relative to that of the VDS of the FET. Using a resistor divider from the output voltage to the FLB pin, the relationship from VOUT, and thus VDS, to VFLB can be derived.

Design the resistor divider to result in a voltage equal to VSET/2 when VOUT falls below the desired level. This voltage must be well below the working tolerance of the supply rail. As VOUT continues to drop, the current-limit reference follows VFLB because it is now the lowest voltage input to the current-limit reference selector block, resulting in a reduction of the current limit and, therefore, the regulated load current. To prevent the current from decreasing to zero, a clamp activates when VFLB reaches 200 mV. The current limit cannot drop below this level.

To ensure that the SOA characteristics of a particular FET are not violated, the minimum current for this clamp varies from design to design. However, the current-limit reference fixes this clamp at 200 mV, which equals 10 mV across the sense resistor. Therefore, the main ISET voltage can be adjusted to adjust the clamp to the required percentage current reduction. For example, if VSET equals 1.6 V, set the clamp at 25% of the maximum current.

TIMER

An essential block of the ADM1270 is the TIMER function, which limits the time the current is in regulation during an overcurrent event. MOSFETs are designed to withstand a given amount of power for a prescribed maximum time. The MOSFET manufacturers outline this range, or SOA, using a graph such as that shown in Figure 6.

![Figure 6. MOSFET SOA Graph](image)

The VCAP pin has a 3.6 V internally generated voltage that can set a voltage at the ISET pin. Assuming that VSET equals the voltage on the ISET pin, select the resistor divider values to set the ISET voltage as follows:

\[ V_{SET} = V_{SENSE} \times 40 \]

where \( V_{SENSE} \) is the current sense voltage limit.

The VCAP rail also can be used as the pull-up supply for setting other pins. To guarantee that VCAP meets its accuracy specifications, do not apply a load to the VCAP pin greater than 100 \( \mu \)A.
The SOA graph shows a relationship between the combined drain to source voltage, the drain current, and the time duration that the MOSFET can withstand this dissipation. For example, the MOSFET in Figure 6 can withstand 60 V and 2 A (120 W) for 1 ms. If this condition persists for a greater duration, the MOSFET may be damaged. The TIMER circuit can ensure that the length of time the MOSFET is subject to these worst-case conditions is limited by the external TIMER capacitor. For example, if the TIMER is set to 1 ms, and the current exceeds the limit for more than 1 ms, the circuit times out and shuts down the MOSFET.

The TIMER pin handles the timing function with an external capacitor, \( C_{\text{TIMER}} \). The two TIMER pin comparator thresholds are \( V_{\text{TIMERL}} \) (0.1 V) and \( V_{\text{TIMERH}} \) (2.0 V). There are two timing current sources as well: a 20 µA pull-up current and a 1 µA pull-down current.

These current and voltage levels, in combination with the user chosen value of \( C_{\text{TIMER}} \), determine the fault current-limit time and the on-time of the hot swap retry duty cycle. The TIMER pin capacitor value is determined using the following equation:

\[
C_{\text{TIMER}} = \left( \frac{I_{\text{on}} \times 20 \text{ µA}}{V_{\text{TIMERH}}} \right)
\]

where:
- \( I_{\text{on}} \) is the time that the FET is allowed to spend in regulation at the current limit.
- \( V_{\text{TIMERH}} \) is the TIMER high threshold.

The choice of FET is based on matching this time with the SOA characteristics of the FET. Foldback can also be used to simplify the selection.

When the voltage across the sense resistor reaches the circuit breaker trip voltage, \( V_{\text{CB}} \), the 20 µA TIMER pull-up current is activated. The ADM1270 begins to regulate the load current at the current limit, initiating a rising voltage ramp on the TIMER pin. If the sense voltage falls below this circuit breaker trip voltage before the TIMER pin reaches \( V_{\text{TIMERH}} \), the 20 µA pull-up current is disabled, and the 1 µA pull-down current is enabled. If the voltage on the TIMER pin falls below \( V_{\text{TIMERL}} \), the TIMER pin is discharged to GND using a strong pull-down current on the TIMER pin.

The circuit breaker trip voltage is not the same as the hot swap sense voltage current limit. There is a small circuit breaker offset, \( V_{\text{CBOS}} \), which causes the timer to start shortly before the current reaches the defined current limit.

In latch-off mode, the TIMER pin is discharged to GND when it reaches the \( V_{\text{TIMERH}} \) threshold. The TIMER_OFF pin begins to charge up. While the TIMER_OFF pin is ramping up, the hot swap controller remains off and cannot be turned back on, and the FAULT pin remains low. When the voltage on the TIMER_OFF pin rises above the \( V_{\text{TMROFFH}} \) threshold, the hot swap controller can be reenabled by toggling the ENABLE pin from high to low and then high again.

**TIMER_OFF**

The TIMER_OFF pin handles two timing functions with an external capacitor, \( C_{\text{TIMER_OFF}} \). There is one TIMER_OFF pin comparator threshold at \( V_{\text{TMROFFH}} \) (2.0 V). There are two timing current sources, a 20 µA pull-up current and a 1 µA pull-up current.

These current and voltage levels, in combination with the user chosen value of \( C_{\text{TIMER_OFF}} \), determine the initial power-on reset time and also set the fault current-limit off time.

When VCC is connected to the input supply, the internal supply (VCAP) of the ADM1270 must charge up. VCAP starts up and settles in a very short time. When the UVLO threshold voltage is exceeded at VCAP, the device emerges from reset. During this first brief reset period, the GATE and TIMER pins are both held low.

The ADM1270 then proceeds through an initial timing cycle. The TIMER_OFF pin is pulled high with 20 µA. When the TIMER_OFF pin reaches the \( V_{\text{TMROFFH}} \) threshold (2.0 V), the initial timing cycle is complete. This initial power-on reset duration is determined by the following equation:

\[
\text{INITIAL} = \frac{V_{\text{TMROFFH}}}{C_{\text{TIMER_OFF}}/20 \text{ µA}}
\]

For example, a 100 nF capacitor results in a delay of approximately 10 ms. If the UV and OV inputs indicate that VCC is within the defined window of operation when the initial timing cycle terminates, the device is ready to start a hot swap operation.

At the completion of this initial power-on reset cycle, the TIMER_OFF pin is ready to perform a second function. When the voltage at the TIMER pin exceeds the fault current-limit time threshold voltage of \( V_{\text{TIMERH}} \) (2.0 V), the 1 µA pull-up current is activated on TIMER_OFF, and \( C_{\text{TIMER_OFF}} \) begins to charge initiating a voltage ramp on the TIMER_OFF pin. When the TIMER_OFF pin reaches \( V_{\text{TMROFFH}} \), the TIMER_OFF fault current-limit off time is complete.

This fault current-limit off time is determined by the following equation:

\[
\text{TIMER_OFF} = \frac{V_{\text{TMROFFH}}}{C_{\text{TIMER_OFF}}/1 \text{ µA}}
\]

For example, a 100 nF capacitor results in an off time of approximately 200 ms from the time that TIMER exceeds \( V_{\text{TIMERH}} \) to the time that TIMER_OFF reaches \( V_{\text{TMROFFH}} \).
**HOT SWAP RETRY DUTY CYCLE**

The ADM1270 turns off the FET after an overcurrent fault and then uses the capacitor on the TIMER_OFF pin to generate a delay before automatically retrying the hot swap operation. To configure the ADM1270 for automatic retry mode, tie the FAULT pin to the ENABLE pin. Note that a pull-up resistor to VCAP is required on the FAULT pin.

When an overcurrent fault occurs, the capacitor on the TIMER pin charges with a 20 µA pull-up current. When the TIMER pin reaches \( V_{\text{TIMER}} (2.0 \text{ V}) \), the GATE pin is pulled high, turning off the FET. When the FAULT pin is tied to the ENABLE pin for automatic retry mode, the TIMER_OFF pin begins to charge with a 1 µA current source. When the TIMER_OFF pin reaches \( V_{\text{TIMER_OFF}} (2.0 \text{ V}) \), the ADM1270 automatically restarts the hot swap operation.

The automatic retry duty cycle is set by the ratio of 1 µA/20 µA and the ratio of \( C_{\text{TIMER}}/C_{\text{TIMER_OFF}} \). The retry duty cycle is set by the following equation:

\[
\text{Duty\_Cycle} = \frac{(C_{\text{TIMER}} \times 1 \mu\text{A})}{(C_{\text{TIMER_OFF}} \times 20 \mu\text{A})}
\]

The value of the \( C_{\text{TIMER}} \) and \( C_{\text{TIMER_OFF}} \) capacitors determine the on and off time of this cycle, which are calculated as follows:

\[
\begin{align*}
\text{t}_{\text{ON}} &= V_{\text{TIMER}} \times \frac{C_{\text{TIMER}}}{20 \mu\text{A}} \\
\text{t}_{\text{OFF}} &= V_{\text{TIMER_OFF}} \times \frac{C_{\text{TIMER_OFF}}}{1 \mu\text{A}}
\end{align*}
\]

A 100 nF capacitor on the TIMER pin gives an on time of 10 ms. A 100 nF capacitor on the TIMER_OFF pin gives an off time of 200 ms. The device retries continuously in this manner and can be disabled manually by holding the ENABLE pin low, or by disconnecting the FAULT pin. To prevent thermal stress in the FET, a capacitor on the TIMER_OFF pin can be used to extend the retry time to any desired level.

**GATE AND RPFG CLAMPS**

The circuits driving the GATE and RPFG pins are clamped to less than 14 V below the VCC/SENSE+ pin. These clamps ensure that the maximum \( V_{\text{GS}} \) rating of the external FETs is not exceeded.

The reverse protection FET gate pin (RPFG) drives the gate of an external PMOSFET. This PMOSFET, Q2, provides reverse polarity protection to the ADM1270 and the system being powered. If the VCC and GND pins have been reverse connected (that is, where power is actually applied to GND), VCC is negative with respect to the system ground. In this condition, Q2 prevents current from flowing in the reverse direction because the gate of Q2 is held at GND, and Q2 is off. \( V_{\text{OUT}} \) is not pulled below GND, and the system is protected against a reverse polarity connection.

In the typical case where power is applied to VCC, the gate is still pulled down and allows the FET Q2 to turn on and conduct current in the forward direction. Operating Q2 in this way provides a low on-resistance, low voltage drop compared to a diode for reverse polarity protection, giving the system higher efficiency and more headroom for operation. Refer to the ADM1270 data sheet for the connection of Q2 and RPFG for proper operation.

**FAST RESPONSE TO SEVERE OVERCURRENT**

The ADM1270 includes a separate, high bandwidth, current sense amplifier to detect a severe overcurrent that is indicative of a short circuit. The fast response time allows the ADM1270 to handle events of this type that could otherwise cause catastrophic damage if not detected and dealt with very quickly. The fast response circuit ensures that the ADM1270 can detect an overcurrent event of approximately 200% of the normal current limit and control the current within approximately 2 µs.

**UNDervoltage AND OVERvoltage**

The ADM1270 monitors the supply voltage for UV and OV conditions. The UV and OV pins are connected to the inputs of the voltage comparators and compared to an internal 1 V voltage reference.

Figure 7 illustrates the voltage monitoring input connections. An external resistor network divides the supply voltage for monitoring. An undervoltage event is detected when the voltage connected to the UV pin falls below 1 V, and the FET is turned off using the 10 mA pull-up current. Similarly, when an overvoltage event occurs and the voltage on the OV pin exceeds 1 V, the FET is turned off using the 10 mA pull-up current.

**ENABLE INPUT**

The ADM1270 provides a dedicated ENABLE digital input pin. The ENABLE pin allows the ADM1270 to remain off by using a hardware signal, even when the voltage on the UV pin is greater than 1.0 V, and the voltage on the OV pin is less than 1.0 V. Although the UV pin can be used to provide a digital enable signal, using the ENABLE pin for this purpose keeps the ability of the UV pin free to monitor undervoltage conditions.

In addition to the conditions for the UV and OV pins, the ADM1270 ENABLE input pin must be high for the device to begin a power-up sequence.
A similar function can be achieved using the UV pin directly. Alternatively, if the UV divider function is still required, the configuration shown in Figure 8 can be used.

Diode D1 prevents the external driver pull-up resistor from affecting the UV threshold. Select Diode D1 using the following criteria:

\[(V_I \times D1) + (V_{OL} \times EN) \ll 1.0 \text{ V} (I_e = V_{ol}/R1)\]

Ensure that the EN sink current does not exceed the specified \(V_{OL}\) value. If the open-drain device has no pull-up, the diode is not required.

**POWER GOOD**

The power-good (PWRGD) output can be used to indicate whether the output voltage exceeds a user defined threshold and can, therefore, be considered good. The PWRGD output is set by a resistor divider connected to the FB_PG pin (see Figure 9).

When the voltage at the FB_PG pin exceeds the 1 V threshold (indicating that the output voltage has risen), the open-drain pull-down current is disabled, allowing PWRGD to be pulled high. The PWRGD pin is an open-drain output that pulls low when the voltage at the FB_PG pin is lower than the 1 V threshold minus the hysteresis (power bad). Hysteresis on the FB_PG pin is fixed at 30 mV. PWRGD is guaranteed to be in a valid state for \(V_{CC} \geq 1.7 \text{ V}\).

Calculate the power-good threshold using the following equation:

\[V_{PWRGD} = 1 \text{ V} \times (1 + RPG1/RPG2)\]

where:

- \(RPG1\) is the resistance from \(V_{OUT}\) to FB_PG.
- \(RPG2\) is the resistance from FB_PG to GND.
EVALUATION BOARD SCHEMATICS AND ARTWORK

Figure 10. ADM1270CP-EVALZ LFCSP Evaluation Board Schematic
Figure 11. ADM1270RQ-EVALZ QSOP Evaluation Board Schematic
ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

<table>
<thead>
<tr>
<th>Qty</th>
<th>Designator</th>
<th>Description</th>
<th>Manufacturer/Vendor</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U1</td>
<td>ADM1270CP or ADM1270RQ</td>
<td>Analog Devices, Inc.</td>
<td>ADM1270ACPZ-R7 or</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ADM1270ARQZ-R7</td>
</tr>
<tr>
<td>1</td>
<td>C1</td>
<td>Capacitor, MLCC, 1 μF, 25 V, 0805, X5R</td>
<td>Murata (or equivalent)</td>
<td>GRM216R61E105KA12</td>
</tr>
<tr>
<td>2</td>
<td>C2, C3</td>
<td>Capacitor, MLCC, 100 nF, 25 V, 0805, X7R</td>
<td>Murata (or equivalent)</td>
<td>GRM218R71E104KA01</td>
</tr>
<tr>
<td>2</td>
<td>J1, J2</td>
<td>Header, single, straight, 2 pins</td>
<td>Sullins Connector Solutions</td>
<td>PEC02SAAN</td>
</tr>
<tr>
<td>5</td>
<td>R1, R8, R10 to R12</td>
<td>Resistor, 332 kΩ, 1%, 0805 case</td>
<td>Vishay Dale</td>
<td>CRCW0805332KFKEA</td>
</tr>
<tr>
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<td>R2</td>
<td>Resistor, 33.2 kΩ, 1%, 0805 case</td>
<td>Vishay Dale</td>
<td>CRCW080533K2FKEA</td>
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<tr>
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<td>R3</td>
<td>Resistor, 10 kΩ, 1%, 0805 case</td>
<td>Vishay Dale</td>
<td>CRCW080510K0FKEA</td>
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<tr>
<td>2</td>
<td>R4, R5</td>
<td>Resistor, 100 kΩ, 1%, 0805 case</td>
<td>Vishay Precision Group</td>
<td>CSM2512</td>
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<tr>
<td>1</td>
<td>R6</td>
<td>Resistor, 0.10 Ω, 1%, 2512 case</td>
<td>Vishay Dale</td>
<td>CRCW08054K75FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R7</td>
<td>Resistor, 4.75 kΩ, 1%, 0805 case</td>
<td>Vishay Dale</td>
<td>CRCW080520K0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R9</td>
<td>Resistor, 20 kΩ, 1%, 0805 case</td>
<td>Fairchild</td>
<td>FDS9958</td>
</tr>
<tr>
<td>1</td>
<td>Q1</td>
<td>FDS9958 dual P-channel MOSFET, −60 V/−2.9 A, 105 mΩ</td>
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</tr>
</tbody>
</table>

Legal Terms and Conditions

By using the Evaluation board discussed herein (together with any tools, components documentation or support materials, the “Evaluation Board”), you are agreeing to be bound by the terms and conditions set forth below (“Agreement”) unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you (“Customer”) and Analog Devices, Inc. (“ADI”), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assigns, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term “Third Party” includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION: ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY: THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED “AS IS” AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER’S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI’S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

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