TERIDIAN SEMICONDUCTOR CORP.

Simplifying System Integration™

73M1822/73M1922 Implementer's Guide

August 27, 2009
Rev. 1.0
UG_1x22_052

Teridian Semiconductor Corp., 6440 Oak Canyon, Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.teridian.com

Table of Contents

Figures

1 Introduction

This guide describes how to use the 73M1822 and 73M1922 MicroDAA® for voice band modem applications. The guide provides application-specific detail that is not found in the *73M1822/73M1922 Data Sheet*. The guide also includes suggested algorithms that can be followed by users who are developing their own software.

The 73M1922 and 73M1822 will be collectively referred to as the 73M1x22 in this document.

1.1 Procedure Conventions

The following conventions apply to the procedures in this document:

- Firmware/software variables in the procedures are in italics (e.g. *VAL*) to distinguish them from register bits or fields.
- The register is shown with the address in the leftmost cell of the first row. The first row shows the bit mnemonic and is ordered with the most significant bit to the left and least significant bit to the right.

0x12	**OFH**	**ENDC**	**ENAC**	**ENSHL**	**$\overline{\text{ENLVD}}$**	**ENFEL**	**ENDT**	**ENNOM**
Write	0/1	0	1	X	0	1	0	X

- The second row indicates values written in the indicated bits during the procedure.
- Cells with multiple values indicate that the bit is used more than once during the procedure. For example, in the example above, OFH is first set to 0 and later set to 1.
- Register fields with an "X" in the procedures indicate bits that remain unchanged during write operations or bits that are not relevant during read operations.
- Registers referenced in the procedures are represented as RGnn where nn is the hexadecimal register address from 0x00 to 0x25 (for example, RG12 represents the register at address 0x12).

1.2 Read-Modify-Write Procedure

Register writes that include unchanged bits should use a read-modify-write procedure to preserve the setting of bits that do not need to be modified during a given SPI transaction. The read-modify-write procedure consists of the following steps:

1. Read the register value into a variable.
2. Apply a mask to the variable to retain bits that are not to be changed and clear bits that are to be changed.
3. Apply a mask to the variable to change the desired bits.
4. Write the new value back to the register.

The following example uses the read-modify-write procedure to write 01xx_110x to Register 0xnn:

1. *VAR* = RGnn
2. *VAR* = *VAR* AND 0011_0001
3. *VAR* = *VAR* OR 0100_1100
4. RGnn = *VAR*

2 Hardware Requirements

2.1 Reset

The 73M1x22 can be initialized to a default state by pulling the $\overline{RST}$ pin low for 100 ns or longer. The device will be ready within 100 µs after the removal of reset pulse. The M/$\overline{S}$ pin is used to provide reset in the 73M1822 and 72M1902 20-pin TSSOP packaged parts. The reset signal is also bi-directional and edge triggered, so either a low-to-high or high-to-low transition will generate a reset. Refer to the *73M1822/73M1922 Data Sheet* for more information on the proper use of reset signals.

2.2 Crystal Oscillator

The Host-Side Device has an on-chip crystal oscillator, prescaler and PLL/NCO to allow a choice of a wide range of sample rates and crystal choices. The crystal oscillator is designed to operate with a wide choice of crystals (from 9 MHz to 27 MHz). It is a common source configuration with current source loading to reduce power consumption. Refer to the *73M1822/73M1922 Data Sheet* (Section 7) for instructions on configuring the Crystal/PLL interface.

2.3 MAFE Interface

The host must use the MAFE interface for accessing all device registers. The final state of the both the TYPE, SCKM and M/S pin will affect the operational mode of the MAFE interface the user should be aware of their settings before attempting to program the device. Configurations such as daisy chain modes and control frame usage will require to user to write some register settings. Refer to the *73M1822/73M1922 Data Sheet* (Section 8) for instructions on configuring the MAFE interface.

2.4 Interrupts

The 73M1x22 devices provide a single hardware interrupt pin (active low – open drain) that goes active upon detection of any of several programmable hardware events within the 73M1x22. The interrupt pin is active and configured for operation upon reset of the 73M1x22. Because interrupts are enabled by default, the device will generate an interrupt as soon as reset is de-asserted (due to a barrier failure detect). The host application must be ready to service or safely ignore this interrupt before the de-assertion of reset. The recommended way to deal with the first interrupt after reset is to disable the interrupt generation until the system is ready to handle them (see Section 3.1.2 First Interrupt). Refer to the *73M1822/73M1922 Data Sheet* (Section 6.2) for instructions on configuring interrupts.

3 Device Configuration and Initialization

3.1 Host-Side Device (73M1902) Configuration

The Host-side device configuration and initialization includes the following steps:

1. Reset
2. First Interrupt
3. MAFE Interface Configuration
4. Clock and Sample Rate Management

3.1.1 Reset

Upon reset, the device will power up in the default state. See the *73M1822/73M1922 Data Sheet* for exact conditions of the default device state upon reset. The device will be ready within 100 µs after reset and the user should not attempt to interact with the device before then.

3.1.2 First Interrupt

As the default device settings allow for the reporting of device interrupts, after reset, the device will report an interrupt. The recommended way to deal with the first interrupt after reset is to ignore this interrupt until the user is able to communicate on the AMFE interface. After MAFE communication has been established it is recommended to disable the interrupt generation until the system is ready to handle them.

✓ Despite being in Register 0x05, ENAPOL is not an interrupt masking register and should not be disabled.

The registers used in this procedure are:

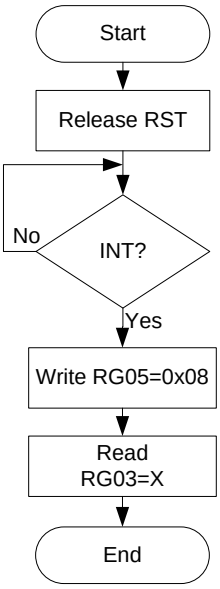
0x03	GPIO7	GPIO6	GPIO5	GPIO4	RGMON	DET	SYNL	RGDT
Read	X	X	X	X	X	X	X	X

0x05	ENGPIO7	ENGPIO6	ENGPIO5	ENGPIO4	ENAPOL	ENDET	ENSYNL	ENRGDT
Write	0	0	0	0	1	0	0	0

Begin

1. Release RST.
2. Wait for Interrupt.
3. Configure MAFE interface.
4. Set ENGPIO[7:4] = ENDET = ENSYNL = ENRGDT = 0, set ENAPOL = 1 (RG05 = 0x08).
5. Read RG03 to clear the register value and de-assert the INT pin.

End



3.1.3 MAFE Interface Configuration

R/W	ADDR	07	06	05	04	03	02	01	00
Write	0x01	DYSEN	NSLAVE[2:0]			MSIDEN	MSID	SCK32	
Write	0x02	TMEN					ENLPW	SPOS	HC

The MAFE interface must be properly configured by the user before the user can properly access the device. The device is powered up out of reset in a default state that may not match the final desired MAFE interface operating mode. The user must be able to operate in this default mode out of reset to configure the MAFE interface registers for proper long term stable operation. Refer to the *73M1822/73M1922 Data Sheet* (Section 8) for instructions on configuring the MAFE interface for optimal operation.

3.1.4 Clock and Sample Rate Management

The clock and sample rate are managed through a series of registers in the host side device. Refer to the *73M1822/73M1922 Data Sheet* (Section 7) for instructions on configuring the device registers for optimal operation in various clock and sample rates. Please note the Barrier and PLL can be expected to temporarily become out of Sync and Lock respectively during a Clock or Sample Rate change. Please note that, unlike and barrier sync loss due to an error condition, the user can assume the line side registers will preserve their contents during a sample rate change

R/W	ADDR	07	06	05	04	03	02	01	00
RW	0x08	PSEQ7	PSEQ6	PSEQ5	PSEQ4	PSEQ3	PSEQ2	PSEQ1	PSEQ0
RW	0x09	PRST2	PRST1	PRST0	PDVSR4	PDVSR3	PDVSR2	PDVSR1	PDVSR0
RW	0x0A	ICHP3	ICHP2	ICHP1	ICHP0	Reserved	KVCOH2	KVCOH1	KVCOH0
RW	0x0B	Reserved	NDVSR6	NDVSR5	NDVSR4	NDVSR3	NDVSR2	NDVSR1	NDVSR0
RW	0x0C	NSEQ7	NSEQ6	NSEQ5	NSEQ4	NSEQ3	NSEQ2	NSEQ1	NSEQ0
RW	0x0D	LOKDET	SLHS	Reserved	Reserved	CHNGFS	NRST2	NRST1	NRST0

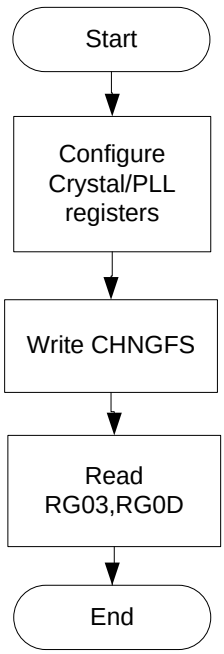
The temporary variables defined in this procedure are:

VAL1 = System appropriate values for RG08 → RG0D

Begin

1. Write RG08 → RG0D = VAL1.
2. Write CHNGFS = 1
3. Wait 10ms
4. Read RG03, RG0D.

END



3.2 Line-Side Device (73M1912) Configuration

The Line-side device setup includes the following procedures:

1. Barrier Synchronization
2. Initial Line State Configuration

3.2.1 Barrier Synchronization

Before the Line-side device can be initialized, the barrier must be in sync and error free. The barrier is designed to power up the line side device and come into sync automatically upon PLL lock. The Barrier may be expected to lose sync during an error condition or during a change in PLL settings (such as a sample rate change or during initialization). The user should check that the device indicates barrier sync before proceeding with line side initialization.

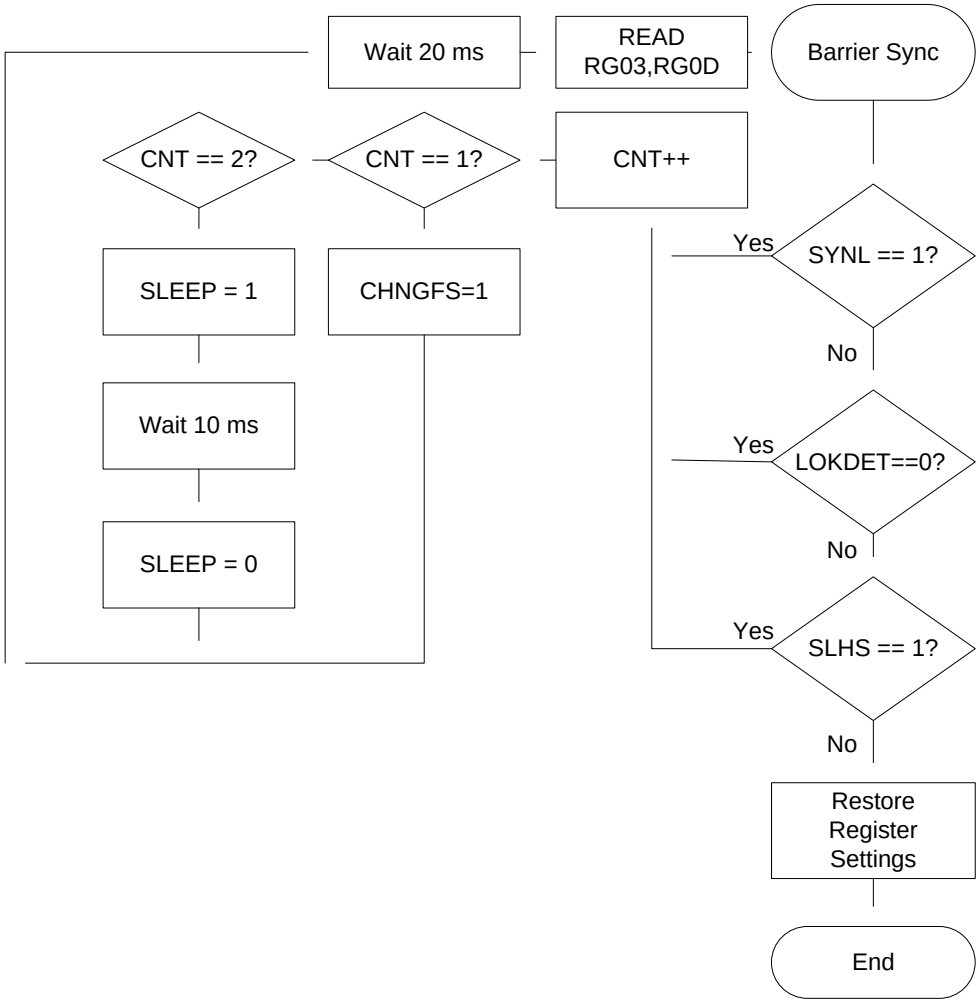
The following registers control the Barrier Synchronization procedure.

0x03	**GPIO7**	**GPIO6**	**GPIO5**	**PCLKDT**	**RGMON**	**DET**	**SYNL**	**RGDT**
Write	X	X	X	X	X	X	?	X

0x05	**ENGPIO7**	**ENGPIO6**	**ENGPIO5**	**ENGPIO4**	**ENAPOL**	**ENDET**	**ENSYNL**	**ENRGDT**
Write	X	X	X	X	X	X	1	X

0x0D	**LOKDET**	**SLHS**	**Res**	**Res**	**CHNGFS**	**NRST2**	**NRST1**	**NRST0**
Read	?	?	X	X	1/0	X	X	X

0x0F	**ENFEH**	**PWDN**	**SLEEP**	**Res**	**XIB1**	**XIB0**	**Res**	**Res**
Write	X	X	1/0	X	X	X	X	X



The temporary variables defined in this procedure are:

CNT1 = Resync Counter. Initial value = 0

Begin : BARRIER CHECK

1. Read RG03.
2. If SYNL == 0 goto RESYNC.
3. Read RG0D.
4. If LOKDET == 0 goto RESYNC.
5. If SLHS == 1 goto RESYNC.
6. Restore Previous Register Settings and go On Hook

END

Begin : RESYNC

1. IF CNT1 !=1 goto 8
2. Write CHNGFS = 1 (RG0D = xxxx_1xxx).
3. Wait 20 ms.
4. READ RGO3,RG0D
5. Goto BARRIER CHECK
6. IF CNT1 !=2 goto 15
7. Write SLEEP = 1 (RG0F = xx1x_xxxx).
8. Wait 10 ms.
9. Write SLEEP = 0 (RG0F = xx0x_xxxx).
10. Wait 10 ms.
11. READ RGO3,RG0D
12. Goto BARRIER CHECK
13. Resync Failed. Report to user and reset or power down entire device.

End

3.2.2 Initial Line State Configuration

The default condition of the device is to be on hook after reset and startup.

The registers used in this procedure are:

0x05	ENGPIO7	ENGPIO6	ENGPIO5	ENGPIO4	ENAPOL	ENDET	ENSYNL	ENRGDT
Write	X	X	X	X	1	X	1	X

0x12	OFH	ENDC	ENAC	ENSHL	$\overline{\text{ENLVD}}$	ENFEL	ENDT	ENNOM
Write	0	0	0	0	0	1	0	0

0x13	DCIV1	DCIV0	ILM	RSVD	PLDM	OVDTH	IDISPD1	IDISP0
Write	*VAL1[1:0]*		0	0	0	0	0	0

0x14	TXBST	DAA1	DAA0	Res	RXBST	RLPNH	RXG1	RXG0
Write	X	X	X	0	X	X	X	X

0x15	RSVD	DISNTR	Res	CIDM	THEN	ENUVD	ENOVD	ENOID
Write	0	0	0	0	1	0	0	0

0x16	TXEN	RXEN	RLPNEN	ATEN	FSCTR3	FSCTR2	FSCTR1	FSCTR0
Write	1	1	0	1	*VAL3[3:0]*			

0x17	APWS	Res	Res	ACZ1	ACZ0	Res	Res	Res
Write	0	0	0	VAL2[1:0]		0	0	0

The temporary variables defined in this procedure are:

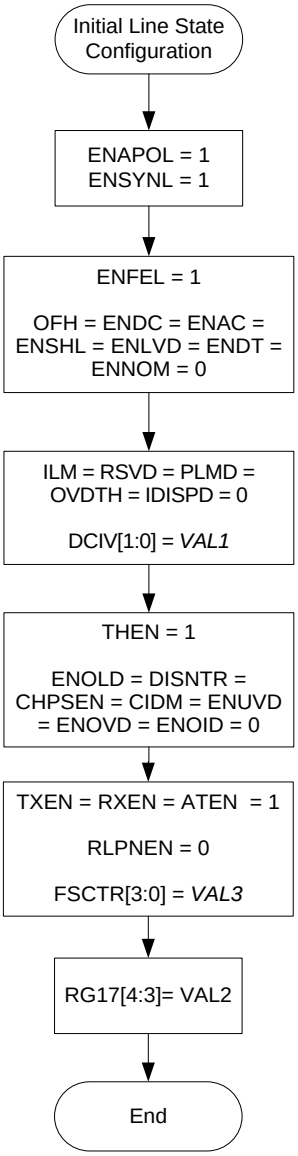
VAL1 = Set the DCIV bits to the desired DC current voltage characteristic as defined in the Data Sheet.
VAL2 = System appropriate value for ACZ[1:0].
VAL3 = System appropriate value for FSCTR[3:0].

Begin

1. Set ENAPOL =1 and ENSYNL = 1, to allow automatic polling of line side registers (write RG05 = xxxx_1x1x).
2. Set ENFEL = 1, OFH = ENDC = ENAC = ENSHL = $\overline{\text{ENVLD}}$ = ENDT = ENNOM = 0 (Write RG12 = 0x40).
3. Set ILM = RSVD = PLDM = OVDTH = IDISPD = Res = 0, DCIV = *VAL1* (Write RG13 = *Val1[1:0]*00_0000).
4. Write RG14 = xxx0_xxxx
5. Set THEN = 1, set ENOLD = DISNTR = CHPSEN = CIDM = ENUVD = ENOVD = ENOID = 0 (Write RG15 = 0000_1000)
6. Set TXEN = RXEN = ATEN = 1, RLPNEN = 0 and FSCTR[3:0] =*VAL3[3:0]* (Write RG16 = 1101_*VAL3[3:0]).*
7. Set RG17[4:3] = VAL2 (write RG17 = 0x000_VAL2_000).

End

After this point the host may selectively enable other on hook operations such as ring detection or CID mode.


Initial Line State Configuration
ENAPOL = 1
ENSYNL = 1
ENFEL = 1
OFH = ENDC = ENAC = ENSHL = ENLVD = ENDT = ENNOM = 0
ILM = RSVD = PLMD = OVDTH = IDISPD = 0
DCIV[1:0] = VAL1
THEN = 1
ENOLD = DISNTR = CHPSEN = CIDM = ENUVD = ENOVD = ENOID = 0
TXEN = RXEN = ATEN = 1
RLPNEN = 0
FSCTR[3:0] = VAL3
RG17[4:3]= VAL2
End

4 On-Hook Procedures

The on-hook procedures described in this section include:

- CID Mode
- Off-Hook Request
- Ring Detection and Line Voltage Reversal
- Line-in-use and Loss of Battery Feed

4.1 CID Mode

It is possible (while on hook) to allow the RGP/RGN input, which is AC coupled to the line through high voltage capacitors, to be transmitted on the MAFE interface. This allows the host to listen for Caller ID information without going off hook.

The registers used in this procedure are:

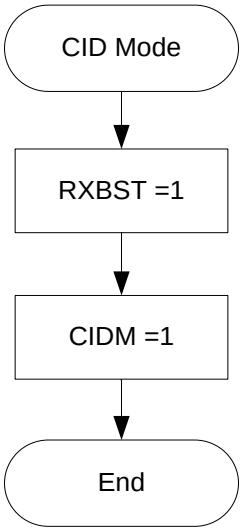
0x14	TXBST	DAA1	DAA0	Res	RXBST	RLPNH	RXG1	RXG0
Write	X	X	X	X	1	X	X	X

0x15	ENOLD	DISNTR	Res	CIDM	THEN	ENUVD	ENOVD	ENOID
Write	X	X	0	1	X	X	X	X

Begin

1. Set RXBST = 1 (Write RG14 = xxxx1xxx).
2. Set CIDM = 1 (write RG15 = xx11_xxxx).

End



4.2 Off-Hook Request

The registers used in the off-hook request procedure are:

0x12	OFH	ENDC	ENAC	ENSHL	$\overline{\text{ENLVD}}$	ENFEL	ENDT	ENNOM
Write	X/X/1/X	1/X/X/X	X/X/0 or 1/1	X	X	1/X/X/X	X	X/0/X/1

0x13	DCIV1	DCIV0	ILM	RSVD	PLDM	OVDTH	IDISPD	IDISPD
Write	*VAL1[1:0]*		X	X	X	X	X	X

0x14	TXBST	DAA1	DAA0	Res	RXBST	RLPNH	RXG1	RXG0
Write	X	X	X	X	0	X	X	X

0x15	Res	DISNTR	Res	CIDM	THEN	ENUVD	ENOVD	ENOID
Write	X	X	0	0/X	X/1	X	X	X

0x16	TXEN	RXEN	RLPNEN	ATEN	FSCTR3	FSCTR2	FSCTR1	FSCTR0
Write	X/1	X/1	X	X/1	*VAL2[3:0]* / X			

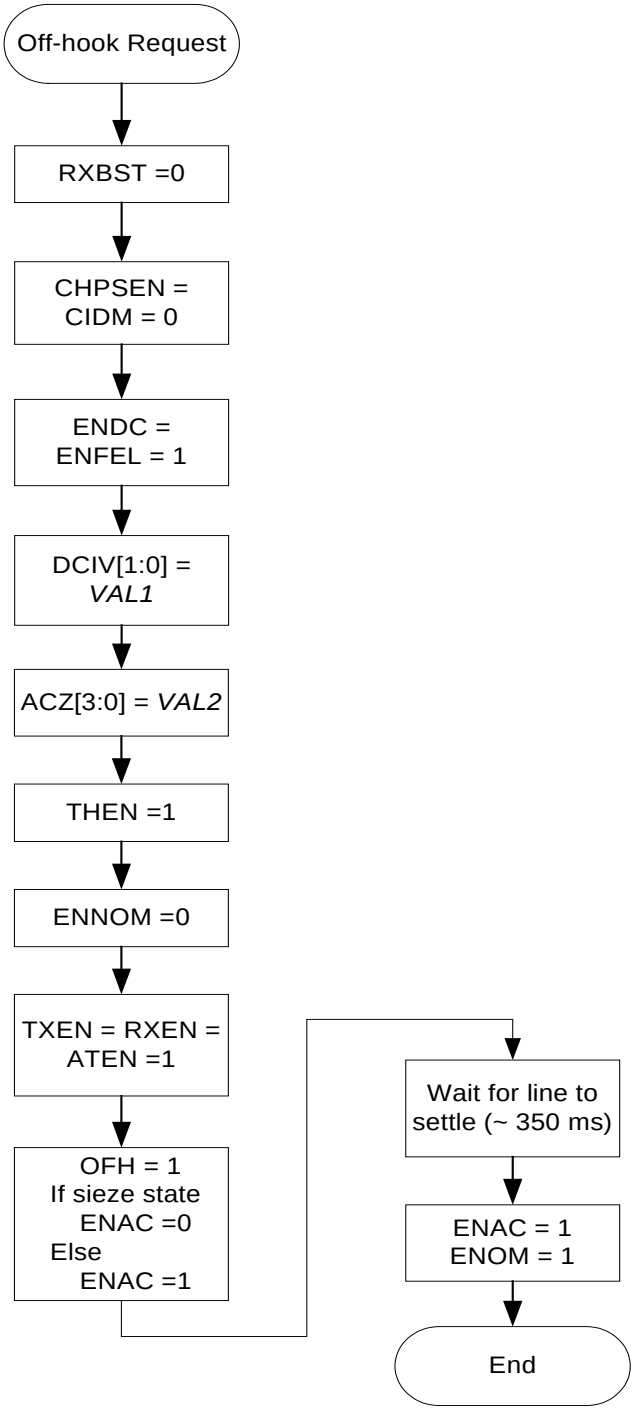
The temporary variables defined in this procedure are:

VAL1 = System appropriate value for DCIV[1:0].
VAL2 = System appropriate value for FSCTR[3:0].

Begin

1. Set RXBST = 0 (write xxxx_0xxx to RG14).
2. Set CHPSEN = CIDM = 0 (write xx00_xxxx to RG15).
3. Set ENDC = ENFEL =1 (write x1xx_x1xx to RG12).
4. Set DCIV[1:0] = *VAL1* (write *VAL1[1:0]*xx_xxxx to RG13).
5. Set FSCTR[3:0] = *VAL2* (write xxxx_*VAL2[3:0]* to RG16).
6. Set THEN = 1 (write xxxx_1xxx to RG15).
7. Set ENNOM = 0 (write xxxx_xxx0 to RG12).
8. Set TXEN = RXEN = ATEN = 1 (write 11x1_xxxx to RG16).
9. Set OFH = 1. If using sieze state, set ENAC =0 else set ENAC =1. (write 1x0x_xxxx or 1x1x_xxxx to RG12).
10. Wait until line settles (typical maximum is 350ms).
11. Set ENAC = ENNOM =1 (write xx1x_xxx1 to RG12).

End


Off-hook Request
RXBST =0
CHPSEN =
CIDM = 0
ENDC =
ENFEL = 1
DCIV[1:0] =
VAL1
ACZ[3:0] = *VAL2*
THEN =1
ENNOM =0
TXEN = RXEN =
ATEN =1
OFH = 1
If sieze state
ENAC =0
Else
ENAC =1
Wait for line to
settle (~ 350 ms)
ENAC = 1
ENOM = 1
End

4.3 Ring Detection and Line Voltage Reversal

When the 73M1922 is in on-hook mode, and when the ring detect interrupt is enabled (ENRGDT), a ring signal can be detected. Figure 1 shows the possible scenarios that can be encountered on the line.

The threshold voltage for detecting the ring signal is programmable in the 73M1x22 (RGTH[1:0]). When the line voltage exceeds the programmed threshold, the 73M1x22 asserts the hardware interrupt output pin ($\overline{INT}$) and asserts both RGDT and RGMON in the interrupt register, as illustrated by "1" and "3" in Figure 1. Note that the behavior is identical when the line voltage goes below the programmed threshold, as shown by "2" and "7" in Figure 1.

When the host reads the 73M1x22 interrupt register, RGDT is cleared, while RGMON remains asserted as long as:

1. The line voltage is above (or below) the upper (lower) threshold level shown in Figure 1 and
2. A time period of 25 ms has not elapsed after the line voltage crossed back over the threshold level. The activity of the timer ruling RGMON is indicated by "4" and "5" (as well as "8" and "9") in Figure 1.

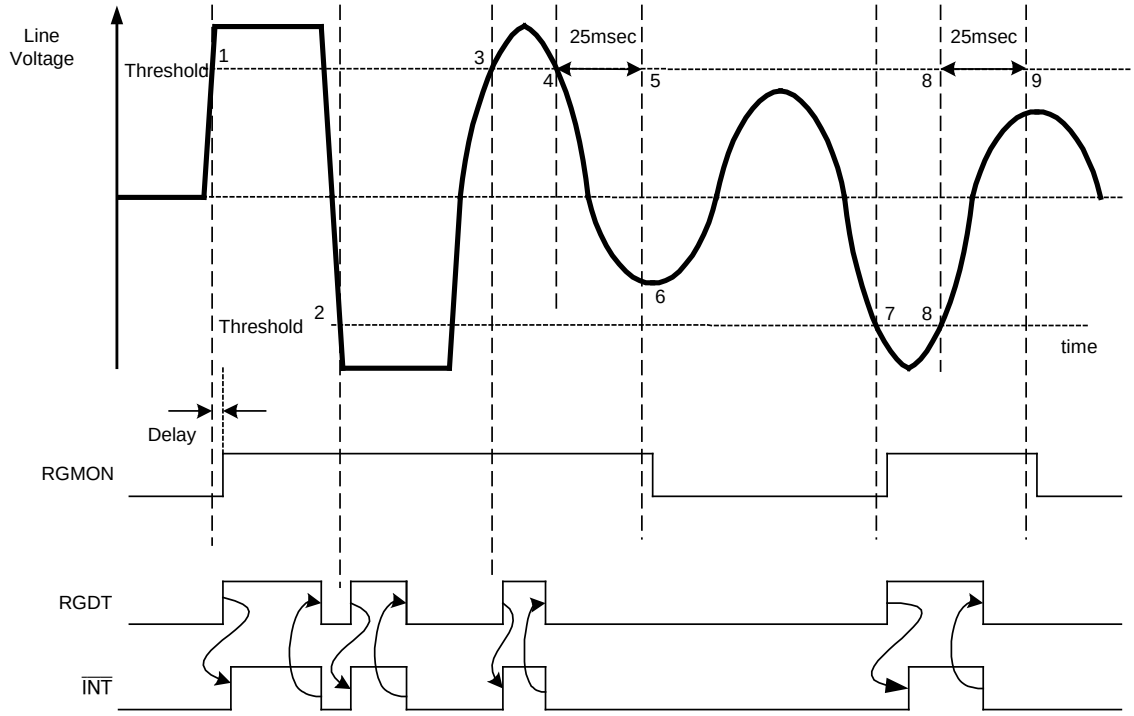


Figure 1: Ring Detection

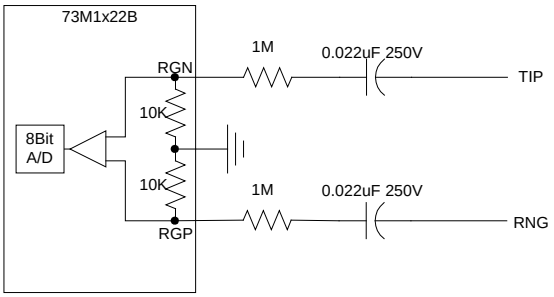


Figure 2 : Ring Circuit

If the line voltage does not exceed the threshold within the 25 ms period, RGMON becomes de-asserted, as illustrated by "6" and "9" in Figure 1.

Upon the first reception of the first RGDT interrupt, if no other ring interrupt was received during a sufficiently long period then it can be assumed that a Line Polarity Reversal has occurred. To filter out spurious ring events (from a parallel device going off hook or battery loss), the driver should check that the line voltage is the same as previously before determining that the single ring event was, in fact, a line polarity reversal.

The registers used for Ring Detection and Line Voltage Reversal are:

0x05	**ENGPIO7**	**ENGPIO6**	**ENGPIO5**	**ENGPIO4**	**ENAPOL**	**ENDET**	**ENSYNL**	**ENRGDT**
Write	X	X	X	X	X	X	X	1

0x0E	**FRCVCO**	**PWDNPLL**	**Res**	**Res**	**Res**	**Res**	**RGTH1**	**RGTH0**
Write	X	X	X	X	X	X	*Threshold*	

0x03	**GPIO7**	**GPIO6**	**GPIO5**	**GPIO4**	**RGMON**	**DET**	**SYNL**	**RGDT**
Write	X	X	X	X	X	X	X	*?*

Set the ring detect threshold voltage[1] (*Threshold*) in the RGTH[1:0] bits in Register 0x0E.
Set ENRGT = 1 in Register 0x05 to enable the RGMON and RGDT interrupts. See Section 6 Interrupt Processing for more information on interrupts.

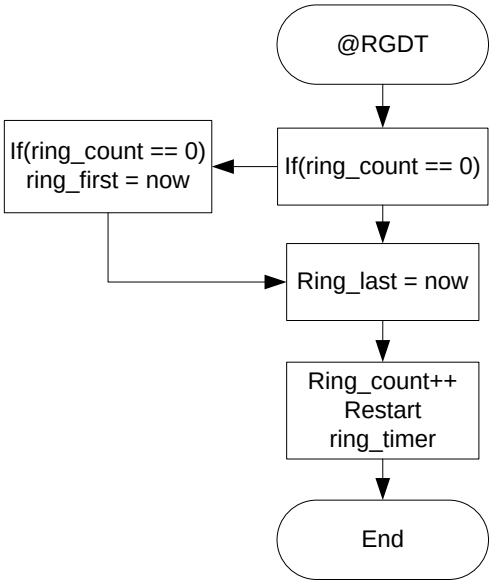
The system variables defined in this procedure are:

ring_count = initial 0, keeps track of number of ring interrupts
ring_first = time of first ring interrupt
ring_last = time of last ring interrupt
ring_frequency = ring frequency in HZ
ring_duration = ring duration

Begin @ RGDT interrupt (RGDT = 1)

1. If (*ring_count* == 0) *ring_first* = now;
2. *ring_last* = now
3. start/restart ring_timer for approx 150 ms

End

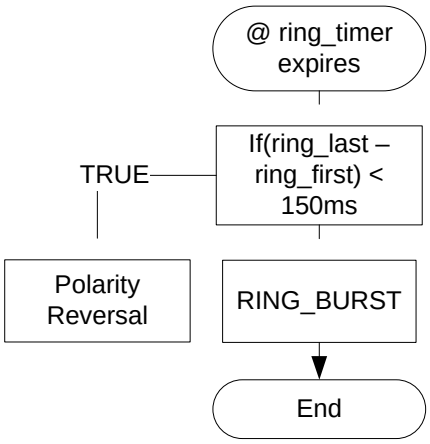


[1] The ring detect threshold is country specific. The recommended values are shown in the *73M1x22 Worldwide Design Guide.*

Begin @ ring_timer expires

1. If (*ring_last* - *ring_first*) < 150 ms Polarity Reversal Event
2. Else Ring Burst
   a. *ring_duration* = *ring_last* – *ring_first*
   b. *ring_frequency* – 2* *ring_count* / *ring_duration*)

End



4.4 Line-in-use and Loss of Battery Feed

When the FXO line is in the on-hook mode, the driver monitors the voltage on the line (typically 48 V in the US) at regular intervals. A loss of battery voltage or a line-in-use event can affect the value of the line voltage.

The loss of battery voltage results from disconnecting the phone line or a central office failure. In this case, the line voltage falls to zero volts after a time constant.

The line-in-use event occurs when another phone connected to that line is going off-hook. The line voltage drops to about 6 V when the line is in use.

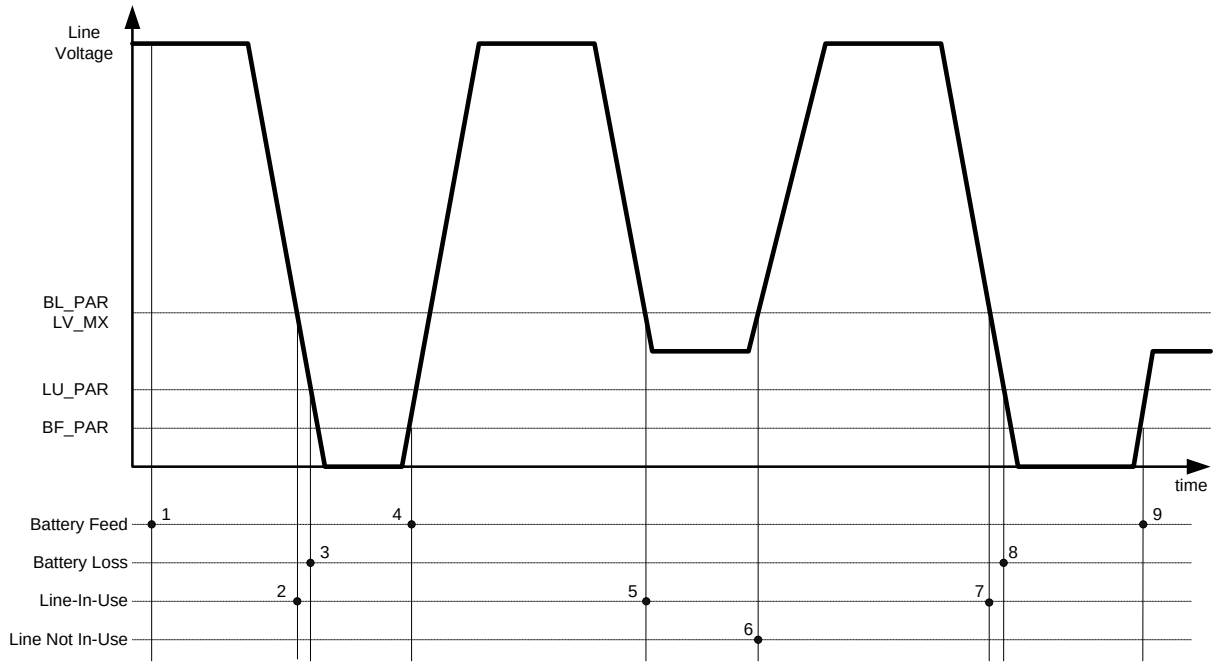


Figure 3 : Battery Feed and Line-in-Use Detection

The LV register (0x1B) can be polled to determine the line voltage. In an on hook case (and using the reference schematics) the line voltage can be calculated as follows:

*Line Voltage = ((LV[7:0] & 0xFE) * 1.13) + 1.4V*

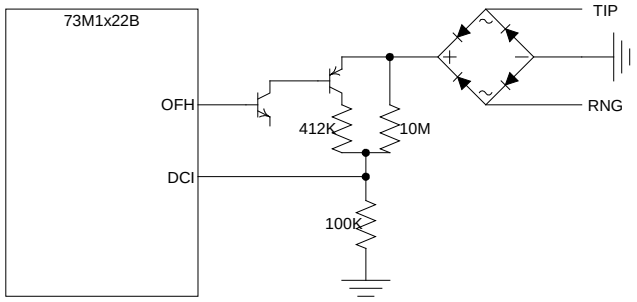


Figure 4: Line Voltage Measurement Circuit

The register which is read to determine the Line voltage is:

0x1B	LV7	LV6	LV5	LV4	LV3	LV2	LV1	Res
Read	*Line Voltage[7:1]*							

5 Off-Hook Procedures

The off-hook procedures described in this section include:

- Barrier Synch Loss
- On-hook Request
- Parallel Pickup Event Detection

5.1 Barrier Synch Loss

When in an off hook state the host must be ready to act in case of a barrier failure. The host should attempt to put the device in an on-hook state and then reset the PLL and barrier so they can resync.

The on-hook request procedure is described in Section 5.2. The procedure for barrier synchronization is described in Section 3.2.1.

5.2 On-hook Request

The registers used in the on-hook request procedure are:

0x12	OFH	ENDC	ENAC	ENSHL	$\overline{\text{ENLVD}}$	ENFEL	ENDT	ENNOM
Write	0	0	0	X	X	X	X	X

Begin

1. Set ENDC = ENAC = OFH = 0 (write RG12 = 000x_xxxx).

End

5.3 Parallel Pickup Event Detection

To be defined.

6 Interrupt Processing

During the course of operation the 73M1x22 can be expected to generate interrupts when errors or other events occur that require immediate action. Each interrupt source corresponds to a bit in register 0x03.

This section will cover each interrupt and the appropriate actions to process it. The registers used in the procedure are:

0x03	GPIO7	GPIO6	GPIO5	GPIO4	RGMON	DET	SYNL	RGDT
Read	?	?	?	?	?	?	?	?

0x05	ENGPIO7	ENGPIO6	ENGPIO5	ENGPIO4	ENAPOL	ENDET	ENSYNL	ENRGDT
Write	X	X	X	X	1	X	X	X

The temporary variables defined in the procedure are:

IntSrc = Interrupt sources (read from Register 0x03).
GPIO[7:4] bits indicate a GPIO Interrupt.
DET bit indicates a line condition error: DET Interrupt.
SYNL bit indicates a barrier failure: SYNL Interrupt.
RGMON and RGDT bits indicate a line signal detection: RGDT and RGMON Interrupts.

Begin

1. Wait for Interrupt.
2. Read Register 0x03 to determine the interrupt source(s), to clear the register value and de-assert the INT pin (*IntSrc* = RG03).
3. Read RG05 (IntMsk = RG05.
4. Set ENAPOL = 1 (write xxxx_1xxx to RG05).
5. Process each interrupt source.
6. Re-enable interrupts set RG05 = IntMsk.
7. goto 1.

End

6.1 GPIO Interrupt

GPIO interrupts are a user dependent function controlled through the POL and ENGPIO registers. Please refer to the *73M1822/73M1922 Data Sheet* for their individual functionality. The functional requirements of the software to handle a GPIO interrupt are user dependent.

0x05	ENGPIO7	ENGPIO6	ENGPIO5	ENGPIO4	ENAPOL	ENDET	ENSYNL	ENRGDT
Write	1	1	1	X	1	X	X	X

0x06	POL7	POL6	POL5	POL4	Res	Res	Res	Res
Write	0/1	0/1	0/1	0/1	X	X	X	X

Set the ENGPIO[7:5] bits of RG05 to enable the corresponding GPIO[7:4] interrupt(s).
Set the POL[7:4] bit of RG06 to the desired polarity.

Begin

1. If GPIO7 or GPIO6 or GPIO5 or GPIO4= 1 (*IntSrc*[7:4] ≠ 0) then goto user defined GPIO Interrupt Processing.

End

6.2 DET Interrupt

The triggering of the DET interrupt indicates that the device has detected one of several line condition errors. When found, it can be assumed that there is a problem with the line status. The general corrective action is for the line side device to go on hook. These interrupts are only valid when the device is in an off hook condition.

0x05	ENGPIO7	ENGPIO6	ENGPIO5	ENGPIO4	ENAPOL	ENDET	ENSYNL	ENRGDT
Write	X	X	X	X	1	1	X	X

0x12	OFH	ENDC	ENAC	ENSHL	$\overline{\text{ENLVD}}$	ENFEL	ENDT	ENNOM
Write	1	1	1	x	x	1	1	x

0x13	DCIV1	DCIV0	ILM	RSVD	PLDM	OVDTH	IDISPD	IDISPD
Write	X	X	0	0	0	1/0	0	0

0x14	TXBST	DAA1	DAA0	Res	RXBST	RLPNH	RXG1	RXG0
Write	X	X	X	0	X	X	X	X

0x15	Res	DISNTR	Res	CIDM	THEN	ENUVD	ENOVD	ENOID
Write	0	0	0	0	1	1	1	1

0x1E	ILMON	UVDET	OVDET	OIDET	SLLS	Res	Res	Res
Read	X	?	?	?	X	X	X	X

Set the ENDET bit in Register 0x05 to enable the DET interrupt.

Begin

1. If DET = 1 (*IntSrc* = xxxx_x1xx).
2. Read RG1E
3. If OVDET = 1, report condition to user and put device on hook.
4. If OIDET = 1, report condition to user and put device on hook
5. If UVDET = 1, report condition to user and put device on hook

End

6.3 SYNL Interrupt

The triggering of the SYNL interrupt indicates that the device has detected a failure in the barrier between the line and host side device. When found, it can be assumed that there is a problem with the barrier. This failure is usually a problem with the PLL operation, therefore, the recommended way to deal with this interrupt is to reset the device PLL.

0x05	ENGPIO7	ENGPIO6	ENGPIO5	ENGPIO4	ENAPOL	ENDET	ENSYNL	ENRGDT
Write	X	X	X	X	1	X	1	X

Set the RNSYNL bit in Register 0x05 to enable the SYNL interrupt.

Begin

1. If SYNL = 1 (*IntSrc* = xxxx_xx1x), goto Barrier Synchronization Process (see Barrier Synchronization Section 3.2.1)

End

6.4 RGDT and RGMON Interrupts

The triggering of an RGDT or RGMON interrupt indicates that the device has detected an AC signal on the line greater than the threshold programmed through the RGTH register.

0x05	ENGPIO7	ENGPIO6	ENGPIO5	ENGPIO4	ENAPOL	ENDET	ENSYNL	ENRGDT
Write	X	X	X	X	1	X	X	1

0x0E	FRCVCO	PWDNPLL	Res	Res	Res	Res	RGTH1	RGTH0
Write	X	X	X	X	X	X	*VAL1[1:0]*	

Set the ENRGDT bit in Register 0x05 to enable the RGDT and RGMON interrupts.

Begin

1. If RGDT = 1 (*IntSrc* = xxxx_xxx1) or RGMON = 1 (*IntSrc* = xxxx_1xxx), goto Ring Detection and Line Polarity Reversal (see Section 4.3).

End

7 Register Summary

Address (hex)	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	00h/9Ch	DSYEN	NSLAVE2	NSLAVE1	NSLAVE0	MSIDEN	MSID	SCK32	Reserved
02	00h	TMEN	Reserved	Reserved	Reserved	Reserved	ENLPW	SPOS	HC
03	F0h	GPIO7	GPIO6	GPIO5	GPIO4	RGMON	DET	SYNL	RGDT
04	F7h	DIR7	DIR6	DIR5	DIR4	REVHSD3	REVHSD2	REVHSD1	REVHSD0
05	0Bh	ENGPIO7	ENGPIO6	ENGPIO5	ENGPIO4	ENAPOL	ENDET	ENSYNL	ENRGDT
06	00h	POL7	POL6	POL5	POL4	Reserved	Reserved	Reserved	Reserved
07	00h	Reserved	Reserved	Reserved	Reserved	DTST3	DTST2	DTST1	DTST0
08	DAh	PSEQ7	PSEQ6	PSEQ5	PSEQ4	PSEQ3	PSEQ2	PSEQ1	PSEQ0
09	EFh	PRST2	PRST1	PRST0	PDVSR4	PDVSR3	PDVSR2	PDVSR1	PDVSR0
0A	31h	ICHP3	ICHP2	ICHP1	ICHP0	Reserved	KVCOH2	KVCOH1	KVCOH0
0B	2Ah	Reserved	NDVSR6	NDVSR5	NDVSR4	NDVSR3	NDVSR2	NDVSR1	NDVSR0
0C	06h	NSEQ7	NSEQ6	NSEQ5	NSEQ4	NSEQ3	NSEQ2	NSEQ1	NSEQ0
0D	42h	LOKDET	SLHS	Reserved	Reserved	CHNGFS	NRST2	NRST1	NRST0
0E	00h	FRCVCO	PWDNPLL	Reserved	Reserved	Reserved	Reserved	RGTH1	RGTH0
0F	2Ch	ENFEH	PWDN	SLEEP	Reserved	XIB1	XIB0	Reserved	Reserved
10	00h	Reserved	Reserved	Reserved	CMVSEL	CMTXG1	CMTXG0	CMRXG1	CMRXG0
12	00h	OFH	ENDC	ENAC	ENSHL	$\overline{\text{ENLVD}}$	ENFEL	ENDT	ENNOM
13	00h	DCIV1	DCIV0	ILM	ACCEN	PLDM	OVDTH	IDISPD1	IDISPD0
14	00h	TXBST	DAA1	DAA0	Reserved	RXBST	RLPNH	RXG1	RXG0
15	00h	Reserved	DISNTR	Reserved	CIDM	THEN	ENUVD	ENOVD	ENOID
16	01h	TXEN	RXEN	RLPNEN	ATEN	FSCTR3	FSCTR2	FSCTR1	FSCTR0
17	00h	APWS	Reserved	Reserved	ACZ1	ACZ0	Reserved	Reserved	Reserved
18	01h	TEST3	TEST2	TEST1	TEST0	Reserved	Reserved	Reserved	Reserved
19	00h	POLL	MATCH	Reserved	IDL2	INDX3	INDX2	INDX1	INDX0
1A	00h	RNG7	RNG6	RNG5	RNG4	RNG3	RNG2	RNG1	RNG0
1B	00h	LV7	LV6	LV5	LV4	LV3	LV2	LV1	Reserved
1C	00h	LC6	LC5	LC4	LC3	LC2	LC1	LC0	Reserved
1D	90h	REVLSD3	REVLSD2	REVLSD1	REVLSD0	Reserved	Reserved	Reserved	Reserved
1E	00h	ILMON	UVDET	OVDET	OIDET	SLLS	Reserved	Reserved	Reserved
1F	00h	POLVAL7	POLVAL6	POLVAL5	POLVAL4	POLVAL3	POLVAL2	POLVAL1	POLVAL0

8 Related Documentation

The following 73M1x22 documents are available from Teridian Semiconductor Corporation:

73M1822/73M1922 Data Sheet
73M1822/73M1922 Demo Board User Manual
73M1822/73M1922 GUI User Guide
73M1822/73M1922 Layout Guidelines
73M1x22 Worldwide Design Guide
73M1822/73M1922 Programming Guidelines
73M1822/73M1922 Reference Driver User Guide

9 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73M1822 and 73M1922, contact us at:

6440 Oak Canyon Road
Suite 100
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: modem.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	8/27/2009	First publication.