### DPD/PA TEST REPORT

<table>
<thead>
<tr>
<th>RF Transceiver</th>
<th>AD9375</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Amplifier</td>
<td>A2I20H040N</td>
</tr>
<tr>
<td>PA Type</td>
<td>Asymmetrical Doherty</td>
</tr>
<tr>
<td>Transistor Type</td>
<td>LDMOS</td>
</tr>
<tr>
<td>Operating Frequency Range (MHz)</td>
<td>758-803 MHz (B28, B14 Tx)</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>55 dB</td>
</tr>
<tr>
<td>Power Added Efficiency</td>
<td>45 % (nom)</td>
</tr>
<tr>
<td>Psat</td>
<td>47.5 dBm (nom)</td>
</tr>
<tr>
<td>Pavg</td>
<td>39.5 dBm (nom)</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>28 V</td>
</tr>
<tr>
<td>Signal Bandwidths Tested</td>
<td>10 MHz &amp; 20 MHz</td>
</tr>
</tbody>
</table>
SUMMARY

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Output Power (dBm)</th>
<th>Signal Bandwidth</th>
<th>Test Signal</th>
<th>ACLR +1 (dBc)</th>
<th>ACLR-1 (dBc)</th>
<th>ACLR+2 (dBc)</th>
<th>ACLR-2 (dBc)</th>
<th>Power Added Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>763 MHz (Low)</td>
<td>39.75</td>
<td>10 MHz</td>
<td>ETM3.1</td>
<td>-51.36</td>
<td>-51.35</td>
<td>-58.82</td>
<td>-58.15</td>
<td>49.6 %</td>
</tr>
<tr>
<td>790 MHz (High)</td>
<td>39.55</td>
<td>10 MHz</td>
<td>ETM3.1</td>
<td>-53.01</td>
<td>-51.88</td>
<td>-57.99</td>
<td>-55.09</td>
<td>45.4 %</td>
</tr>
<tr>
<td>790 MHz (High)</td>
<td>39.4</td>
<td>20 MHz</td>
<td>ETM3.1</td>
<td>-51.65</td>
<td>-50.13</td>
<td>-56.54</td>
<td>-52.49</td>
<td>47.1 %</td>
</tr>
</tbody>
</table>

SYSTEM BLOCK DIAGRAM

A high-level system block diagram of the DE705 RF Frontend and the interface to the ADRV9371/9375 Transceiver board + Xilinx Zync706 FPGA board is shown below in Fig 1.

Software GUI’s for this platform exists for the AD9371/9375 TES (Transceiver Evaluation Software), the AD9375 DPD and for the DE705. The DE705 GUI is provided to set the proper DC Bias of the PA as well as the Phase and Attenuation settings of the Advanced Doherty Alignment Module (ADAM) IC to optimize performance of the A2I08H040N PA.

Figure 1. High Level Systems Block Diagram
DE705 RF FRONTEND BLOCK DIAGRAM

A detailed block diagram of the key functional blocks that comprise the DE705 RF Frontend is illustrated below in Figure 2.

Figure 2. DE705 RF Frontend Block Diagram

DE705 HW Test Setup
Figure 3. DE705 + AD9375 DPD Test Setup

SW GUIs for:
- 9371/75 TES
- AD9375 DPD
- DE705
ACLR TEST RESULTS - LOW BAND
763 MHZ, 10MHZ BANDWIDTH - ACLR

Before DPD

Figure 4. Frequency 763MHz, 10MHz ETM3.1 Spectrum Analyzer Plot Before DPD
After DPD

![Spectrum Analyzer Plot](image)

**Figure 5. Frequency 763MHz, 10MHz ETM3.1 Spectrum Analyzer Plot After DPD Correction**

<table>
<thead>
<tr>
<th>Before/After DPD</th>
<th>Output Power (rms)</th>
<th>ACLR+1 (dBc)</th>
<th>ACLR-1 (dBc)</th>
<th>ACLR+2 (dBc)</th>
<th>ACLR-2 (dBc)</th>
<th>Drain Current (A)</th>
<th>PAE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before DPD</td>
<td>39.75 dBm</td>
<td>-29.85</td>
<td>-31.77</td>
<td>-44.93</td>
<td>-47.02</td>
<td>0.68</td>
<td>49.6</td>
</tr>
<tr>
<td>After DPD</td>
<td>39.75 dBm</td>
<td>-51.36</td>
<td>-51.35</td>
<td>-58.82</td>
<td>-58.15</td>
<td>0.68</td>
<td>49.6</td>
</tr>
</tbody>
</table>

*Table 1. Summary of Results: Frequency: 763 MHz, 10MHz ETM3.1 Signal*

**Bias and ADAM Settings for A2I08H040N PA (763 MHz, 10MHz BW):**

**Carrier:**
- VGS1A: 4.416 V
- VGS2A: 4.077 V
- IDS1A: 26.4 mA
- IDS2A: 95.6 mA

**Peaking:**
- VGS1B: 2.4 V
- VGS2B: 2.2 V
- IDS1B: 1.0 mA
- IDS2B: 1.0 mA

**ADAM:**
- Carrier Phase: -7 Deg
- Carrier ATTN: 5.5 dB
- Peaking Phase: -14 Deg
- Peaking ATTN: 0 dB
ACLR TEST RESULTS - HIGH BAND
790 MHZ, 10MHZ BANDWIDTH ACLR RESULTS

Before DPD

Figure 6. Frequency 790 MHz, 10MHz ETM3.1 Spectrum Analyzer Plot Before DPD Correction
After DPD

Figure 7. Frequency 790 MHz, 10MHz ETM3.1 Spectrum Analyzer Plot After DPD Correction

<table>
<thead>
<tr>
<th>Before/After DPD</th>
<th>Output Power (rms)</th>
<th>ACLR+1 (dBc)</th>
<th>ACLR-1 (dBc)</th>
<th>ACLR+2 (dBc)</th>
<th>ACLR-2 (dBc)</th>
<th>Drain Current (A)</th>
<th>PAE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before DPD</td>
<td>39.77</td>
<td>-30.89</td>
<td>-28.43</td>
<td>-45.85</td>
<td>-43.97</td>
<td>0.74</td>
<td>45.8</td>
</tr>
<tr>
<td>After DPD</td>
<td>39.77</td>
<td>-51.56</td>
<td>-50.67</td>
<td>-56.18</td>
<td>-53.26</td>
<td>0.74</td>
<td>45.8</td>
</tr>
</tbody>
</table>

Table 2. Summary of Results: Frequency: 790MHz, 10MHz ETM3.1 Signal

Bias and ADAM Settings for A2108H040N PA (790 MHz, 10 MHz BW):

Carrier: VGS1A: 4.416 V, VGS2A: 4.172 V
IDS1A: 26.4 mA, IDS2A: 105 mA

Peaking: VGS1B: 2.4 V, VGS2B: 2.2 V
IDS1B: 1.0 mA, IDS2B: 1.0 mA

ADAM: Carrier Phase: -28 Deg, Carrier ATTN: 5.5 dB
Peaking Phase: 0 Deg, Peaking ATTN: 0 dB
ACLR TEST RESULTS - HIGH BAND
790 MHZ, 20MHZ BANDWIDTH ACLR RESULTS

Before DPD

Figure 8. Frequency 790 MHz, 20MHz ETM3.1 Spectrum Analyzer Plot Before DPD Correction
After DPD

Figure 9. Frequency 790 MHz, 20MHz ETM3.1 Spectrum Analyzer Plot After DPD Correction

<table>
<thead>
<tr>
<th>Before/After DPD</th>
<th>Output Power (rms)</th>
<th>ACLR+1 (dBc)</th>
<th>ACLR-1 (dBc)</th>
<th>ACLR+2 (dBc)</th>
<th>ACLR-2 (dBc)</th>
<th>Drain Current (A)</th>
<th>PAE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before DPD</td>
<td>39.75</td>
<td>-31.94</td>
<td>-27.57</td>
<td>-46.61</td>
<td>-43.2</td>
<td>0.74</td>
<td>45.6</td>
</tr>
<tr>
<td>After DPD</td>
<td>39.75</td>
<td>-52.14</td>
<td>-50.50</td>
<td>-57.55</td>
<td>-52.65</td>
<td>0.74</td>
<td>45.6</td>
</tr>
</tbody>
</table>

Table 3. Summary of Results: Frequency: 790MHz, 20MHZ ETM3.1 Signal

**Bias and ADAM Settings for A2I08H040N PA (790 MHz, 20 MHz BW):**

**Carrier:**
- VGS1A: 4.416 V
- VGS2A: 4.072 V
- IDS1A: 25.9 mA
- IDS2A: 98.6 mA

**Peaking:**
- VGS1B: 2.4V
- VGS2B: 2.2 V
- IDS1B: 1.0 mA
- IDS2B: 1.0 mA

**ADAM:**
- Carrier Phase: -35 Deg
- Carrier ATTN: 5.5 dB
- Peaking Phase: 0 Deg
- Peaking ATTN: 0 dB
PA WIDEBAND LS GAIN VS FREQUENCY

Figure 10. Wideband PA Large Signal Gain Plot