Explaining SAR ADC Power Specifications

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One of the mysteries—or at least the cause of considerable confusion—of successive approximation register (SAR) ADCs is calculating their exact power requirements at the system level. Data sheets can be confusing on this specification.

SAR ADCs provide a low power means to measure input signals. Very often, the power consumption scales with the sample rate, making for a very efficient measurement system. This means that in order to calculate the total power consumption of the ADC, all supply pins need to be taken into account.

Typically, on SAR converters, there are three potential power consuming rails: the V_{DD} supply, the reference input, and the digital interface I/O supply.

The V_{DD} supply provides power to the analog circuitry and ADC core.

On SARs that require an external reference, the reference input is a switched capacitor that consumes charge current during the SAR conversion bit trials. This can be a significant source of power consumption, depending on the ADC throughput rate and size of the internal capacitor DAC. The higher the ADC throughput, the more conversion bit trials (charging of caps), and therefore, more current is consumed in the capacitive DAC array.

Similarly, a larger capacitor DAC means more capacitance to charge, which results in a higher current draw. If the cap DAC is large, it may pose a problem to the reference drive circuit, and a higher power reference circuit may be required. The same is true for the analog input, in which a more powerful driving amplifier may be required to drive the higher capacitive DAC load during acquisition. Sometimes additional circuitry related to the analog input can be powered from the reference, which can further add to power consumption. Some ADCs have an internal reference buffer that gives the reference input high impedance. In this scenario, the buffer supplies the necessary reference current through another supply pin.

The digital I/O supply consumes power depending on the throughput/output data rate, as well as load conditions on the data output lines. Again, higher ADC throughput means more power consumed by the digital I/O, due to the higher clock rates required to transfer the converted data. Any capacitive loading on the data output lines will increase the digital I/O current because of charging and discharging. Digital I/O current will also be output code dependent; the worst case in which alternate ones and zeros are the output. Typically, the digital I/O current should be measured with a signal present that exercises most of the ADC output codes, such as a sinusoidal input. In high throughput ADCs with high clock rates, the power consumed by the digital interface can become quite significant.

Many data sheets will quote power for the V_{DD} supply only. You have to dig into the specification table to determine the reference and digital supply power requirements. To get an accurate measure of the power consumption from a system-level perspective, all three inputs need to be considered.

Table 1. Example Power Dissipation from ADI's AD7980 Data Sheet

Parameter	Conditions	Min	Typ	Max	Unit
Power Dissipation	V_{DD} = 2.625 V, V_{REF} = 5 V, VIO = 3 V				
Total	10 kSPS throughput		70		μW
	1 MSPS throughput, B Grade		7.0	9.0	mW
	1 MSPS throughput, A Grade		7.0	10	mW
V_{DD} Only			4		mW
REF Only			1.7		mW
VIO Only			1.3		mW

When it comes to data sheets, especially with something as important as power consumption, all specifications need to be taken into account and stated separately like the AD7980 16-bit, 1 MSPS PulSAR® ADC shown above.

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