Digital PWM Controller and Current Estimator for A Low-Power Switching Converter

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Abstract **- This paper describes design and implementation of a digital controller for an experimental low-power converter in a battery-powered system with power management. Multiple operating modes are used to maintain high efficiency over wide ranges of input voltages and loads. A current estimation technique to perform load-dependent mode switching is proposed and tested. A digital PID regulator design example is described, with emphasis on practical limitations imposed by the fixed-point arithmetic and the delay due to sampling and processing.**

I. INTRODUCTION

It is expected that digital controllers will increasingly replace currently predominant analog controllers in high-frequency switch-mode power supply applications. Potential advantages of digital controller implementation include much improved flexibility, reduced design time, programmability, elimination of discrete tuning components, improved system reliability, easier system integration, and possibility to include various performance enhancements. With advances in DSP technology, significant amount of processing is available even at relatively high switching frequencies. However, in addition to cost issues, problems with digital controller realizations are related to limited resolution of pulse-width modulators, effects of fixed-point arithmetic, as well as delays introduced by sampling and processing.

In this paper, we consider implementation of a digital controller for a low-power converter in a battery-powered system with power management. It is required to maintain tight voltage regulation and high efficiency over a wide range of loads. To meet these requirements, and to demonstrate potential benefits of a digital controller implementation, a converter with multiple operating modes was used in this application.

The converter configuration is introduced in Section II, together with the experimental test system. The controller configuration is described in Section III. A current estimator used to enable load-dependent mode switching is introduced in Section IV. Section V gives details of the digital regulator design, together with experimental results.

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II. CONVERTER TOPOLOGY AND OPERATING MODES

The application example considered in this paper is a DC-DC converter for a battery-powered system with power management. The input voltage is in the range from 2V to 5V (such as from a single-cell Li-Ion battery). The output voltage is tightly regulated at 3V. The system has two modes of operation: "run" or heavy-load mode, when the load current is in the 1-2A range, and "stand-by" or light-load mode when the load current is in the 10-150mA range. It is desired to maintain tight voltage regulation and high efficiency in both heavy and light load modes.

The converter topology selected for the application is the non-inverting buck-boost shown in Fig. 1. This topology has only two passive components and can work as a buck, a boost or a buck-boost, depending on the driving sequence.

The experimental test system was based on the Analog Devices ADMC-401 DSP development board, as shown in Fig. 1. ADMC-401 is based on a 26 MIPS, 16-bit fixed-point digital signal processor. Intended for motor control applications, it has a range of peripherals including eight A/D converters, and three independent pulse-width modulators, two of which are used in our application. The effective duty-cycle resolution of the system's pulse-width modulators drops with increasing switching frequency. The switching frequency of f_s=50KHz was selected to have 8-bit resolution in the output duty ratios.

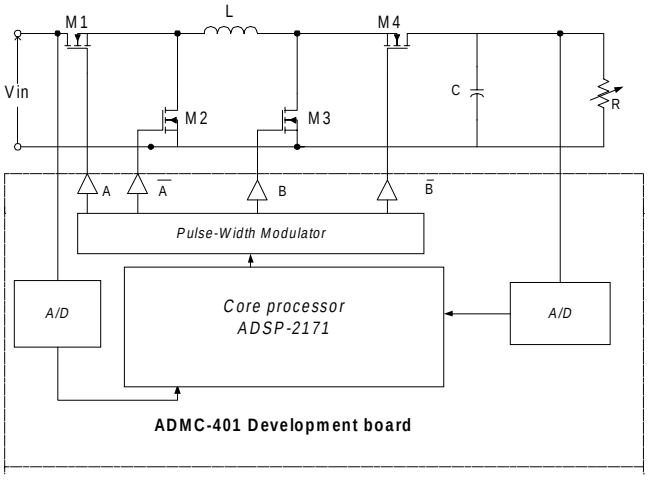

Fig.1. Non-inverting buck-boost converter with a digital controller.

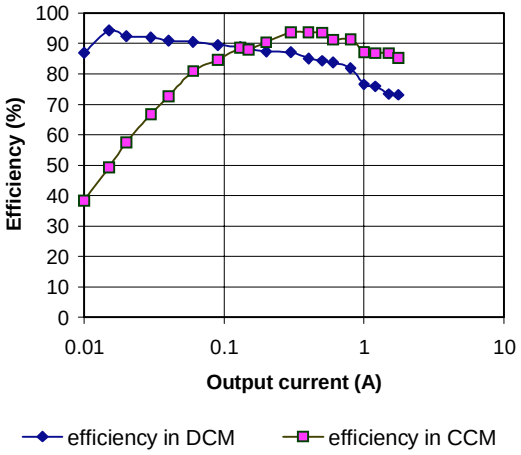

Fig.2. Efficiency of the converter operating in CCM at 50KHz and in DCM at 20KHz.

A. Operating Modes

When the input voltage is greater than the output, the converter is operated as a buck converter: M3 is always off, M4 is always on, M1 is switched at constant frequency with duty cycle D_{buck}, and M2 operates as a synchronous rectifier. When the input voltage is smaller than the output, the converter is operated as a boost: M1 is always on, M2 is always off, M3 is switched periodically with duty cycle D_{boost}, and M4 works as a synchronous rectifier. It is interesting to compare the converter of Fig. 1 to a conventional, two-switch buck-boost converter. The transistor conduction losses are comparable even though the non-inverting buck-boost has two active devices conducting the inductor current in each switching subinterval. The volt-seconds applied to the inductor, and the RMS inductor current are significantly smaller in the non-inverting buck-boost converter of Fig. 1 when it is operated in the buck or in the boost mode. Therefore, a smaller inductor can be used, at the expense of more active devices and a more complicated controller.

When the load is heavy, the converter is designed to operate in the continuous conduction mode (CCM) at constant switching frequency f_s=50KHz. Experimentally measured efficiency as a function of the load current is shown in Fig. 2. The efficiency is high at heavy load, but it drops to low values at light load. This is because the light-load losses are dominated by switching losses that are essentially independent of the load current. The light-load efficiency can be significantly improved by operating the converter in the discontinuous conduction mode, and by reducing the switching frequency [1]. Fig. 2 also shows the efficiency measured when the converter is operated in DCM at a reduced switching frequency f_{DCM}=20KHz. The efficiency curves for the two modes intersect at the load current of about 150mA. Based on the results of Fig. 2, we decided to apply mode switching depending on the load current: in the heavy-load mode, the converter is operated at high frequency in CCM; in the light-load mode, the converter is operated at low frequency in DCM. Constant-frequency, duty-ratio control is used for the output voltage regulation in both modes.

B. Converter Dynamics

In each of the four possible modes of operation (CCM-buck, CCM-boost, DCM-buck, DCM-boost), the converter ac equivalent circuit model and transfer functions can be obtained using standard averaging techniques [2]. For example, the CCM-buck exhibits a second-order control-to-output frequency response,

$$G_{vd}(s) = G_{d0}\frac{1}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \qquad (1)$$

The response in boost-CCM has a pair of complex-conjugate poles, and a RHP zero. In contrast, the response in buck-DCM and in boost-DCM is dominated by a single pole at low frequencies. Furthermore, in all modes, corner frequencies and gains depend on steady-state operating conditions.

To summarize, challenges in the controller design include: mode switching depending on the input voltage (buck/boost) and the load current (CCM/DCM), and the regulator design to handle different converter dynamics in different operating modes. A digital controller has clear advantages over analog realizations in addressing these challenges.

III. Controller Configuration

The proposed digital controller configuration is shown in Fig. 3. The output voltage is sensed and compared to a reference. The error signal is the input to a PID regulator. The regulator output $x=c$ is the control input to the pulse-width modulators A (for the buck switches M1 and M2) and B (for the boost switches M3 and M4). A current estimator and a mode

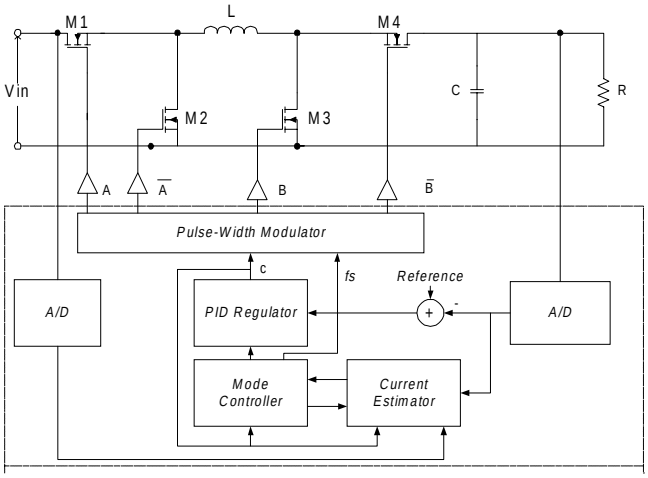

Fig.3. Controller configuration.

controller are used to enable the mode switching and changes of the control law and the regulator parameters to handle different converter dynamics. The current estimator is described in more detail in Section IV. The mode controller determines the switching sequence and the switching frequency. For example, in buck-DCM, M3 is always off, M4 is always on, M2 operates as a diode, while M1 is switched at f_{DCM}=20KHz. If, based on the current estimator calculations, it becomes necessary to switch from buck-DCM to buck-CCM, the mode controller increases the switching frequency to f_s=50KHz, and enables complementary switching of M1 and M2, so that M2 operates as a synchronous rectifier.

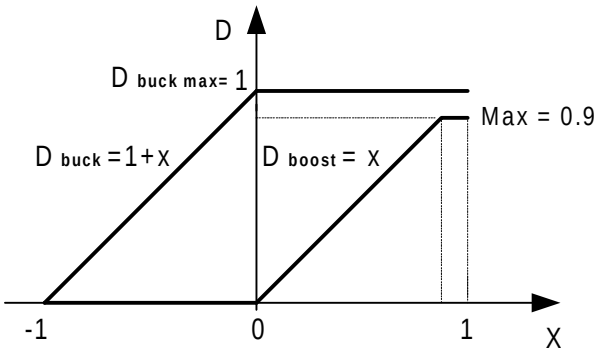

Fig.4. Buck and boost duty ratios as functions of the PID regulator's output *x*.

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Switching between the buck and the boost modes is accomplished using two pulse-width modulators with the common control input *x*. The buck and the boost duty ratios, D_{buck} and D_{boost}, respectively, as functions of the PID regulator output *x* are shown in Fig. 4. For negative values of *x*, the converter is in the buck mode, the boost duty ratio is zero, and the buck duty ratio is equal to *1+x*. For positive *x*, the converter is in the boost mode, the buck duty ratio equals one, and the boost duty ratio is equal to *x*. This simple scheme results in smooth buck/boost mode transition and simple regulator implementation using the single control variable *x*. The buck/boost mode switching based on the control variable *x* available in the closed-loop system does not require knowledge of the input voltage.

IV. Current estimation and CCM/DCM mode switching

For the purpose of the load-dependent (CCM/DCM) mode switching described in Section II.A, it is necessary to have information about the load current. In low-power converters, it is a common practice to sense the switch or the inductor current using a sense resistor. Problems associated with the current sensing include handling large common-mode switching noise in the sensed signal, and additional power losses on the sense resistor. To eliminate the need to sense the current, an analog current estimation technique was used in [3]. Here we propose a simple load current estimation technique that takes advantage of the digital controller implementation.

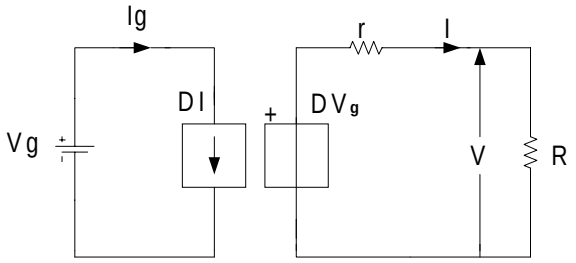

Fig.5. Equivalent DC model for the converter operating in buck-CCM.

The converter DC model, including conduction losses, is shown in Fig. 5, for buck-CCM. The load current is given by:

$$I = \frac{DVg - V}{r} \tag{2}$$

where *D* is the switch duty ratio, $r = 2R_{on}+R_L$, R_{on} is the switch on-resistance, R_L is the inductor series resistance, V_g is the input voltage, and *V* is the output voltage.

Given that an approximate value of *r* can be found from component data, and that the values of V_g, *V*, and *D* are available in the closed-loop controller, Eq. (2) can be used to estimate the load current *I*. By equating this value with the load current at the boundary between CCM and DCM, we obtain a condition for switching between conduction modes.

The same analysis can be applied to the other modes, and the mode-switching conditions are summarized in Table I.

TABLE I
CONDITONS FOR MODE SWITCHING

Buck CCM→DCM	Buck DCM→CCM
$\frac{DV_g - V_O}{2R_{ON} + R_L} < \frac{D(V_g - V_O)}{2Lf_{CCM}}$	$D(V_g + V_D) > (V_D + V_O)$
Boost CCM→DCM	**Boost DCM→CCM**
$\frac{V_g D}{2 f_{CCM} L} > \frac{V_g - D'V_O}{2R_{ON} + R_L}$	$V_g D > V_O - V_g$

A test result illustrating CCM/DCM switching after a load transient is shown in Fig.6. Initially, the converter is in buck-CCM, with the load current equal to 1A. After the load current drops to 0.1A, a transient in the output voltage and the inductor current is observed. In this case, a slow PI regulator was used, so that the load transient resulted in a relatively large overshoot. After a time delay, during which the current estimator detects the change in load based on the observed change in the steady-state duty ratio, a mode-switching transient occurs, the switching frequency is

reduced and the converter moves to buck-DCM. An adjustment of the duty cycle is done so that the mode switching does not produce any significant output voltage transients, as shown by the experimental results in Fig.6.

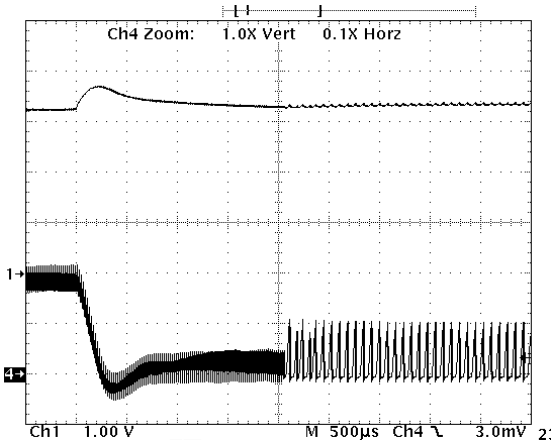

Fig.6. Test of the current estimator: change from CCM to DCM after the load current change from 1.1 A to 0.1 A: the output voltage (top) and the inductor current at 0.5A/div (bottom).

V. Regulator Design

A digital PID regulator can be designed using a variety of methods available in literature [4,5,6]. In this section, attention is given to some of the practical limitations imposed by the system implementation, including: delay due to the sampling and processing, limited PWM and A/D resolution, and limited precision of the regulator parameters.

Although other design methods may give better performance results, we used the Euler method [6] to design the PID regulator. An advantage of this method is that deviations of the regulator parameters due to the limited number of bits have predictable effects on the magnitude and phase responses. Also, the Euler method results in a simple, low-order discrete-time control law.

We start from the continuous-time PID regulator law described in time domain by:

$$x(t) = k\left[e(t) + \frac{1}{T_i}\int e(t)dt + T_d \frac{de(t)}{dt} \right] \tag{3}$$

where $x(t)$ is the output controlled variable, $e(t)$ is the error signal, k is the gain (proportional constant), and T_i, T_d are the integral and the differential constants, respectively.

Laplace transform of Eq.(3) gives the corresponding continuous-time transfer function of the regulator:

$$Gvc(s) = \frac{\omega_i}{s}\left(1 + \frac{s}{Q_1\omega_1{}^2} + \frac{s^2}{\omega_1{}^2} \right)$$

where, (4)

$$f_1 = \frac{1}{2\pi\sqrt{T_i T_d}}, Q_1 = \sqrt{\frac{T_d}{T_i}}, f_i = \frac{K}{2\pi T_i}$$

In the Euler method, the digital control law is obtained by replacing derivatives in Eq.(4) with differences:

$$\begin{aligned} x(n) &= x[n-1] + \\ &+ k\left[(1+\frac{T_S}{T_i}+\frac{T_d}{T_S})e[n] - (1+2\frac{T_d}{T_s})e[n-1] + \frac{T_d}{T_S}e[n-2] \right] \\ &= x[n-1] + ae[n] + be[n-1] + ce[n-2] \end{aligned} \tag{5}$$

The corresponding z-domain regulator transfer function is:

$$G_{VC}(z) = \frac{a + bz^{-1} + cz^{-2}}{1 - z^{-1}} \tag{6}$$

To design the regulator, i.e., to calculate the coefficients *a*, *b*, *c*, it is convenient to construct the complete system loop gain, as in the design of analog controllers. To do so, in addition to the converter's control-to-output response, and the regulator's transfer function, it is necessary to find equivalent gains of the A/D converter and the PWM, and to include the delay due to the sampling and processing.

A. Delay Due to Sampling and Processing

The timing sequence in Fig. 7 shows the origin of the sampling and processing delay in the system. The analog-to-digital conversion is synchronized with the PWM, and it starts at the beginning of a switching period. The sampling frequency equals the switching frequency of the converter. The A/D conversion is completed within 2µs, which leaves enough time to perform all necessary calculations in the controller before the end of the switching period. The output pulse is centered around the middle of a switching period, and is doubly modulated: the rising and the falling edge move by one-half of the total duty-cycle variation. As a result of this timing sequence, we have an effective delay of $1.5T_s$ from the sampling instant to the time the newly updated duty ratio affects the converter operation. The phase lag due to the delay is shown in Fig.8 as a function of frequency.

B. Regulator Design Example

In this Section we discuss the regular design for the buck-CCM example. The buck-CCM control-to-output transfer function is given by Eq.(1), with the following numerical values f_0*=4.1KHz,*, G_{d0}*=4.2* and *Q=4.84.* The system loop gain can be found as:

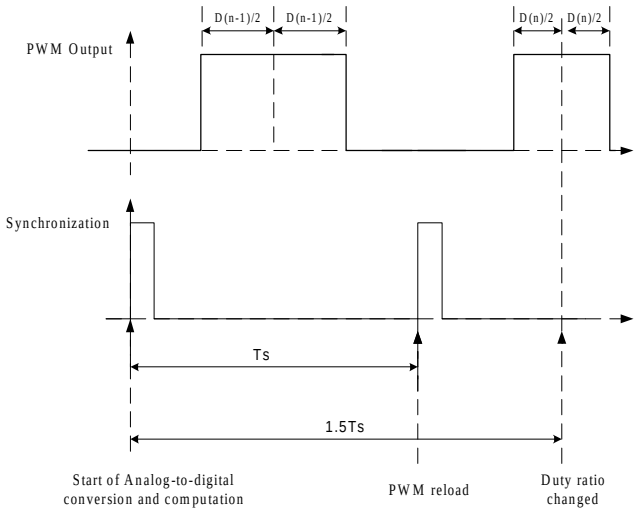

Fig.7. Timing sequence of the PWM and the A/D converter.

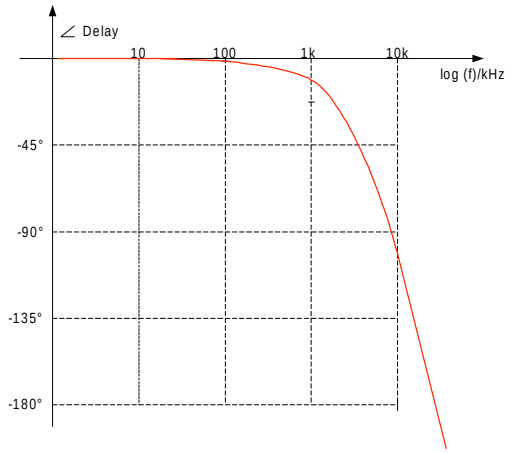

Fig.8. Phase shift caused by the delay of the system.

$$T(s) = K_{A/D} K_{PWM} G_{vd}(s) G_{vc}(e^{sT_s}) e^{-1.5sT_s} \qquad (7)$$

where $K_{A/D}$ is the gain of the A/D converter (equal to 0.208 in our case), K_{PWM} is the gain of the pulse width modulator (equal to one in our case). The usual continuous-time PID design would use $T_i >> T_d$, and the regulator zero would be selected so that the loop is closed at the slope of –20dB/dec with a cross-over frequency greater than the pole corner frequency f_o. Unfortunately, we see from Fig.8 that the system delay introduces significant phase lag at frequencies above f_o, so that adequate phase margin cannot be obtained. Another disadvantage of the approach starting with $T_i >> T_d$ is that very high precision would be needed to represent the coefficients *a, b, c* in the digital regulator. In particular, small changes in the coefficient *a* due to the limited number of bits would result in large changes of the integral constant T_i.

We designed the regulator by attempting to cancel the converter poles with the regulator zeros, in order to approach the ideal loop gain of the form:

$$T(s) = \frac{\omega_a}{s} \qquad (8)$$

In Eq.(4), we selected f_1 to be equal to 4.1 KHz (which is the same as the converter corner frequency f_o), while Q_1 was set to 3.8. This resulted in T_d=143μs and T_i=10.5μs. Finally, the regulator gain was adjusted to k=0.08 so that the resulting cross-over frequency of the system loop gain was set to 1KHz, with the phase margin close to 84 degrees. Using Eq.(5), we obtained the following digital control law:

$$x[n] = x[n-1] + 0.80352e[n] - \\ -1.22304e[n-1] + 0.5712e[n-2] \qquad (9)$$

The magnitude response of the continuous-time equivalent of this digital regulator is shown in Fig.9. Notice that the zeros are indeed located close to the design frequency (f_1=f_o=4.1KHz), but the Q factor of the zeros is lower than the design value Q_1=3.8. This is a result of limitations of the Euler method in moving from continuous-time to discrete-time design.

The magnitude and phase responses of the resulting loop gain are shown in Fig. 10 (dotted lines).

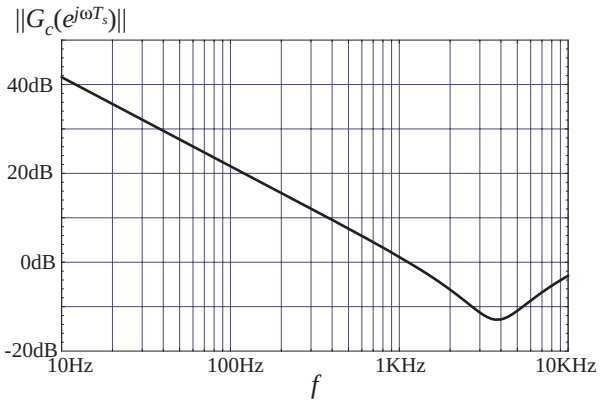

Fig.9. Magnitude response of the digital PID regulator.

C. Effects of Limited Precision of Regulator Parameters

With the limited number of bits it is not possible to implement the designed control law exactly. Deviations of the regulator parameters result in changes of amplitude and phase characteristics of the regulator. To obtain an 8-bit result for the duty ratio, each element at the right hand side of Eq.(9) has to be represented with 10-bit. Higher resolution doesn't improve accuracy, while lower resolution brings additional errors. With 10-bit representation of the PID regulator parameters, the actual control law implemented in the experimental system was:

$$x(n) = x[n-1] + 0.80468e[n] - \\ -1.202306e[n-1] + 0.57812e[n-2] \quad (10)$$

Figure 10 (solid lines) shows the modified magnitude and phase responses of the loop gain. The cross-over frequency increased to 1.2KHz, and the phase margin decreased to 79 degrees. A reason for concern is the peaking in the response after the cross-over frequency, which is due to the fact that the effective Q factor in the PID regulator response did not match the Q factor of the poles in the converter response.

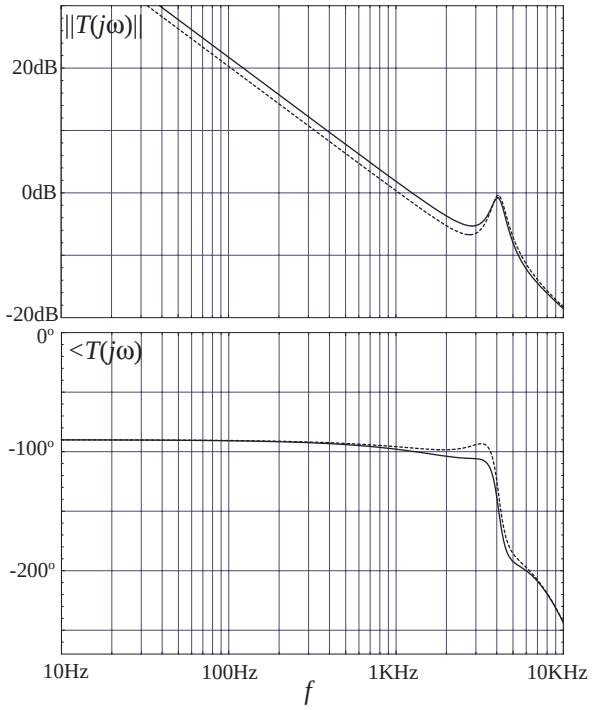

Fig.10. Magnitude and phase responses of the loop-gain: designed response (dashed lines), and actual response (solid lines)

Fig. 11 shows a load transient response of the converter in buck-CCM. The test was performed for the input voltage of 4.2 V and the load transient from 20mA to 1.2A. The output voltage returns within regulation in less than 200μs, with small oscillations that are related to the peaking in the loop-gain response shown in Fig.10.

VI. Conclusion

Digital controller implementation allows potentially much greater flexibility and better utilization of switching power converters. In this paper, we described design and implementation of a digital controller for an experimental low-power converter in a battery-powered system with power

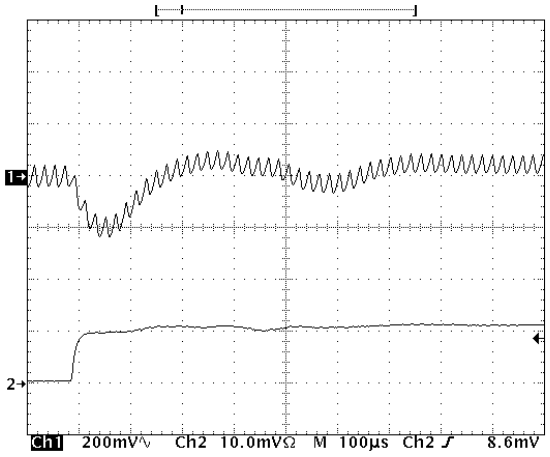

Fig.11. Transient response for a load change from 20mA to 1.2 A: AC component of the output voltage (top) and the load current at 1A/div (bottom).

management. A non-inverting buck-boost converter was used in this application. This converter can operate as a buck, or as a boost, depending on the input voltage. In addition, to maintain high efficiency over a wide range of loads, the converter is operated at high frequency in the continuous conduction mode at heavy load, and at low frequency in the discontinuous conduction mode at light load. A current estimation technique to enable load-dependent CCM/DCM mode switching without current sensing is proposed and tested. Calculations in the simple current estimator are based on the converter DC model, using the values of the switch duty ratio, input and output voltage. A digital PID regulator design example is described, with emphasis on practical limitations imposed by fixed-point arithmetic, limited resolution, and the delay due to sampling and processing. Experimental results are shown to illustrate performance of the digital current estimator and the regulator.

VII. References

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