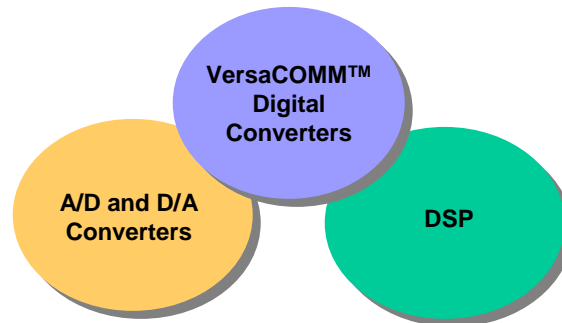




## Overview

Analog Devices Inc. introduces the VersaCOMM™ family of Versatile Communications products providing the link between analog converters and the DSP. Our VersaCOMM™ digital converters perform digital mixing, filtering, tuning, and are reconfigurable in the field for multi-standard signals (2G and 3G cellular air standards) processed as either single carrier or multi-carrier digital receive and transmit architectures. These digital converters are designed for compatibility with Analog Devices family of high speed IF sampling ADCs and DACs. VersaCOMM™ products combine the best product capabilities found in ASICs, FPGAs, and DSPs to provide the systems engineer with competitive field reconfigurable specialized products offering shorter time to market and lower cost compared with alternative product options. Applications include macro, micro, and pico cellular basestation designs for processing of air standards such as IS136, GSM, EDGE, IS95, cdma2000, and UMTS. Other applications include cellular E911 location services, wireless local loop, smart antennas, phased array antennas, and medical imaging and ultrasound applications.

## Providing the link between Analog Converters and the DSP





## VersaCOMM Digital Converters

The VersaCOMM™ Digital Converter family consists of digital Receive Signal Processors (RSP), digital Transmit Signal Processors (TSP), and Quadrature Digital Up Conversion/Modulator (QDUC) products. Many specialized signal processing blocks are built into our digital converters.

### The VersaCOMM Product Family

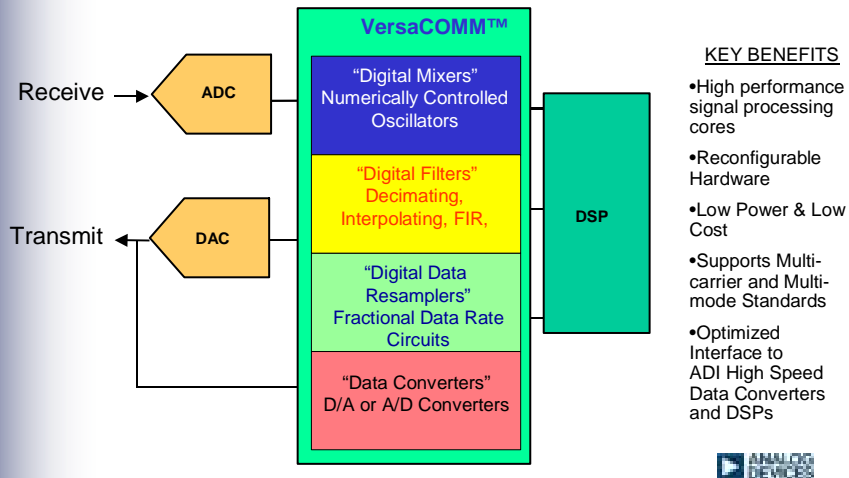
#### Versatile Communications Products

- Receive Signal Processing (RSP)
  - AD6620 – Single/Dual Channel 65 MSPS
  - AD6624 – Single/Dual/Quad Channel 80 MSPS
  - AD6634 – Dual Channel WCDMA 80 MSPS
- Transmit Signal Processing (TSP)
  - AD6622 – Single/Dual/Quad Channel 75 MSPS
  - AD6623 – Single/Dual/Quad Channel 104 MSPS
- Quadrature Digital Upconversion/Modulation (QDUC)
  - AD9853 – 5-65 MHz QPSK/16-QAM Digital Modulator w/10 bit DAC
  - AD9856 – 200 MSPS Quadrature Digital Upconverter w/12-bit DAC
  - AD9857 – 200 MSPS Quadrature Digital Upconverter w/14-bit DAC



Numerically controlled oscillators (NCO) perform “digital mixing” or quadrature modulation to process frequency carriers and generate in-phase (I) and quadrature (Q) digitally sampled words. The NCOs are programmable to provide very precise frequency resolution and can be synchronized for frequency hopping and phase control. The I&Q words are processed in several digital filtering stages found in our RSPs and TSPs such as resampling cascaded integrated comb filters (rCIC2, CIC5) and a RAM coefficient filter (RCF). These filters decimate and interpolate the I&Q data streams removing signal interferers, aliased, and images signal components. The decimation and interpolation rates are user programmable. The digital data resamplers in our RSPs and TSPs permit fractional resampling such that a common clock can be used while generating multiple output data rates. RAM coefficient filters also have programmable coefficients and allow the user to specify the number of filter taps necessary for the particular application. Microport and serial control ports are used to read and write data to and from the part. Our QDUC products have digital quadrature modulators that drive an integrated digital-to-analog converter (DAC) to produce a sample modulated waveform.

## Link Between Data Converters & DSPs



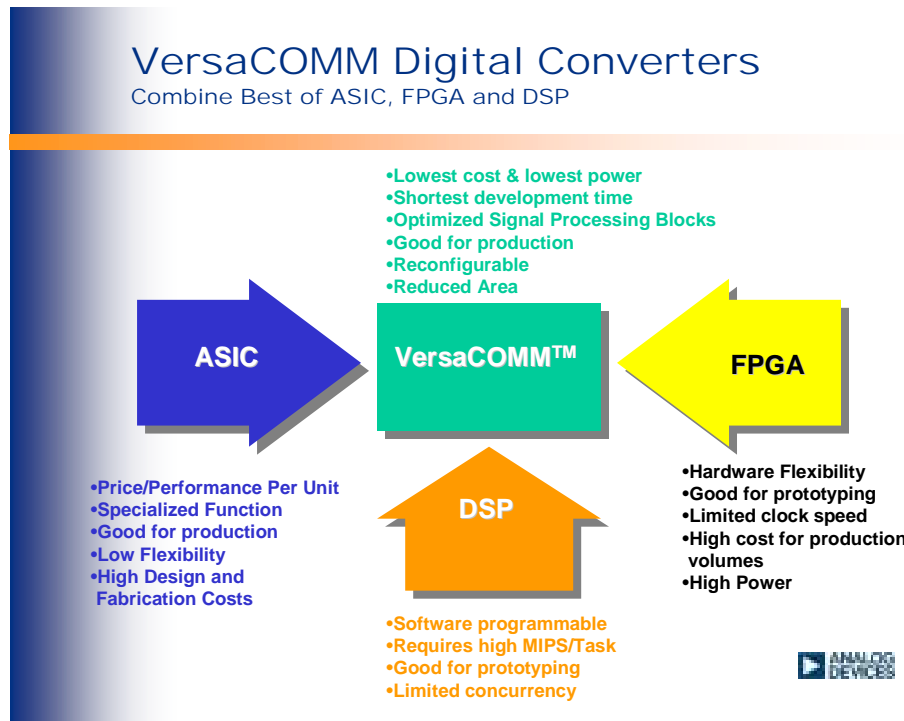
## High Performance Capabilities for Digital Up/Down Conversion

	RSP	TSP	QDUC
High Speed NCO Frequency Translation	✓	✓	✓
Decimating Filters	✓		
AGC Support	✓	✓	
Non-Integer Data Rate Re-Sampling	✓	✓	
Synchronized Operations (Hop, Ramp, Mode)	✓	✓	✓
Programmable Filter Response	✓	✓	✓
JTAG, BIST, PN Generation	✓	✓	
Phase Equalization		✓	
Digital Modulation (GMSK, QPSK, 8PSK)		✓	✓
Interpolating Filters		✓	✓
On Chip DAC			✓

## Digital Converters for Cellular Base Stations

Digital IF sampling and filtering techniques have been used to replace analog base band I&Q signal processing techniques. Digital down and up conversion operations for 2G and 3G cellular base stations can be implemented using a multitude of possibilities. Among these are DSPs, FPGAs, ASICs, and optimized digital converters such as those being offered by ADI within the VersaCOMM™ family. We will discuss and compare the different product design approaches. The table below summarizes the different design approaches and the compares some implementation tradeoffs.

Product	Time to Market	Functionality	Power	Field Config.	Size	Cost	Use
DSPs	Med	Software Programmable	Med/High	High	Large	Med/High	Prototype
FPGAs	Med/Long	Hardware Programmable	High	High	Very Large	High	Prototype
In-House ASICs	Very Long	Specialized	Low/Med	Low	Med	Low	Production
VersaCOMM™	Short	Specialized/Reconfigurable	Low/Med	Med	Med	Low	Prototype & Production



## General Purpose DSPs

Using DSPs to perform digital conversion operations such as IF mixing, filtering, and tuning is possible but is not optimal. Although a DSP can be used to decimate (interpolate) and filter the carrier this consumes resources within the DSP that could otherwise be used for many base band operations such as



adaptive equalizers, RAKE receivers, etc. The high speed IF analog-to-digital converter (ADC) outputs (14 bits at 80 MSPS) much be processed into digital I&Q data streams which requires very high MIPS data processing rates. This function is more optimally performed using our RSP digital converters. The DSP can be programmed to perform the digital I&Q mixing of the IF input, however, this much less efficient compared with hardware I&Q generation using numerically controlled oscillators (NCO) as found in VersaCOMM™ digital converters. The digitized IF stream in the receive (transmit) path needs to be decimated (interpolated) and digitally filtered to remove intermodulation (IM) products, blockers, and meet the filter mask requirements of the signal carrier being processed.

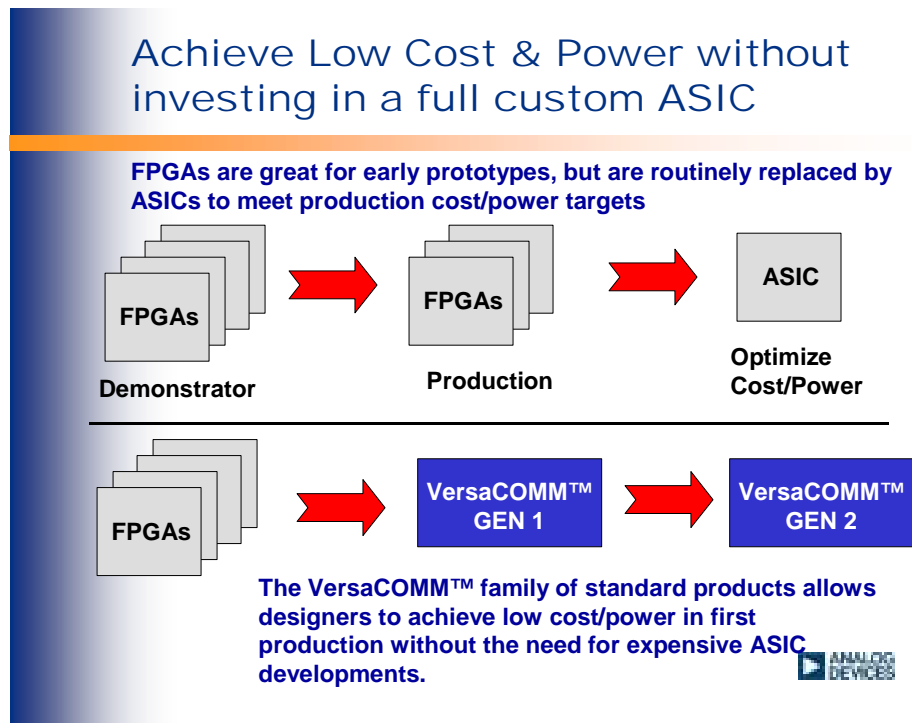
For multi-carrier receive and transmit signal architectures multiple DSPs would be required whereas, a single four channel RSP could be used thereby saving system board area as well. In addition, because the DSP is a general purpose signal processor many embedded features are not used while filtering the digital IF carrier. Consequently, DSPs will also consume more power than digital converters when performing IF digital filtering and tuning operations. VersaCOMM™ digital converters utilize specialized function blocks to perform digital I&Q mixing, filtering, and tuning for over a range of signal input frequencies. Embedded programmable decimation, interpolation, and RAM coefficient filters also allow reconfigurability for processing different air interface standards.

### **Field Programmable Gate Arrays**

FPGAs offer the designer the flexibility of programmable hardware, and are well suited for system prototypes or low volume applications. Often FPGAs are replaced by ASICs to meet production, lower cost, and lower power initiatives. However, FPGA designs require high intellectual property (IP) investment and maintenance to support different air interface standards. In contrast our VersaCOMM RSPs/TSPs can be programmed to process multiple air standards. Very large gate count FPGAs are required to implement a digital down/up converter channel. For example, to implement the NCO along with the appropriate channel filters to process a single GSM channel requires 40K to 80K gates. This gate count increases upward to 100K to 500K gates for 2.5G cellular standards such as IS95 CDMA and up to 1 million gates for 3G WCDMA. Because the digital mixing and filtering modules are implemented in the FPGA using low level logic gates and rudimentary fixed function blocks this also results in overhead circuitry that remains unused. Unit prices for very high density FPGAs can easily run five to ten times the cost of an ASIC or standard product.

Multiple FPGAs may be needed as in the case with DSPs to process multi-carrier IF architectures. In addition to containing specialized signal processing modules, VersaCOMM RSP and TSP products utilize asynchronous clocking to save power. FPGA designs are entirely synchronous and consume more power. Consequently, VersaCOMM™ digital converters allows designers a degree of

field programmability along with the benefit of achieving lower cost and power from prototyping to production development phases.



## ASICs

Application specific ICs (ASICs) can be designed specifically to perform the IF up and down conversion operations described earlier for both DSP and FPGA implementations. ASICs are routinely used to replace FPGA based designs to meet production cost and power targets. Although an ASIC design can be optimized over either DSP or FPGA designs with respect to power consumption, silicon area, and device cost, a great deal of in-house intellectual property and IC design resources must be maintained. ASICs that are designed to process a specific air interface standard or frequency band do not provide the reconfigurability found in VersaCOMM™ digital converters which are capable of processing multiple air interface standards. High IC design costs, wafer processing, and testing costs along with a long time-to-market development schedule are tradeoffs to be considered when developing an ASIC. VersaCOMM digital converters permit designers to achieve low cost/power prototype designs as well as production designs without the need for expensive in-house ASIC developments.

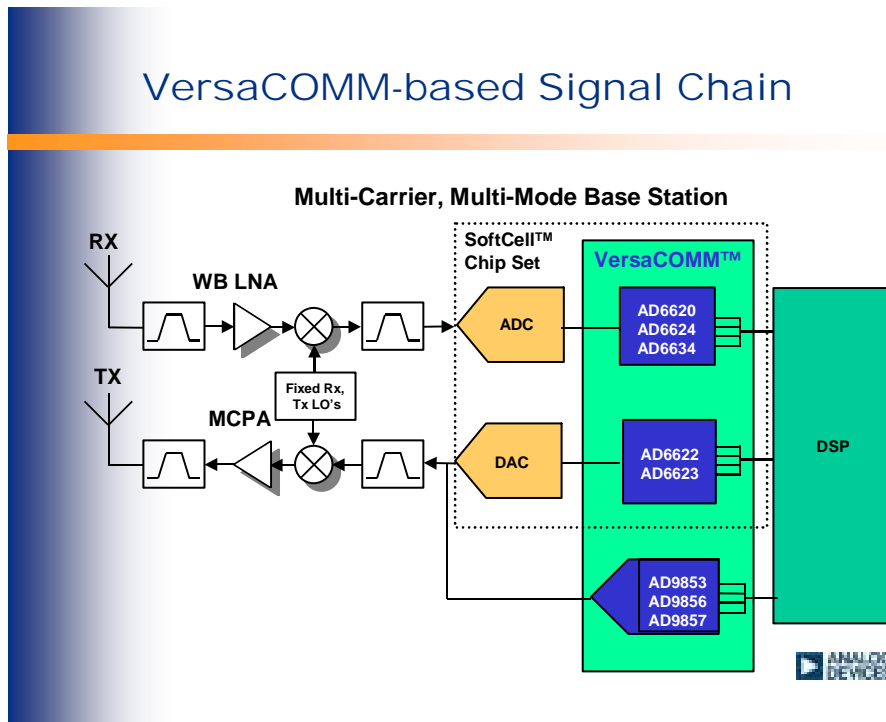
## Using VersaCOMM™ in Software Radio

A receive or transmit software radio consists of high-speed, wide dynamic range analog data converters, and digital converters (receive signal processors, and transmit signal processors). These components, coupled with a high-speed DSP, not only address demanding RF performance requirements, but also provide the



necessary versatility to be reprogrammed to meet the filtering and modulation requirements of any air interface standard.

The receiver front end of a software radio consists of an analog radio frequency (RF) down-converter that converts the desired signal band to a convenient intermediate frequency (IF) for digitization. The down-conversion is followed by a high-performance ADC such as the AD6644, which digitizes the IF signal bandwidth of interest. The ADC output is processed with the AD6624, which is a quad receive signal processor that is responsible for tuning and channel filtering. The output of the RSP consists of a channel-filtered digital base band signal requiring only demodulation that the DSP provides. In the transmit direction, the DSP sends modulated digital data to a transmit signal processor like the AD6622, which modulates the digital carrier. The output of the TSP consists of a channel filtered digital IF signal. Data is then converted to the analog domain using a high performance DAC such as the AD9772A, where it is mixed up to the desired RF frequency.



### RSPs for Wireless Systems

The receive signal processor is a numeric preprocessor for the DSP. The purpose of the RSP is to replace a local oscillator, quadrature mixer, channel select filter and data decimation. In a multi-carrier application, the RSP replaces the analog selectivity and tuning functions with digital equivalents. An RSP sets the receiver apart from traditional receivers because all channel characteristics are now programmable. This includes data rate, channel bandwidth, and air interface mask requirements. In addition to the unlimited selection of channel





characteristics, a digital filter will perform exactly alike across all boards, unlike analog solutions that always have mismatches.

There are several important specifications to consider when selecting an RSP. First, the device must be capable of handling the high data rates required by the interface (ADC). Since the ADC's sample rate determines the bandwidth that can be processed according to the Nyquist theory, the RSP must be capable of handling the same data rate. The Nyquist theory states that the sample rate must be at least twice the bandwidth of signals being processed to recover the information contained therein. In practical systems, the sample rate is frequently run three times faster than the bandwidth of the signals being received to allow for anti-aliasing filter response.

The next specification of interest is the internal and external bus widths. They must be wide enough to preserve the signal integrity. Although the ADC may only be 14 bits wide, oversampling followed by narrow band filtering improves the effective S/N (processing gain) of the ADC by up to 30 dB for some air interface standards. This is the equivalent of 5 more bits. Therefore, internal bus widths must have the equivalent of at least 19 bits to preserve signal integrity.

Since a large portion of any air interface is the channel bandwidth and shape, it is important that the RSP include flexible decimation and filtering configurations that allow for a wide variety of data rates and filter bandwidths. Fixed filter widths and shapes should be avoided since they limit channel bandwidths and often preclude raised root cosine filtering.

Finally, one of the most unique features of an RSP is the ability to select the desired frequency band precisely and rapidly. Most RSPs have a 32-bit NCO which provides a frequency resolution of about 1 in 4 billion. This is usually much more than adequate, and gives great flexibility in frequency selection. In addition to the flexibility, frequency hopping is greatly simplified. Since no PLL is used, changing frequencies is instantaneous. This can be beneficial in applications where hopping must occur within the guardband of a few symbols.

#### TSPs for Wireless Systems

The transmit signal processor is a numeric post-processor for the DSP. The purpose of the TSP is to replace the first local oscillator, quadrature modulator, channel filtering, and data interpolation. Like the RSP, the TSP sets the transmitter apart from traditional designs because all channel characteristics are now programmable. This includes data rate, channel bandwidth and channel shape. Since pulse shaping, channel filtering, and other aspects of the modulation are done digitally, the filters will always perform exactly alike across all boards, unlike analog solutions that always have tolerances.

There are several specifications that are important when selecting a TSP. First, the device must be capable of generating data at the rates required to preserve





the Nyquist bandwidth over the spectrum of interest. As with the ADC's sample rate, the sample rate of the DAC determines how much spectrum can be faithfully generated by the DAC. Therefore, the TSP must be capable of generating data at least twice as fast as the band of interest and preferably three times faster as reasoned earlier for anti-imaging filter response.

Similar to RSPs, the bus widths are also important, yet for different reasons. In the transmit direction, there are two different issues. If the TSP is used in a single-channel mode, then the issue is simply quantization and thermal noise. It is usually not desirable to transmit excess in-band or out-of-band noise, since this wastes valuable transmitter efficiency. In a multi-carrier application, the concern is slightly different. Here, many channels would be digitally summed before reconstruction with a DAC. Therefore, each time the number of channels is doubled, an additional bit should be added so that the dynamic range is not taken from one channel when another is added. As a general rule, the bit precision of the TSP+DAC should not be a major contributor to the noise figure of the transmitter.

Again, channel bandwidth and shape are important and require flexible interpolation and filtering options. Fixed filter widths and shapes should be avoided since they limit channel bandwidths and usually preclude raised root cosine filtering.

Finally the ability to frequency hop is vital. Since a TSP implements frequency control with an NCO and a mixer, frequency hopping can be very fast, allowing the implementation of the most demanding hopping applications as found in the GSM specification.

#### Quadrature Modulators/Upconverters with integrated DAC

TSPs can also have integrated high-speed DACs which enable a direct analog modulated carrier output. These complete digital modulators can contain modulation encoding, up-sampling, and pulse-shaping circuitry to form a complete baseband modulator or they can provide only the upsampling function. These integrated mixed-signal devices serve as an interface between fine-geometry dense digital ASICs and the RF analog output. Quadrature digital upconverters (QDUCs) accept a 14-bit oversampled and pulse-shaped complex data word, upsample the data, modulate a carrier in quadrature, and output a frequency-agile, high-fidelity modulated carrier via a 12-bit or 14-bit on-chip DAC. The QDUC provides programmability in input data rate, output carrier frequency, and internal sample rate. This high-degree of digital flexibility and integration coupled with a high-performance analog output, position QDUCs as superior alternatives to discrete DACs or to a digital ASIC with integrated DAC.

Integrating an encoder stage and FIR filters in front of a QDUC forms the TSP digital modulator solution. This solution provides programmability in input data rate, pulse-shaping function, upsampling rate, modulation encoding format,



analog output frequency, and internal sampling rate. This high-performance mixed-signal solution moves the modulator function into the digital domain where the parameters and configuration are placed under processor control.