Microwaves & RF

COVER FEATURE

Digital Upconverter IC Tames Complex Modulation

An improved 14-b architecture, simplified synchronization, and enhanced power-saving circuitry are a few of the features of this quadrature digital upconverter.

Ken Gentile
System Design Engineer
Analog Devices, Inc., Greensboro, NC 27409; (336) 605-4073, FAX: (336) 605-4187, e-mail: ken.gentile@analog.com, Internet: http://www.analog.com.

DIGITAL technology continues to replace many analog functions in modern receiver architectures. The latest contributor to this trend is the AD9857 quadrature digital upconverter from Analog Devices, Inc. (Norwood, MA), which can replace several front-end components, including a mixer and local oscillator (LO). The 14-b integrated circuit (IC) provides improved dynamic range and sensitivity when compared to its 12-b predecessor, with enhanced power-conservation circuitry.

As the demand for higher data rates continues to grow, system designers are finding it more attractive to design carrier transmission systems instead of baseband transmission systems. There are several reasons for this. First, many data-transmission systems are broadcast over the "air," such as mobile phones, satellite communications, and digital radio and television. The transmission of signals through free space is not practical at low frequencies. The main reason is due to the physical size of the required antenna, which is inversely related to the transmitted frequency. Thus, placing baseband information on a high-frequency carrier makes the use of a smaller antenna possible. Secondly, a modulated carrier is capable of carrying a complex spectrum, which is not possible with a baseband signal. A complex spectrum results when data are encoded into real and imaginary parts and mixed onto the carrier orthogonally. This offers an automatic factor-of-two reduction in the bandwidth required to carry the data (relative to a signal confined to baseband). Thirdly, a modulated carrier can be easily shifted in frequency to offer multiple channels of operation.

At the heart of any data-transmission system resides a bit stream, which is a sequence of ones and zeros that represents the information being transmitted. The bit stream can be converted to a sequence of pulses through a variety of methods, but the end result in any case is the generation of a baseband signal. A baseband signal has a spectrum that starts at 0 Hz (DC) and extends to some positive frequency. The frequency range thus spanned defines the bandwidth of the baseband signal. As mentioned earlier, it is often desirable to shift the baseband signal to a higher frequency to take advantage of the benefits of carrier transmission. The process of shifting a baseband signal to a higher frequency is known as upconversion.

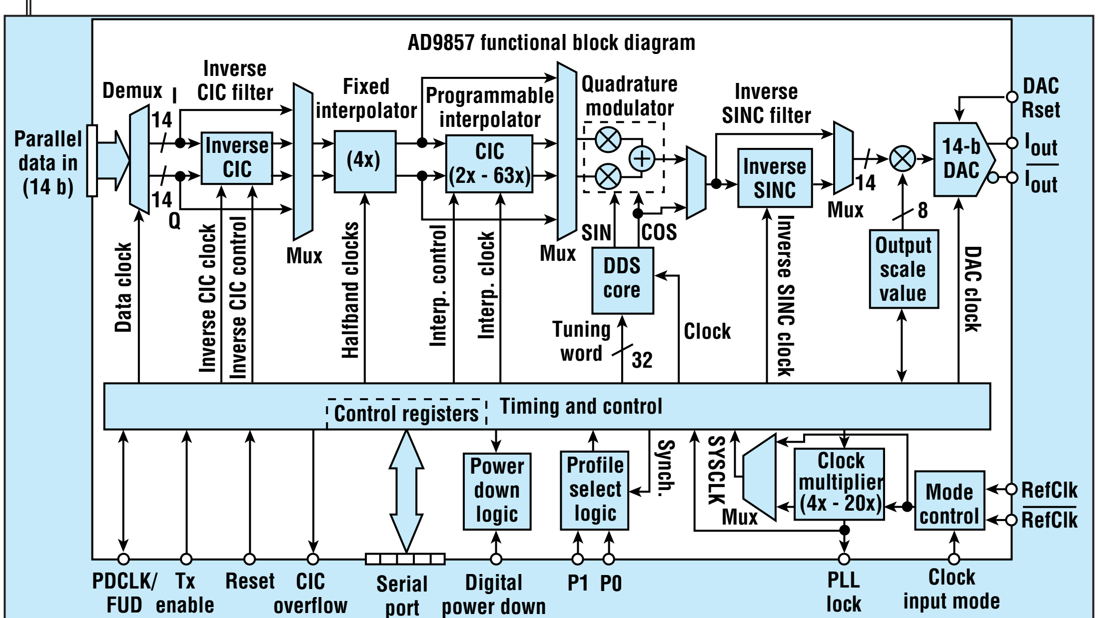
In the past, upconversion has been accomplished through analog mixers, oscillators, and filters. However, upconversion is now possible through digital methods. The first digital upconverter from Analog Devices, the model AD9856 (see *Microwaves & RF*, February 1999, p. 125), provided 12-b resolution and the capability to work at clock rates up to 200 MHz. With the introduction of the AD9857 quadrature digital upconverter, enhanced performance is possible by virtue of the AD9857's 14-b architecture. The additional bits of resolution yield increases in dynamic range and signal-to-noise ratio (SNR). Improvements have also been made to simplify the synchronization process between the device's baseband data port and the user's controlling hardware. Additionally, improvements to the signal-processing chain make the AD9857 a more robust and flexible device than its predecessor. The AD9857 also incorporates a sophisticated power-conservation architecture that automatically shuts down functional blocks that are not configured for use.

Similar to the AD9856, the AD9857 incorporates baseband signal-processing, quadrature mixing, and oscillator functions—all implemented in digital technology. There are a number of significant advantages to implementing these functions digitally. 1. A digital quadrature modulator supports precise matching of the in-phase (I) and quadrature (Q) channels, a challenging task when implemented with analog circuits. 2. The digital circuits used to implement the signal-processing functions do not suffer the effects of thermal drift and aging associated with their analog counterparts. 3. Digital circuitry provides the ability to control and program the device, which means more flexibility for the system designer. 4. The digital nature of the device yields precise control of frequency and nearly instantaneous tuning speed, greatly expanding the range of system capabilities available to the designer. 5. The implementation of digital functional blocks makes it possible to achieve a high degree of system integration. This implies a major reduction in the printed-circuit-board (PCB) area required, which is relative to an equivalent analog design.

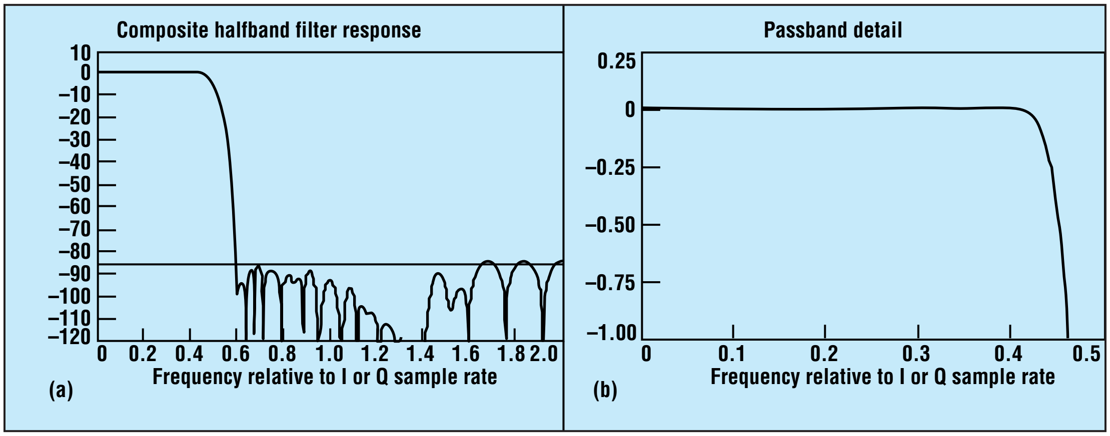
Even though the AD9857 incorporates a largely digital architecture, it nonetheless delivers analog output signals by virtue of its integrated 14-b digital-to-analog converter (DAC). This saves the user the burden of having to provide an external DAC to make the conversion to analog signals. Despite the presence of high-speed digital circuitry, the AD9857 IC achieves analog output signals with excellent noise performance, all on a single silicon (Si) complementary-metal-oxide semiconductor (CMOS) chip.

A look at the block diagram of the AD9857 helps to appreciate the design's blending of digital and analog circuitry (Fig. 1). The AD9857 is designed to operate with a +3.3-VDC supply (with ± 5-percent regulation) over the extended industrial temperature range of –40 to +85°C. As with the AD9856, the AD9857's internal system clock (SysClk) can operate at rates to 200 MHz, which is the maximum sample rate of the onboard DAC (200 MSamples/s). The quadrature digital upconverter is controlled through an SPI-compatible serial input/output (I/O) port that is capable of operating at rates up to 10 MHz. The architecture is designed so that the device may be used in any one of three operating modes: single-tone generator mode, interpolating DAC mode, and quadrature upconverter mode.

The focus here will be on the last mode of operation, which makes use of all of the AD9857's functional blocks. The other two operating modes are simply subsets of the quadrature upconverter mode. Briefly, in the interpolating



1. The AD9857 quadrature digital upconverter employs a 14-b architecture for improved sensitivity and dynamic range compared to its 12-b predecessor, the AD9856.



2. Note that the stopband attenuation is 85 dB (a). In this plot, passband ripple is virtually nonexistent (b).

DAC mode, the quadrature modulator is bypassed. In the single-tone mode, the quadrature modulator and the entire baseband signal-processing section are bypassed.

Many of the features of the AD9857 are directly controlled or programmed by a set of internal control registers, which are accessed by the user through the serial I/O port. The serial I/O port is limited to a maximum clock rate of 10 MHz, which sets an upper limit on the rate at which registers may be updated. The control registers have write and read access, which can be beneficial during the prototype phase of a design because it provides the designer with the ability to verify the contents of the control registers after they have been programmed.

SYNCHRONIZATION

The AD9857 derives its timing through a user-supplied external reference clock (RefClk) from which the internal SysClk signal is derived. The RefClk input will accept either a differential or single-ended clock source at frequencies up to 200 MHz. The SysClk signal is either a directly buffered version of RefClk or it is derived from RefClk through an internal phase-locked-loop (PLL)-based frequency multiplier (programmable in integer values from 4 to 20 through the control registers). The PLL is bypassed or enabled with a control bit in the control registers. This allows the user to employ a low-frequency crystal oscillator for the RefClk signal (e.g., 10 MHz), yet still obtain 200-MSamples/s performance by enabling the PLL at a multiplication factor of 20. Of course, any phase noise inherent in the RefClk signal will be amplified by the PLL multiplication factor. For this reason, very-low-noise clock sources are preferred when the PLL is employed.

The PLL also provides an external-lock indication signal (the PLL lock pin). When the PLL lock signal registers high, it indicates to the user that the PLL has acquired a lock condition. In addition, this signal is routed internally to provide certain internal housekeeping functions within the baseband signal-processing sections of the device. A control bit in one of the control registers will determine whether the PLL lock indicator triggers the internal housekeeping functions.

The heart of the AD9857 is its direct-digital-synthesizer (DDS) core. The DDS consists of a 32-b accumulator that operates at the SysClk rate of f_S. The frequency of the DDS is tunable from DC to $f_S/2$ by means of programming registers, which are accessed through the I/O port. With its 32-b tuning word, the DDS offers a tuning resolution of $f_S/2^{32}$, which is equivalent to 0.047 Hz when operating at the maximum clock rate of 200 MHz.

In the AD9857, the primary role of the DDS is the simultaneous generation of a digital sine and cosine waveform. Each waveform is represented as a series of 14-b numbers that are samples of the tuned frequency taken at the f_S rate. In the quadrature upconverter mode, the digital sine and cosine samples serve as a digital quadrature local oscillator (LO) operating at the carrier frequency, f_C. The carrier is simply the user-specified frequency to which the DDS is tuned.

The quadrature modulator (or digital mixer) multiplies the quadrature carrier samples from the DDS core by the baseband I and Q samples. A fundamental requirement must be established at this point, which is that the sample rate at the input to the digital mixer must be the same as the sample rate of the quadrature carrier signal. For the AD9857, the quadrature carrier signal is sampled at f_S, the frequency of SysClk. This means that the I and Q samples must also arrive at the digital mixer at the f_S sample rate. The quadrature modulator also handles the merging of the multiplication results by either adding or subtracting the two products. By default, the Q results are subtracted from the I results. However, the user can specify a spectral inversion, in which case the products are summed. This feature makes it possible to select either the upper or lower sideband when the device is used as a single-sideband (SSB) transmitter. The presence or absence of the spectral inversion function is handled through the control registers.

The output of the quadrature modulator may be optionally routed to an inverse SINC filter. When selected, this digital FIR filter compensates for the inherent sin(x)/x (SINC) rolloff characteristic introduced by the DAC (an unavoidable artifact of the sampling process) by imposing an x/sin(x) response on the samples before they are routed to the DAC. This compensation is effective over the frequency range of DC to $0.45f_S$. The inverse SINC filter is enabled or disabled through the control registers.

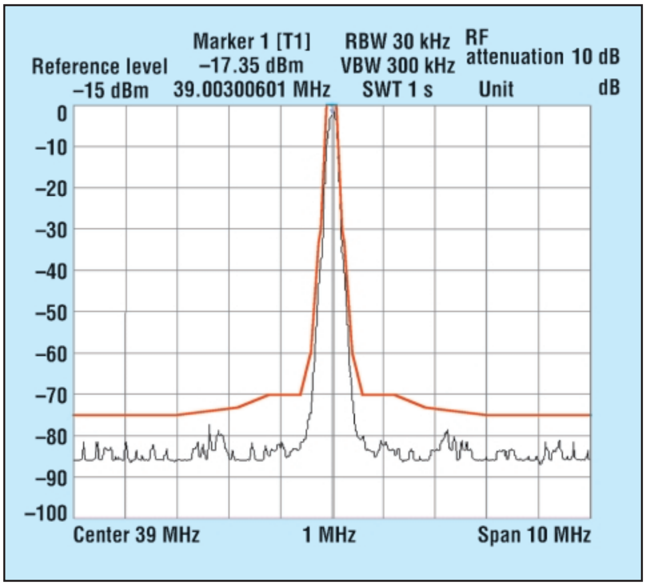
Additionally, the digital samples may be scaled just prior to the DAC input. This is accomplished through a programmable scaler. The scaler multiplies the samples by an 8-b positive number that is programmed by the user through the control registers. The scaler is designed so that the maximum multiplier value (all digital ones) corresponds to a scale factor of 510/256 (1.9921875). The digital scaler makes it possible to generate amplitude-modulated (AM) signals or to ramp the analog output signal level up or down at will.

The AD9857's most enabling attribute is its integrated 14-b DAC. With 14-b resolution, there is sufficient dynamic range to satisfy multicarrier and spread-spectrum applications. Additionally, there is the benefit of a reduced noise floor over devices with fewer bits of resolution. The DAC can handle sample rates up to 200 MSamples/s, while still offering a spurious-free dynamic range (SFDR) of better than –50 dBc with an 80-MHz output signal. Though this specification does not seem to be overly impressive, it should be noted this represents a worst-case scenario. Since the largest spurious components are harmonics of the fundamental output signal (a DAC-induced artifact), it is often possible to select a clock and signal plan that minimizes harmonic artifacts, thereby making it possible to achieve better SFDR performance numbers than those specified.

The DAC is implemented as a current-output DAC with complementary output pins. An externally connected resistor (Rset) establishes the full-scale current generated by the DAC. Typically, Rset is chosen for 10-mA full-scale output current. When the input data to the DAC are at positive full scale, the normal DAC output pin sources 10 mA while the complementary DAC output pin sources 0 mA. The opposite is true when the input data to the DAC are at negative full scale. This complementary output architecture makes it possible to easily interface to a differentially coupled pulse transformer in order to reduce common-mode spurious signals.

BASEBAND PROCESSING

The preceding sections have described the functional blocks of the AD9857 related to generating and conditioning a carrier signal for the purpose of modulating a baseband signal. The following sections describe the baseband signal-processing chain. Baseband information is delivered to the AD9857 over a 14-b parallel data bus. The data presented to the device are assumed to consist of sampled I and Q data pairs that arrive consecutively. That is, a 14-b "I word" which is followed by a 14-b "Q word." The device provides an output clock (PDCLK) to assist the user in synchronizing the transfer of data. The PDCLK signal is a square wave at a frequency determined by the programmed interpolation rate of the digital cascaded-integrator-comb (CIC) filters. Specifically, the output data-clock frequency, f_{DClk}, is equal to $f_S/2M$, where M is the programmed interpolation rate of the CIC filters. Each rising edge of the PDCLK signal causes the AD9857 to read in an I or Q word. The user provides a synchronization signal to the AD9857 (T_x Enable), the rising edge of which signifies that the next rising edge of PDCLK represents an I word. The AD9857 continues to accept alternating I and Q words with each rising edge of PDCLK as long as the user holds T_x Enable high. This input timing architecture makes it very easy to implement data transmission in either burst mode or continuous mode.



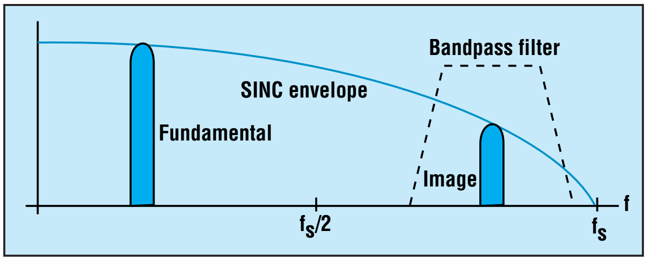
3. This plot shows GMSK modulation for a 39-MHz carrier with a sampling rate of 156 MSamples/s.

The I and Q words are demultiplexed at the front end of the device and fed down parallel paths, which constitutes the baseband signal-processing pathway. The I and Q data are first routed to an optional inverse CIC filter. Next, it is passed through two consecutive halfband finite-impulse-response (FIR) filters that result in the I and Q data being upsampled by a factor of 4. The images normally produced by the upsampling process are effectively eliminated by the frequency-response characteristic of the halfband filters (Fig. 2). The frequency scale is relative to the sample rate of either the I or Q samples (which equates to half the frequency of the PDCLK signal). Note in Fig. 2a that the stopband attenuation is 85 dB. In Fig. 2b, it can be seen that the passband ripple is virtually nonexistent. Close inspection of Fig. 2b indicates that some of the input bandwidth at the high end must be sacrificed as part of the transition region of the filter. Approximately 10 percent of the bandwidth needs to be sacrificed to retain flatness within 1 dB. This implies that the user must upsample the raw baseband data by at least a factor of 2 prior to delivering the data to the AD9857 to avoid the bandwidth limitation imposed by the halfband filters.

Following the halfband filters is an optional CIC filter, which may be bypassed through the control registers. There are two advantages to using a CIC filter. First, the architecture is easy to implement in hardware since there are no multiplication operations required—only additions, negations, and unit delays. Second, a single CIC filter can be made to interpolate data at different rates. This is a unique characteristic of CIC filters and makes it possible to have a programmable interpolation rate. In the AD9857, the CIC filter can be programmed (through the control registers) to interpolate at any integer rate from 2 to 63. Programming the CIC filter with a value of 1 causes it to be completely bypassed.

A CIC filter is not without its shortcomings, however. There are three distinct disadvantages associated with the use of a CIC filter, but each of these shortcomings has been overcome in the AD9857 through careful system design. The first disadvantage imposed by a CIC filter is that the loss through the filter is a function of the programmed interpolation rate (an unavoidable consequence of the architecture). The magnitude of the loss ranges from no loss up to 6-dB loss. To combat this problem, the output stage of the CIC filter incorporates a digital scaler that automatically corrects the rate-related loss. A second disadvantage of a CIC filter is that the passband response is not flat, but follows a form very similar to a SINC response. This problem can be overcome by enabling the optional Inverse CIC filter mentioned earlier. This FIR filter modifies the data before they arrive at the halfband filters to compensate for the frequency response of the CIC filter. This effectively flattens the CIC response over the bandwidth of the passband of the halfband filters. In most applications, the inverse CIC filter is not required because the halfband filters limit the spectrum of the incoming data to a nearly flat region of the CIC response curve. However, some applications cannot tolerate the 0.5 to 0.7 dB of droop imposed by the CIC filters, in which case, the user has the option of enabling the inverse CIC filter to flatten out the offending droop. A third disadvantage of a CIC filter is that the integrator section incorporates feedback. This is not a problem in and of itself, but if the device is not used properly, the CIC filters can be forced into an overflow condition (from which a soft recovery is not possible). As a fail-safe against this potential problem, a control bit is provided in the control registers that can force the CIC filters to be cleared. In addition, the user is provided with a CIC overflow indicator pin, which serves as an alarm, indicating that the CIC filters have entered an overflow condition.

The AD9857 has been designed with both power conservation and noise reduction in mind. A separate clock domain controls each major functional block. When a functional block (e.g., the CIC filters) is disabled or bypassed, the clock to that section is stopped, thereby reducing power consumption and any associated digital switching noise.



4. This diagram shows the technique of using a spectral image of the output signal to eliminate an upconversion stage in a Tx.

CONFIGURATION PROFILES

The AD9857 has another feature that adds to its versatility—its ability to switch between four configuration profiles. A profile is a specific grouping of control registers. Each profile consists of an identical grouping of registers. However, the individual registers within each profile are independently programmable, allowing four different device configurations to be programmed. The registers associated with each profile support programming of a tuning-word value (frequency), a CIC interpolation rate, spectral inversion (or not), an output scale value, and bypassing of the inverse CIC filter (or not). To select a specific profile, the user simply applies the appropriate logic levels to the two profile-select pins (P0 and P1). This provides the user with the ability to rapidly switch between configurations through external hardware control. Furthermore, the profile-select pins are synchronized internally with the rising edge of the PDCLK signal to ensure predictable latency through the device.

The advantages of using profiles become apparent when, for example, a form of modulation known as frequency-shift keying (FSK) is employed. FSK modulation is accomplished by switching between two predefined frequencies in sympathy with the 0's and 1's of an input data stream. FSK can be easily implemented by loading frequency number one in to Profile 0 and frequency number two into Profile 1. Then, with the P1 pin held low, the user simply drives the P0 pin with the FSK data stream. Thus, whenever the FSK data stream presents a logic zero to the P0 pin, then frequency number one is transmitted. Likewise, when a logic one is presented to the P0 pin, then frequency number two is transmitted. Many other scenarios are feasible using this flexible architecture.

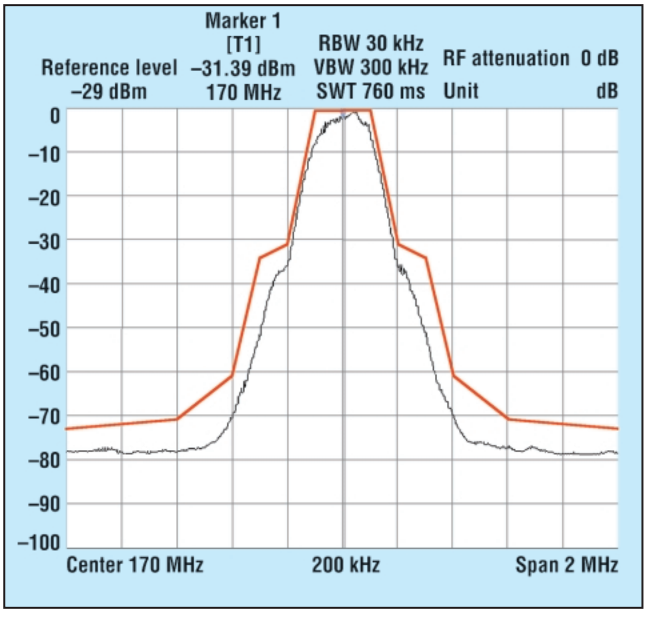
The AD9857 is well-suited for wireless base-station applications. Base stations in Global System for Mobile Communications (GSM), for example, offer a significant design challenge in terms of noise floor and spurious requirements. Especially those systems that employ Gaussian minimum-shift-keying (GMSK) modulation. The stringent noise and spurious requirements can make it difficult for the system designer to find an adequate digital solution. However, with its 14-b integrated DAC and 14-b data pathway, the AD9857 yields sufficient resolution and dynamic range to provide the designer with a digital alternative to base-station transmitter (Tx) design.

Given that the basic GSM data rate is 270.833 kb/s, it is a simple matter to convert the basic GSM data rate to a higher sample rate with the AD9857's baseband signal-processing chain. For example, assume that the user elects to oversample the basic GSM data by a factor of 2 prior to presenting it to the AD9857. This alleviates the bandwidth-sacrificing problem pointed out in the halfband-filter section. The sample rate is now 541.667 kSamples/s. With a CIC interpolation rate of 63 (the maximum value) and the 4 ×upsampling of the two halfband filters, the sample rate becomes 136.5 MSamples/s, well within the 200-MSamples/s limit of the AD9857. Since it is now established that the sample rate is 136.5 MSamples/s, in this case, the GMSK signal can be broadcast on an intermediate-frequency (IF) carrier at any frequency up to 40 percent of this rate. For this example, any carrier frequency up to 54.6 MHz may be used.

To demonstrate the AD9587's capability in generating a GMSK-modulated carrier, consider Fig. 3. It shows a spectral plot of the AD9857 transmitting a GMSK-modulated signal on a 39-MHz carrier (156 MSamples/s). The basic GSM data have been oversampled by a factor of 4 and the CIC interpolation rate set to 36. Note that the AD9857 meets the GSM spectral mask with margin to spare.

In some systems, multiple upconversions are required to shift the IF up to the final broadcast frequency, which can be in the 900- or 1800-MHz range depending on the GSM system employed. Thus, a 39-MHz IF signal may not be sufficiently high enough to eliminate an upconversion stage. However, the exceptional performance of the AD9857 makes the use of an image of the output signal possible instead of the fundamental. Figure 4 demonstrates the technique of using a spectral image.

Figure 5 shows a spectral plot of the AD9857 transmitting on a 170-MHz carrier (195 MSamples/s), which is the first image of the 25-MHz fundamental carrier. Similar to the setup of Fig. 3, the basic GSM data rate has been oversampled by a factor of 4, but the CIC interpolation rate is set to 45 instead of 36. Note that the AD9857 is still able to meet the GSM spectral mask despite the reduced SNR imposed by the SINC rolloff characteristic. In Figs. 3 and 5, the spectral mask specified in the GSM 05.05 document for GSM-900 transmitters is superimposed on the AD9857 output spectrum.[1] This demonstrates the AD9857's performance relative to the GSM specification.



5. This plot shows GMSK modulation for a 170-MHz carrier at a sampling rate of 195 MSamples/s.

In short, the AD9857 is an extremely flexible, low-cost DDS-based solution for a wide range of frequency-synthesis applications. It can be used as a single-tone clock source or LO, as a rate-programmable interpolating DAC, or as a quadrature digital upconverter in a wide variety of applications. Its 14-b DAC and 14-b baseband data path yields sufficient resolution and dynamic range to make it suitable for wireless (and wired) base-station and spread-spectrum applications. A low-cost evaluation board is available for checking the performance of the AD9857, complete with a Windows™-based software package with intuitive graphical user interface (GUI). The evaluation board connects to the parallel port of a personal computer (PC), which serves as the link between the user and the AD9857's serial I/O port. The register programming protocol is handled by the software package, thereby sparing the user the task of learning the details of communicating with the AD9857. P&A: $15.40 (1000 qty.) and $250 (evaluation boards); stock. **Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; (800) 262-5643, (781) 329-4700, FAX: (781) 326-8703, Internet: http://www.analog.com.**

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Reference

1. "Digital Cellular Telecommunications System (Phase 2+); Radio Transmission and Reception", GSM Technical Specification, GSM 05.05, Version 5.2.0, July 1996, European Telecommunications Standards Institute (ETSI).

Acknowledgments

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