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DSPs step forward in 3G stations

Ericsson turns away fromm ASICs, FPGAs

By Patrick Mannion

Manhasset, N.Y. — Ericsson has shifted to a DSP-only, software-defined approach to basestation design in response to the cost, processing and flexibility requirements of third-generation wireless infrastructure. In doing so, the company—the leading basestation manufacturer—has rekindled the debate over the optimum mix of ASICs, FPGAs, DSPs and reconfigurable processors for advanced wireless systems.

Tapping Analog Devices Inc.'s TigerSharc, Ericsson hopes to improve flexibility and lower maintenance costs via software upgrades to accommodate the frequent changes to 3G standards. The trade-offs of DSPs, ASICs and FPGAs have not changed all that much. But the rapid-fire pace of 3G standards evolution convinced Ericsson to reevaluate the architectures' respective positions on the totem poles of cost, power consumption, flexibility and processing abilities.

The flexibility issue came to a head last year with the introduction of the latest enhancement to wideband CDMA: Release 5, or high-speed downlink packet access (HSDPA). The introduction caught many ASIC-centric basestation manufacturers off guard. With Release 6 on the way and interoperability fears rampant as systems roll out, many predict designers will face reengineering and tweaking that can only be economically tackled through software.

But Ericsson is banking on other advantages too, according Kevin Leary, product line director for wireless infrastructure at Analog Devices (Norwood, Mass.), the maker of the designed-in DSP, the TigerSharc TS-201. These include simplified board design, enhanced scalability to enable design reuse, lower R&D resources, faster time-to-market and lower inventory costs through the use of a single processor.

Ericsson confirmed the deal with ADI but would not discuss it at press time, pending the release of earnings.

DSP-only basestations are not new, but to date they have been relegated to niche or low-volume markets such as TD-CDMA in China, where Siemens distributes basestations based on Texas Instruments Inc. DSPs. Low-volume W-CDMA basestation manufacturers also use DSP-only designs; the Fujitsu-Alcatel venture Evolium, for example, uses a design that, like Ericsson's, is based on ADI's TS-201.

'Second look'

But powerhouse Ericsson's decision to go with the TigerSharc "is going to make a lot of companies give DSPs a second look," said analyst Will Strauss, president of Forward Concepts (Tempe, Ariz.).

The design-in is a coup for ADI, which has been struggling to gain a foothold in DSPs for basestations. Forward Concepts estimates that of the $280 million in DSPs delivered to the wireless-infrastructure market in 2003, ADI shipped 7.1 percent, coming in a distant fourth behind Agere (33.9 percent), Motorola (28.6 percent) and Texas Instruments (26.8 percent).

Ericsson dominates the wireless-infrastructure market, with $9.426 billion in annual revenue in an estimated $36 billion market, according to May 2003 data from U.S. Bancorp Piper Jaffray Inc. Ericsson was followed by Nokia, at $5.9 billion, and then Lucent, Motorola, Nortel and others.

The design-in also changes the competitive dynamics of the DSP market, since it lets ADI, armed with the wireless-infrastructure market's highest-volume customer, go gunning for TI. "This is hitting TI's home turf [3G]," Strauss said.

And since Ericsson will no longer employ an ASIC or FPGA for the rake (W-CDMA receiver processing), its decision could cut into the market shares of such ASIC and FPGA suppliers as TI, Xilinx and Altera, Strauss said. Ericsson has been a major Xilinx customer, he noted.

At the heart of the decision to opt for a DSP was Ericsson's confidence in the processor's ability to handle the intensive processing that CDMA and W-CDMA systems use to gain multiuser and spectral efficiency. To date, the options to perform this intensive processing have been either a DSP alone or a DSP plus an FPGA or ASIC. Reconfigurable processors are a third option, but "what invariably gets them is the software," said David Squires, director of Xilinx Inc.'s DSP Center of Excellence, referring to the relative immaturity of development tools for that processor category.

ASICs remain the most efficient option for the intensive chip-rate processing, observers say. But they are also the least flexible and most expensive solution, and their cost is becoming increasingly prohibitive, said Tom Starnes, an analyst with Gartner Dataquest.

Strauss estimates that ASICs average $10 million to develop.

FPGAs still offer more flexibility and faster time-to-market, "but you get a lot of overhead, in terms of significantly higher cost per chip and energy consumption," said Jeff Bier, general manager of Berkeley Design Technology Inc. (Berkeley, Calif.).

Still, that overhead continues to diminish, said Xilinx's Squires.

Programmable DSPs provide flexibility. But as processing requirements increase, the power and performance capabilities of traditional DSPs have been taxed.

From one point of view, "the first stage is always to get product out and get a foothold, so the initial model of a DSP plus FPGA makes sense," said Sandeep Kumar, TI's strategic-marketing manager for wireless infrastructure. "But as devices move forward and functions become more clearly defined, that's when you see the move toward DSP plus ASIC or [DSP plus an] ASSP accelerator."

Changing standards force re-evaluation of basestation architectures
Flexibility of DSP-only approach attracts Ericsson

Basestation architecture	Development cost	Cost per channel	Performance and efficiency	Programmability and flexibility	Power	Space	Time to market
DSP	Lowest	Highest	Lowest—but rising through special instructions and other enhancements	Highest	Highest	Lowest	Fast
DSP + FPGA	Medium	Medium	Medium and rising	Medium	Medium	Highest	Medium
DSP + ASIC	Highest	Lowest	Highest	Lowest	Lowest	Medium	Slow

Source: EE Times

To combat that, Starnes said, both DSPs and RISCs "are adding a lot of very clever things to stay ahead, including special instructions and accelerators and multiple processors that go way beyond the performance improvements that can be gotten from a process-node advancement."

While BDTI's Bier isn't convinced of the cost argument against ASICs, Xilinx's Squires said the debate goes beyond cost.

ASIC teams have been decimated over the past three years, crippling their ability to design, Squires argued. "Also, OEMs have been forced to be brutally honest with themselves, and they've found that ASICs don't really pay for the kinds of volumes you're dealing with on the infrastructure side."

Also working against ASICs is their inherent inflexibility, which has come to light with the evolution of such 3G standards as HSDPA, for which initial designs were found wanting. Along with high costs and changing standards, ASICs as well as FPGAs have had to face evolving DSP architectures.

When ADI announced its revamped TigerSharc in 2003, it broke with the pack by adding up to 24 Mbits of IBM low-leakage embedded DRAM. In addition, ADI streamlined the data path and enhanced its I/O structure. That memory-to-processing-unit shuttling of data had been a major bottleneck in DSP architectures.

Most important in the context of W-CDMA, however, was the addition of CDMA-specific instructions to accelerate the chip-rate processing to a degree that ADI's Leary said obviates the need for any coprocessor or ASICs on the basestation.

"Because of the bit-oriented nature of the chip-rate processing in CDMA, you can get really big efficiency gains by specializing the processor to the data types, and that's what ADI has done," said BDTI's Bier.

Leary also cited the TigerSharc's scalability and homogenous programming architecture, with a "sea" of processors.

But Xilinx's Squires argued that a homogenous-processor approach opens a design to latency if code is changed, a problem that can ripple back to affect verification. Squires suggests a combination of FPGA and DSP so that functions can be separated between the blocks to reduce interaction and time dependencies.

Stumping for ASICs, TI's Kumar argued that the company's ASSPs and ASICs have a large degree of flexibility built in to adapt to standards, including HSDPA and Release 6.

But ADI's Leary countered that "ASSPs do have constraints; you're constrained in how many fingers of rake filtering an ASSP can do, per user, on an aggregate basis."

System interoperability questions loom large, said Leary. "CDMA2000 didn't face this issue, as Qualcomm controlled the deployment very well, but that's not the case with W-CDMA," he said. Instead, operators and equipment vendors have to figure out the interoperability issues as they go along, "so there'll be a significant stage of reengineering to ensure industry levels of interoperability." That solidifies the case for software basestations, in Leary's view.

But nobody is saying the days of mixed-processor solutions are over.

"This is a little victory in a little skirmish for ADI," Bier said, "but there's no reason to assume DSPs have won the war. When volumes increase and standards stabilize, the trend will be toward more tailored solutions. It's a continuum."