Profound changes in the design of high speed mixed-signal ICs are needed to cope with their increasing complexity and performance demands.

Traditional functional partitions and expertise domains—such as circuit design, layout design, and verification—are rapidly blurring. The ability of developers to innovate across different technology spaces is key. The implications of these technology trends go beyond product development—they deeply impact business strategies.

High speed mixed-signal systems bridge digital signal processing, RF (including microwave/millimeter wave), and wired communications, creating a formidable combination of technology and business-related challenges. These challenges are being driven by the rapid increase in demand for pervasive access to high throughput data transmissions.

5G communications promise even faster and more ubiquitous connectivity, supporting multiple communication standards while reducing the size and operating costs of infrastructure. The demands for higher integration, lower power consumption, and cost reduction are all expected to accelerate to a level that simply doesn’t seem to be supported by what might, in fact, be a decelerating Moore’s law.

While transistor density increases and cost reductions will continue for at least five more years or so, speed improvements are substantially diminishing in finer lithography nodes. Digital circuits will still see declines in switching energy and power as they scale to 16 nm and beyond, but we should not expect gates to run much faster than in previous nodes. After all, clock speeds in digital processors plateaued a decade or so ago with greater processing speed realized through parallelism.

Despite continued declines in the cost of digital functions, companies still face financial barriers in the form of skyrocketing upfront costs and design complexity. These factors are rapidly increasing, which shapes engineering and business choices.

As we press on to build complex systems in scaled lithography, we must ask whether the return makes it worthwhile. More than ever, there are no easy and broad answers.

As has been the case at other turning points of our industry, the ingenuity of engineers who see beyond ingrained assumptions will be key. The path to substantial power reduction, and thus smaller size and greater integration, can be summarized in three steps:

The first step lies in architectural innovation in mixed-signal and data converter systems including different forms of analog parallelism, higher order continuous time loops, and emerging time-domain converters. The second step is in far greater use of digitally assisted analog techniques, including self-trimming and calibration, dynamic element matching, and dithering. Finally, engineers need to smartly partition functional blocks among different dies while integrating appropriate technologies in appropriate CMOS nodes as well as compound semiconductor processes such as SiGe, GaAs, and GaN to create high performance modules and packages.

In this way, functional boundaries between traditional components such as power management, RF, and mixed-signal blocks will blur, opening the door to greater co-design. Corporate executives, please take note: we won’t get out of this conundrum with marketing or incremental innovation. We need technology leadership to take the risks needed to empower the designers of next-generation mixed-signal systems if we are to continue to deliver financial returns.