Part one of this article appeared in *Linear Technology X:1* (February 2000) and is also available on the Linear Technology web site at www.lineartech.com/ezone/dsl.html. It discusses the different DSL standards, characteristics of the DSL signals, the design of differential drivers for DSL and the requirements for amplifiers used in this application.

### Design Calculations, Volts, Amps and Power Dissipation

It is very important to consider the power requirements of the line driver in DSL applications. Although a nominal power level of 100mW RMS or less into a 100Ω load does not seem to be a lot of power, the driver must handle large peak signals and therefore requires a larger than nominal power supply voltage. This increases both the power dissipation in the driver package and the peak current capability needed from the power supply.

This issue becomes most critical in central office designs, where many DSL ports are included on a single card powered from one supply. Additionally, the heat generated by the drivers must be handled properly to ensure reliable operation.

This section will provide the calculations necessary to determine the voltages, currents and power dissipation for an ADSL driver of either standard. It can be quite useful to place these equations in a spreadsheet to allow quick observation of the effect of different design variables on the overall system. Assuming that a wide band, low distortion driver has been selected (the LT1795 and LT1886 are excellent choices), the three most important system issues to consider are the total supply voltage, the peak output current and the driver power dissipation required.

For these calculations, the RMS voltages required are treated as DC levels for the purpose of estimating the power dissipation. In an actual DSL design this approach overestimates the typical power dissipation with a DMT signal by 10% to 20% because a data transmission is not always at the maximum output power level. The DSP intelligence built into the system automatically adjusts the transmitted power level and frequency spectrum for each connection made. With shorter phone-line loops, the transmitted power is reduced; with longer loops, not all of the channels are used and the number of data bits per channel is reduced. The maximum transmitted power is provided when the connection loop length is in the range of 4000 feet to 10,000 feet and there happens to be a significant level of noise interference and/or low line impedance conditions. Designing to handle the conservative estimate provides a margin of safety for reliable operation.

### The Input Variables

Before a design can begin, the following information must be known: which DSL standard is to be used, Full Rate or G.Lite, whether upstream (CPE) or downstream (CO). These same equations apply for any DSL standard (HDSL and HDSL2 for example) with some changes to the input parameters (see Table 1).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Description</th>
<th>Typical Values for ADSL</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{\text{LINE}}$ (dBm)</td>
<td>Line Power</td>
<td>RMS power to be put on the line</td>
<td>20dBm (Full Rate, CO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>16.3dBm (G.Lite, CO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>13dBm (Full Rate and G.Lite, CPE)</td>
</tr>
<tr>
<td>PAR</td>
<td>Crest Factor</td>
<td>Peak-to-average ratio for the DMT signal</td>
<td>5.3</td>
</tr>
<tr>
<td>$Z_{\text{LINE}}$</td>
<td>Line Impedance</td>
<td>Characteristic impedance of the line</td>
<td>100Ω</td>
</tr>
<tr>
<td>$n$</td>
<td>Turns Ratio</td>
<td>The turns ratio of the line coupling transformer</td>
<td>1:1 or higher</td>
</tr>
<tr>
<td>$P_{\text{LOSS}}$ (dBm)</td>
<td>Insertion loss</td>
<td>The power loss of the transformer being used</td>
<td>0.2dBm to 2dBm</td>
</tr>
<tr>
<td>$V_{HR}$</td>
<td>Headroom Voltage</td>
<td>A function of the output saturation voltages (positive and negative swing)</td>
<td>2V to 5V</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent Current</td>
<td>Total quiescent (no input signal) supply current of the driver that is not</td>
<td>10mA to 30mA</td>
</tr>
<tr>
<td>$e_{IN}$</td>
<td>Input Voltage</td>
<td>Maximum peak-to-peak differential input voltage from the AFE (analog front</td>
<td>1.5V to 4.5V&lt;sub&gt;p-p&lt;/sub&gt;</td>
</tr>
</tbody>
</table>

### Table 1. Input variables


Basic System Requirements

The following equations determine the essential operating requirements independent of the driver amplifier used in the design:

Line Power in Watts:
\[ P_{\text{LINE}}(\text{W}) = 10 \cdot 10^{-10} \cdot 1\text{mW} \]
\[ \text{example: } 20\text{dBm} = 100\text{mW}. \]

RMS Line voltage:
\[ e_{\text{LINE}}(\text{RMS}) = P_{\text{LINE}}(\text{W}) \cdot Z_{\text{LINE}} \]

Power to the primary of the transformer:
\[ P_{\text{PRI}}(\text{dBm}) = P_{\text{LINE}}(\text{dBm}) + P_{\text{LOSS}}(\text{dBm}) \]
\[ P_{\text{PRI}}(\text{W}) = 10 \cdot 10^{-10} \cdot 1\text{mW} \]

Impedance of primary of the transformer:
\[ Z_{\text{PRI}} = Z_{\text{LINE}} \]

Transformer termination resistors:
\[ R_{\text{BT1}}, R_{\text{BT2}} = \frac{Z_{\text{PRI}}}{2} \]

Primary RMS voltage:
\[ e_{\text{PRI}}(\text{RMS}) = \sqrt[2]{P_{\text{PRI}}(\text{W})} \cdot Z_{\text{PRI}} \]

Driver amplifier RMS output voltage:
\[ e_{\text{AMPLIFIER}}(\text{RMS}) = \frac{\left(Z_{\text{PRI}} + (2 \cdot R_{\text{BT}})\right)}{Z_{\text{PRI}}} \cdot e_{\text{PRI}(\text{RMS})} \]

This is the RMS voltage between the two amplifier outputs. If the \( R_{\text{BT}} \) resistors are properly sized this voltage is twice the RMS voltage of the transformer primary.

Peak driver amplifier output current:
\[ I_{\text{PEAK}} = \frac{e_{\text{PRI}(\text{RMS})} \cdot \text{PAR}}{Z_{\text{PRI}}} \]
\[ = \frac{l_{\text{PRI}(\text{RMS})} \cdot \text{PAR}}{Z_{\text{PRI}}} \]

The peak current handling capability is key to selecting the driver amplifiers.

Power supplied by the driver amplifiers:
\[ P_{\text{OUT}} = e_{\text{AMPLIFIER}}(\text{RMS}) \cdot I_{\text{PRI}(\text{RMS})} \]

Overall line driver voltage gain:
\[ A_{\text{V(TOTAL)}} = \frac{e_{\text{LINE}}(\text{RMS}) \cdot 2 \cdot \text{PAR}}{e_{\text{IN}}} \]

Differential amplifier voltage gain:
\[ A_{\text{V(DIFF)(AMPLIFIERS)}} = \frac{e_{\text{AMPLIFIERS}}(\text{RMS}) \cdot 2 \cdot \text{PAR}}{e_{\text{IN}}} \]

The turns ratio of the transformer used is critical to the overall design. Figure 1 illustrates the minimum total supply voltage across the driver and the peak driver output current required as a function of the turns ratio. These are the absolute minimum requirements based on an ideal amplifier that has 0V headroom and is therefore able to swing fully to either supply voltage rail, and an ideal transformer, with zero insertion power loss. A practical implementation will require a larger supply voltage, as determined from the next section. Trying to design a system with less supply voltage or current capability using conventional transformer termination resistors will result in clipping and transmission data errors.

Figure 1 also compares the different ADSL standards with the central office, downstream, Full Rate ADSL, which requires the most current and voltage. The reduced line power requirements for the downstream G.Lite and the upstream Full Rate and G.Lite modems produce designs with lower voltage and current requirements.

**Important Driver Characteristics: Headroom Voltage and Quiescent Current**

To determine the required supply voltage, power consumption and power dissipation of the driver, the headroom voltage and required quiescent current of the driver amplifier must be considered.

Minimum total supply voltage for the amplifiers:
\[ V_{\text{SUPPLY(MIN)}} = E_{\text{AMPLIFIER}}(\text{RMS}) \cdot \text{PAR} + V_{\text{HR}} \]

The actual supply voltage for the driver amplifier must be set above the minimum peak-to-peak amplifier output swing to provide for the headroom voltage to prevent peak signal clipping. Using a supply voltage greater than this minimum value will increase the power dissipation in the driver amplifiers.
Figure 3. Much of an amplifier’s quiescent current is transferred to the load current

The headroom voltage of an amplifier is determined from either the guaranteed specification for output voltage swing or from characteristic curves showing output saturation voltage vs output current or vs temperature with different load currents. The headroom voltage is the difference between the supply voltage rail and the maximum output voltage swing, both positive and negative, for a given load current. Figure 2 shows a simple model for determining an amplifier’s output saturation voltages and an example of a useful data sheet curve.

During large signal transients, the transistors in the output stage of the amplifier will fully turn on to pull the output as close as possible to the supply voltage rails. The limitation on how close the signal can swing is determined by a fixed voltage drop across the transistor being driven with a resistance in series. This resistance increases the voltage swing limitation in proportion to the amount of load current the transistor must source or sink. The combined total of the fixed voltage drop and the voltage across the resistor is called the output saturation voltage. The values to use to model this characteristic can be determined from a data sheet curve.

The total power consumption of each line driver: $P_{IN} = V_{SUPPLY} \times (I_Q + I_{PRI(RMS)})$ (14)

With $V_{SUPPLY}$ set large enough to prevent signal clipping the total power consumption from the supplies can be determined with Equation 14:

Power consumption of the complete line driver:

$$P_{DISS} = (V_{EXTRA} + V_{HR} + V_{AMPLIFIER(RMS)} \times PAR) \times (I_Q + I_{PRI(RMS)})$$

This equation introduces two new terms, $V_{EXTRA}$ and $I_Q$. $V_{EXTRA}$ is the total additional power supply voltage above $V_{SUPPLY(MIN)}$ that is actually used to power the driver amplifiers. For example, if the minimum total supply voltage for a design is determined to be 20V (or ±10V) but the actual supplies available are ±12V, then the $V_{EXTRA}$ term will be 24V – 20V or 4V.

The total power consumption of each line driver is very important when sizing the power supply for both voltage and current capability to be used in the system. This becomes most significant when multiple DSL ports are to be powered from a predetermined power supply. The power supply could become the limiting factor to the number of ports allowable.

The quiescent current, $I_Q$, is basically the operating supply current of the driver amplifiers. This is the curr-
The power dissipated in the driver package is important to consider when addressing heat management issues. To minimize power dissipation, the driver should be powered from a power supply with voltages set to the minimum required. The design of power supply voltages is not found on typical data sheets. For each of the ADSL standards, a certain minimum power dissipation is required. Three factors that add to this power dissipation are the amplifier headroom voltage, the amplifier quiescent operating current and the power loss of the line-coupling transformer. Attention to these three factors when selecting an amplifier and transformer can optimize the overall power dissipation. 

### Optimizing Power Dissipation, Adjustable Quiescent Current and Shutdown

Several high speed power amplifiers from Linear Technology provide the ability to externally set the operating quiescent current. For the design of any of the DSL standards, this allows for fine tuning the amplifier’s performance. For fine tuning the amplifier’s performance, the power dissipated in a line driver, $P_{\text{AMPLIFIERS}}$, is given by

$$P_{\text{AMPLIFIERS}} = P_{\text{IN}} - P_{\text{OUT}} = e_{\text{AMPLIFIERS(RMS)}} \cdot (\text{PAR} \cdot I_Q + I_{\text{PRI(RMS)}}) \cdot (\text{PAR} - 1)) + (V_{HR} + V_{EXTRA}) \cdot (I_Q + I_{\text{PRI(RMS)}})$$

This shows the effect on total package dissipation for each factor taken individually with the other two factors set to zero. The term $I_Q$ is the transformer turns ratio.

The factors in Table 2 provide a rough indication of the additional power dissipation from these three system variables. The combined effect on power dissipation from $I_Q$, $V_{HR}$ and $P_{\text{LOSS}}$ must still be determined from Equation 15.

### Table 2. Additional power dissipation factors

<table>
<thead>
<tr>
<th>Standard</th>
<th>ADSL Full Rate Downstream</th>
<th>G.Lite Downstream</th>
<th>Full Rate and G.Lite Upstream</th>
<th>Additional Power Dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Power Dissipation, $P_{\text{MIN}}$</td>
<td>860mW</td>
<td>367mW</td>
<td>172mW</td>
<td></td>
</tr>
<tr>
<td>Amplifier Quiescent Current, $I_Q$</td>
<td>33.5mW/n</td>
<td>22.14mW/n</td>
<td>15mW/n</td>
<td></td>
</tr>
<tr>
<td>Transformer Insertion Loss, $P_{\text{LOSS}}$ in dBm</td>
<td>2.3%</td>
<td>2.3%</td>
<td>2.3%</td>
<td></td>
</tr>
<tr>
<td>$P_{\text{LOSS}}$ (dBm) - 1</td>
<td>(P_{\text{MIN}} \cdot 1.023 \cdot (P_{\text{LOSS(dBm)}} - 1))</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
operating point for minimum power dissipation and adequate distortion performance. There is a direct trade-off between the two, however. Designing for very low quiescent current significantly reduces the power dissipation, but obtaining the lowest distortion performance requires additional biasing current for the internal amplifier circuitry. Figure 5 illustrates the adjustability of the operating current for the LT1795. An internal current source is programmed via a single external resistor. The current through this source is mirrored and scaled up to become the biasing current for the two amplifiers. Also shown in Figure 5 is the effect of adjusting the operating current on distortion. The spectrum analyzer plots show the intermodulation components from twenty carrier tones (from 200kHz to 500kHz). With too low of an operating current, the signal on the line is far too distorted and interference with other channels is inevitable. However turning up the current drops all of the distortion products into the noise floor. This adjustment should be made during the evaluation of the driver under actual transmission conditions and optimized for the highest data rates obtainable.

The best power and thermal management technique in multiple-port systems or energy efficient stand-alone modem designs is to shut off the driver when the line is inactive. The digital circuitry always knows when there is no data transmission activity and can issue a signal to the driver to shut down operation. Many drivers accept this control signal and completely power down the internal circuitry. The LT1795, for example, can be shut down to consume less than 200µA of current when not required to transmit data. When commanded to power up, the driver requires only a few microseconds to reestablish full performance, an insignificant time when compared to a typical communication training-up interval. When powered down, however, the output stage of the amplifier loses all bias and enters a high impedance state. This essentially opens the connection to the transformer back-termination resistors. As these resistors are often used to sense the received signal from the line, no signal can be developed across them if they are left floating.

Figure 6 illustrates a power saving function, called partial shutdown, that keeps the amplifier slightly biased and thus allows the modem to continue to monitor the line for transmission signals to be received. Here, two resistors are carefully chosen to control the amount of operating quiescent current as well as to retain a small amount of “keep-alive” current when shut down. Resistor scaling can accommodate a direct connection to an I/O pin from the DSP processor with any logic voltage level. Shutting down to a quiescent current level of 2mA keeps the output stage active and terminates the received signal sensing resistors, resulting in a better than 10-to-1 reduction in idle-channel power consumption and dissipation.

**Thermal Management**

Depending on the ADSL standard being applied, the power supplies and the transformer turns ratio used, the driver amplifier package will dissipate somewhere between 500mW and 2W. The average power dissipation...
times the overall thermal resistance from the junction of the driver to the ambient air will determine the rise in operating junction temperature above the maximum ambient temperature. Most power amplifiers have a built in thermal protection mechanism that will disable the output stage when the junction temperature exceeds typically 160°C. Should this temperature ever be reached, the amplifier will protect itself, but data transmission errors will abound and most likely the system to limit the driver junction temperature above the maximum ambient temperature.  As most of the heat is dissipated in the area immediately surrounding the driver amplifier package, there comes a point of diminishing returns where more copper area does not provide much additional benefit. This can be seen in the plot of thermal resistance in Figure 7 where, beyond a total PCB area of 1 in², further reduction in thermal resistance is minimal. One word of caution regarding PCB planes for heat spreading is that the fiberglass material (typically FR-4) is a fairly good thermal insulator. Any component interconnect traces that cut through the plane of copper significantly reduce the effectiveness of the lateral area. Interconnect traces should be made on the inner layers of multilayer boards to minimize the distance between components. The complex interconnect of the logic circuits used in DSL modems usually requires a multilayer PC board that can be put to good use in the line driver area.

Another measure that can be taken is to provide some forced airflow cooling. A linear flow of air across the driver package can significantly reduce the effective thermal resistance from junction to ambient ($\theta_{JA}$) of the heat-spreading system. A reduction of $2^\circ C/W$ to $3^\circ C/W$ for each 100lfpm (linear feet per minute) can
be achieved. This is particularly important in a multiport system housed in an enclosed case.

A Gallery of Design Recommendations

This section will provide examples of driver and receiver circuits for each of the ADSL standards. These circuits provide a good starting point for implementing the line interface functions for a DSL modem. The circuits were designed with all of the considerations mentioned so far, but other system variables, such as available supply voltages or AFE output and input dynamic range, could mandate some modifications. The total voltage gain of each line-driver design, from the differential input voltage to the actual voltage output to the phone line, has been scaled to a value that requires less than 3V P-P from the AFE providing the transmitted signal. The gain of the amplifier stage is adjusted to take into account the signal boost of the transformer used as well as the signal loss through the back-termination resistors.

Common to all of the designs is a good power supply bypassing approach. This is shown in Figure 8. A large- and a small-valued bypass capacitor at the points where the supplies connect to the board provide decoupling of noise and ripple over a wide frequency range. Additional high frequency decoupling at the driver and receiver supply pins is recommended. Another large-valued bypass capacitor connected directly between the supply pins of the driver helps to reduce the 2nd harmonic component of ripple on the supply lines. This component comes from the peak current demands from each supply, which occur twice for each input signal cycle due to the differential amplifier topology (each amplifier sources and sinks the peak current once each signal cycle).

The Differential Receiver

Not all DSL modems will require a receiver circuit. Some analog front end ICs have sophisticated circuitry for a very wide dynamic input range to directly pick the small received signals out of the noise floor after passing through the receive/echo filter. Other designs may use a second transformer to process the differential received signal directly to the filter/AFE. Many designs still prefer to sense the differential signal across the termination resistors and provide gain to the received signal before passing it through the filter to the AFE. This basic differential receiver circuit

**Figure 9. Basic differential receiver (4-wire to 2-wire)**

**Figure 10. Full Rate or G.Lite upstream (CPE) driver**
is shown in Figure 9. Each receiver amplifier is a summing stage that sums the received signal and the attenuated transmitted signal seen at the primary of the transformer with a weighted, opposite-phase transmitted signal. This weighted summing of the transmitted signal ideally cancels the 180° out-of-phase signals, leaving only the received signal at the differential amplifier outputs. This is called local echo cancellation. In a standard line-driver design, the transmit signals at nodes A and B in Figure 9 are twice the magnitude of the signals at nodes C and D. To cancel these signals in the receiver requires resistors $R_A$ and $R_B$ be set to exactly twice the value of resistors $R_C$ and $R_D$.

The gain of the receiver is simply the inverting gain of the received signal path, $\frac{R_{F1}}{R_C}$ and $\frac{R_{F2}}{R_D}$. In the driver design examples to follow, the receiver input resistors connect to the driver at nodes A through D. The recommended component values for the receiver provide for unity gain from the received signal appearing at the line to the differential receiver output. This takes into account the attenuation of the line-coupling transformer. A small feedback capacitor is also shown that reduces the gain at a frequency just above the received signal bandwidth, which varies depending on the application.

**ADSL Full Rate or G.Lite Upstream (CPE) Line Driver**

This driver (Figure 10) is the lowest powered of the ADSL standards, consuming less than 500mW. The lower line power, 13dBm, and resulting lower peak current requirement allows the use of the LT1886, which is a high speed 200mA dual amplifier. The use of a 2:1 transformer turns ratio allows this driver to be powered from a single 12V power supply.

In order to obtain the highest open-loop gain and bandwidth to minimize distortion, the LT1886 is decompensated and is only stable with closed-loop gains of ten or greater. In this design the signal gain of each amplifier is only 6.35. To remain stable with this low value of gain requires the addition of gain-compensation components $R_{C1}$, $C_{C1}$, $R_{C2}$ and $C_{C2}$. These components, which come into play only at frequencies greater than 15MHz, parallel the gain-setting resistances, $R_{C1}$ and $R_{C2}$, to make the feedback factor of each amplifier a value of 0.9, which is the same as having a closed-loop gain of ten; thus, stability is ensured.

The LT1886 is a 700MHz gain bandwidth amplifier. The combination of gain at such high frequencies and not being unity gain stable requires that the gain-setting resistors be returned to a low impedance at all frequencies. For this reason, the two gain setting

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**Figure 11. ADSL G.Lite downstream (CO) line driver**

**Figure 12 ADSL Full Rate downstream (CO) line driver**
resistors are connected to ground rather than using a single resistor connected to the other amplifier’s inverting input. Capacitors C1 and C2 are included to prevent applying gain to the DC offset voltages of the amplifiers. The different values of feedback capacitors for the receiver amplifier account for the frequency spectrum of the downstream information from the CO modem in either the Full Rate (1104kHz) or G.Lite (552kHz) implementation.

**ADSL G.Lite Downstream (CO) Line Driver**

This moderate power (16.4dBm) driver requires less than 1W and is shown in Figure 11. This design is biased from ±12V supplies and uses a transformer with a turns ratio of only 1:1.2. Although the peak current is only 140mA, the LT1886 cannot be used due to its limited operating supply voltage of 13.2V total. Instead the LT1795CFE, which is in a very small TSSOP power package, is used. This small package is ideal for central office, multiple DSL port designs for compacting a high number of drivers on a single PC card.

**ADSL Full Rate Downstream (CO) Line Driver**

Figure 12 is the highest powered DSL line driver application, used in central office applications to obtain up to 8Mbps data rates throughout the Internet. This design uses standard back termination and can be powered from ±12V supplies. Instead of using the standard value of R BT resistors, the circuit still reduces the amount of received signal. It is most applicable for systems that use a sensitive receiver AFE that can still detect the reduced received signal.

The approach is termed active termination. A small amount of positive feedback in each amplifier is obtained from the opposite amplifier output. This feedback makes the effective output impedance seen looking into the circuit at nodes C and D the proper value even though the R BT resistor has been reduced by 40% from what is should be. The design equations for this topology are as follows.

Instead of using the standard value of R BT, it can be reduced to any value desired, with attendant received-signal loss. A factor called K can be used to define the new R BT resistance:

\[
R_{BT} = \frac{K \cdot Z_{LINE}}{2 \cdot n^2}
\]

With standard termination and a 1:1.5 turns ratio transformer, the value of R BT should be 22Ω. In the design of Figure 13, this resistor is reduced by 40% to 13.3Ω, therefore the factor K = 0.6.

The normal forward path circuit gain from the noninverting input of each amplifier to the output nodes A and B is a term called G where \( G = 1 + \frac{R_F}{R_G} \).

The gain of the positive feedback signal path for each side (from node D to A and from node C to B, is called P where \( P = \frac{R_P}{R_F} \).
Using these abbreviations:
For proper impedance matching: \( P = 1 - K \).

To obtain a desired voltage gain from the AFE output to the line, \( A_V \), the term \( G \) is set to:

\[
G = \frac{A_V \cdot e_{PRI}}{e_{LINE}} \cdot (1 + K - P) - P \quad (17)
\]

where \( e_{PRI} \) and \( e_{LINE} \) are the voltages at the transformer primary and on the line, determined by taking into account the turns ratio and transformer insertion loss.

The use of a high performance amplifier such as the LT1795 does not result in any degradation of distortion performance when modifying the closed-loop gain by positive feedback. Significant power savings can be obtained but the design may not be suitable for all applications as previously mentioned.

**Conclusion**

Following the design procedures described in this article should make the design and implementation easy and accurate. At the very least, it will ensure that power and heat issues receive proper consideration.

Linear Technology offers a variety of high speed, low distortion power amplifiers and low noise dual amplifiers that can be used to implement the driver/receiver functions of the DSL modem (see Table 3).