Serial Interface for High Speed Data Converters Simplifies Layout over Traditional Parallel Devices

*Introduction*

The LTC2274 is a 105Msps, 16-bit ADC that simplifies the digital connection between the ADC and FPGA by replacing the usual parallel interface with a novel high speed serial interface, thus reducing the typical number of required data input/output (I/O) lines from 16 CMOS or 32 LVDS parallel data lines to a single, self-clocking, differential pair communicating at 2.1Gbps. This frees up valuable FPGA pins and board space. It also allows flexibility to route across analog and digital boundaries—in noise sensitive applications, the serial interface provides an effective isolation barrier between digital and analog circuitry and serves to eliminate coupling between the digital outputs and analog inputs to reduce digital feedback.

*Current Mode Logic and 8B/10B Encoding Allows High Speed Serial Data Transfer*

The LTC2274 achieves excellent signal to noise ratio (SNR) performance of 77.6dBFS and spurious free dynamic range (SFDR) of 100dB at baseband, as shown in Figure 1. The input topology of the LTC2274 family is based on its predecessor, the LTC2207 family, and achieves similar AC performance. However, the LTC2274 differs from the LTC2207 in its output structure. The LTC2274 uses an 8B/10B encoder to encode and serialize the data before it is transmitted. 8B/10B encoding is a process that takes 8 bits of data and encodes them into 10 bits to ensure zero DC offset and a limited run length. To encode a 16-bit word, the LTC2274 must transmit 20 bits of serial data. This requires that the serial data must be transmitted at 2 times the clock frequency of the ADC. Sampling at 105Msps requires the LTC2274 to transmit serial data at 2.1GHz. This is beyond the usable range of LVDS signaling, and therefore requires a faster, more robust differential signaling scheme. The LTC2274’s differential signaling uses current mode logic (CML), which is capable of transmitting data in excess of 10GHz.

Current mode logic uses a differential output transistor pair (usually N-type) to steer current into resistive loads. The output swing and offset depends on the bias current and termination resistance. The output driver bias current is typically 16mA, generating a signal swing potential of 400mV (800mV differential) across the combined internal and external termination resistance of 25Ω on each output. LVDS typically uses 3.5mA to develop its signal swing, and the capacitance of the ESD protection diodes becomes a limiting factor for transmission speed. CML uses more current, and therefore this capacitance becomes less of a limiting factor to data throughput.

CML is typically faster than LVDS. A typical LVDS output stage requires four transistors to steer current into the load, usually using both P-channel and N-channel devices. A mixture of N- and P-channel makes it difficult to produce devices that have the same characteristics. P-channel devices are often slower—that is, if an N-channel
and a P-channel device are cascaded, the P-channel cannot pull up the signal as fast as the N-channel can pull down. This causes the output waveform to be distorted, which can lead to bit errors, and limits the speed at which LVDS can transfer data.

The LTC2274 CML driver is implemented with only N-channel devices, which allows faster throughput rates. Since CML only sinks current, it has true differential signal, which improves signal integrity. The eye diagram and bathtub curves of the LTC2274 are shown in Figure 2. The eye diagram shows very little variation cycle to cycle of the CML logic output, and the bathtub curve shows that total jitter in the signal is less than 0.35UI (unit interval). This equates into a very clean uniform signal that can easily be received by a properly terminated receiver.

**Termination of CML**

CML must be terminated for proper operation. Figure 3a shows a recommended design in which an FPGA receiver uses internal 50Ω pull up resistors for termination. These resistors pull up to the OV\textsubscript{DD} of the LTC2274. OV\textsubscript{DD} must be between 1.2V and 3.3V to ensure proper operation. The signal has a common mode voltage of OV\textsubscript{DD} – 0.2V. The directly-coupled differential termination of Figure 3b may be used in the absence of a receiver termination voltage within the required range. In this case, the common mode voltage is shifted down to approximately 400mV below OV\textsubscript{DD}, requiring an OV\textsubscript{DD} in the range of 1.4V to 3.3V. If the serial receiver’s common mode input requirements are not compatible with the directly-coupled termination modes, the DC balanced 8B/10B encoded data permits the addition of DC blocking capacitors as shown in Figure 3c. In this AC-coupled mode, the termination voltage is determined by the receiver’s requirements. The coupling capacitors should be selected appropriately for the intended operating bit-rate, usually between 1nF and 10nF. In AC coupled mode, the output common mode voltage is approximately 400mV below OV\textsubscript{DD}, so the OV\textsubscript{DD} supply voltage should be in

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**Figure 3. CML termination schemes**
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CML Power Consumption
With a constant 16mA of bias current and a voltage swing of 800mV differential, CML logic consumes a moderate amount of power. For an equal data rate, CML logic consumes less total power than PECL and LVPECL. A single CML driver uses more power than a single LVDS driver, but only marginally more that the three pairs of LVDS drivers required for a typical LVDS serial bus.

8B/10B Encoding Makes for Simple Connection
The 8B/10B encoding process results in an average DC offset of zero, allowing the data to be routed through transformers or fiber channel transceivers that can provide isolation between the digital and analog realm. 8B/10B encoding also does not require a framing signal or a data clock, whereas both are required in traditional serial communication. 8B/10B encoding transmits data over a single pair of data lines, whereas a typical serial LVDS serial bus requires three or more pairs, and a typical parallel ADC can require more than 16 pairs.

The complexity of decoding 8B/10B lies in the receiver. Fortunately Xilinx, Altera and Lattice have solutions to receive data from the LTC2274 and decode the 8b/10b data, simplifying the collection of 8b/10b data. Other 8b/10b decoding solutions may be available. The FPGA required to receive data from the LTC2274 must be able to receive high speed serial transmissions of 2GHz or more.

Conclusion
Without sacrificing resolution or sample rate, the LTC2274 delivers full 16-bit performance at 105Msps over a single pair of transmission lines, greatly simplifying layout and saving valuable board space. This mitigates interaction with other circuitry in software defined radio, base station or industrial applications which involve many channels of an ADC routed to one FPGA.

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