High speed analog-to-digital converters (ADCs) are by definition devices that sample an analog signal and, as such, must have sample clock inputs. Some system designers that utilize ADCs have observed a slower than expected startup from the time the sample clock is initially applied. Surprisingly, the cause of this delay has often been the wrong start-up polarity of the externally applied ADC sample clock.

Many high speed ADCs have sample clock inputs that have the following characteristics:
- Differential
- Internally biased to a set input common-mode voltage (VCM)
- Designed for ac coupling to the clock source

This discussion applies to converters having clock buffers that have these properties.

Differential ADC clock input buffers often have a designed in toggle threshold offset. If there were no such offset, the toggle threshold would occur at 0 V differential. In the case where a clock buffer with no offset were undriven and ac-coupled, the clock inputs (CLK+ and CLK−) would each be pulled internally to the common-mode voltage. In this case the dc voltage on CLK+ and the voltage on CLK− would be the same, which means that the differential voltage equals 0 V.

In an ideal world with no signal on the inputs, the clock buffer would not toggle. In reality there is always at least some noise in electronic systems. In this hypothetical case where the input toggle threshold is 0 V, any noise on the inputs will cross the toggle threshold of the clock buffer and cause inadvertent toggling.

When sufficient input toggle threshold offset is designed into the clock buffer, the same conditions will not cause toggling. As such, designing in an offset to the toggle threshold voltage of ac-coupled differential clock buffers is beneficial and for this reason, clock buffers often include a toggle threshold offset.

With no clock applied, CLK+ and CLK− will each be pulled to the same VCM by the internal biasing circuit in the clock buffer. When the clock is initially applied, the clock edges on CLK+ and CLK− will swing positively and negatively, or negatively and positively away from the previously established VCM. In Figure 1, VCM = 0.9 V.

Figure 1 shows the clock being applied after it has been inactive (either when first bringing up the system, or after the clock driver has been inactive for a period of time). In this case, CLK+ swings positive on the first edge and CLK− swings negative. With a positive offset added to the input toggle threshold, this clock signal will toggle the clock buffer on its first edge, as shown in Figure 1. The clock input buffer will produce a clock right away.

If perchance the clock was started with the opposite polarity, CLK− swings positive on the first edge and CLK+ swings negative. With the same positive offset added to the input toggle threshold, this clock signal will not toggle the clock buffer on its first edge and subsequent edges until the waveform is pulled toward steady state, and crosses the toggle threshold over time, as shown in Figure 2.
As can be seen, the polarity of the initial start-up clock makes a difference in toggling a clock buffer with input threshold offset. In one case (CLK+ initially rising in this example) the clock buffer will ideally start toggling immediately when the clock is first applied. With the opposite polarity (CLK+ initially falling in this example), the clock buffer will not start toggling immediately when the clock is first applied.

If you are seeing an unexpected delay in ADC startup, try reversing the clock start-up polarity. This could make a difference in your start-up time.

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