Precision measurement is extending into application areas that require greater and greater power efficiency. This is particularly true with the advent of IoT, which is driving greater need for wireless sensor nodes with precision measurement capability, battery-powered wearable fitness/medical devices, and industrial signal chains that use isolated power, 4 mA to 20 mA loop-powered or battery-powered field instruments. In these scenarios, greater power efficiency means longer battery lives with less maintenance as well as simplified power supply design.

Typically, precision measurement systems use low dropout regulators (LDOs) as part of their power supply schemes to generate low noise rails for precision ADCs. However, LDOs can be very inefficient in delivering power and often the majority of power is lost in the LDO dissipated as heat. This article discusses a means of achieving a higher efficiency power solution for your precision successive approximation register (SAR) ADC. This is achieved by using an ultralow power switching regulator in a hysteretic mode and analyzing the performance trade-offs—including a means to intelligently control the switching regulator synchronous to the SAR conversion to improve noise performance.

Fixed frequency or pulse-width modulated (PWM) switching regulators provide a very efficient (often >90%) means of generating voltage rails in a measurement system at medium to high load currents (hundreds of mA to multiple A). However, this efficiency comes at the cost of switching ripple that is usually at a fixed frequency of hundreds of kHz to a couple of MHz. As seen in Figure 1, the power supply rejection ratio (PSRR) of a typical precision SAR ADC is very good at low frequencies up to ~100 kHz—beyond this the PSRR drops off rapidly.

![Figure 1. SAR ADC analog power supply rejection vs. frequency.](image)

Typical load currents to supply the VDD line of a precision SAR ADC are in the couple mA range or µA if the ADC is run at a lower throughput—so there are no efficiency benefits in using a fixed frequency switcher to supply the ADC directly instead of an LDO.

However, high efficiency, ultralow power step-down switching regulators can be operated in a hysteretic mode with very low quiescent current.

In hysteretic mode, the regulator charges the output voltage slightly higher than its nominal output voltage with PWM pulses by regulating the constant peak inductor current. When the output voltage increases until the output sense signal exceeds the hysteresis upper threshold, the regulator enters standby mode. In standby mode, the high-side and low-side MOSFETs and a majority of the circuitry are disabled to allow a
low quiescent current as well as high efficiency performance, as seen in Figure 2. During standby mode, the output capacitor supplies energy into the load, and the output voltage decreases until it falls below the hysteresis comparator lower threshold. The regulator wakes up and generates the PWM pulses to charge the output again.

In the hysteretic case, the switching ripple frequency is a function of the load current and LC network and for loads of a couple mAs is in the kHz range. At a few kHz, the PSRR of the precision ADC is very good and will do a good job of rejecting/attenuating the switching ripple at the ADC digital output.

Take for example the circuit shown in Figure 3 with the AD7980 ADC; its \( V_{DD} \) current consumption is typically 1.5 mA at full throughput (1 MSPS) and scales linearly as you decrease the throughput. As can be seen in Figure 4, the switching frequency ripple is 4.5 kHz and 50 mV peak-to-peak on a 2.5 V regulated output from a 5 V rail. This ripple is attenuated at the ADC digital output by the PSRR rating of the ADC. In the ADC FFT output it shows up as a spur of magnitude \(-120\) dBFS at 4.5 kHz. For a 5 V input range on the ADC, this equates to

\[
5 \times 10^{-120} \text{ dBFS} = 5 \mu V \text{ p–p}
\]

This level of ripple showing up in the ADC output is extremely low for a 16-bit converter; 5 \( \mu V \) peak-to-peak corresponds to 0.07 LSB at 16 bits. Ripple at this level is buried in the ADC noise floor and requires a large amount of averaging to uncover it and will not be seen in many applications. This output ripple corresponds to a PSRR of

\[
20 \times \log \left( \frac{50 \text{ mV}}{5 \mu V} \right) = 80 \text{ dB}
\]

This measurement is similar to what is shown in Figure 1 for the AD7980 PSRR of \(~77\) dB at 4.5 kHz.

![Figure 2. PWM (top) and hysteretic mode (bottom)—efficiency vs. load current.](image)

![Figure 3. AD7980 and ADP5300 application circuit.](image)

![Figure 4. ADP5300 hysteretic switching ripple (ac-coupled) when supplying the AD7980 and ripple tone in ADC FFT output at 1 MSPS throughput.](image)
If the ADC throughput is reduced to 10 kSPS then the current consumption of the ADC scales linearly down to 15 μA (factor of ~100) and correspondingly, the switching frequency ripple of the ADP5300 scales to 46.5 Hz (factor of ~100) with an amplitude of 55 mV peak-to-peak, as seen in Figure 5. The ripple shows up in the ADC FFT output at 46 Hz again with an amplitude of −120 dB (5 μV peak-to-peak) because the PSRR is similar at this frequency. There is evidence of a second harmonic at 93 Hz that is −125 dB down.

Figure 5. ADP5300 hysteretic switching ripple (ac-coupled) when supplying the AD7980 and ripple tone in ADC FFT output at 10 kSPS throughput.

Figure 6 shows how the efficiency of the ADP5300 stacks up vs. that of an LDO across ADC throughput rate when regulating a 2.5 V output from a 5 V rail. As you would expect, the switcher is far more efficient at delivering power than the LDO, 90% vs. 50% (for a 5 V input) at 1 MSPS and holds up much better at lower ADC throughputs/lower current consumption, staying above 80% until 5 kSPS.

At an ADC throughput of 1 MSPS using an LDO, the current consumed from a 5 V rail is 1.5 mA or 7.5 mW. Using the ADP5300, the current consumed from a 5 V rail is 828 μA or 4.1 mW. This is a 3.4 mW or 45% reduction in the power drawn by the ADC power supply.

Figure 6. Efficiency vs. ADC throughput for ADP5300 and LDO.

The performance of the AD7980 at 1 MSPS using the ADP5300 as the $V_{DD}$ supply is shown in Figure 7 with a 10 kHz almost full-scale input signal (−0.5 dB). The ADC still meets data sheet specifications in terms of SNR (91.5 dB) and THD (−103 dB). However, the ADP5300 switching ripple at 4.5 kHz gets modulated on top of the input signal and appears as spurs at 10 kHz − 4.5 kHz (5.5 kHz) and 10 kHz + 4.5 kHz (14.5 kHz). These spurs are still at a very low level (−116 dBFS) and much less than the THD introduced by the second harmonic of the fundamental signal (−103.8 dBFS at 20 kHz). These artifacts are a small fraction of an LSB at the 16-bit level, so in many applications it will be perfectly acceptable for the power savings of the ADP5300 regulator.

Figure 7. Performance of AD7980 using ADP5300 as $V_{DD}$ supply. Side bands due to switching ripple modulation can be seen around the fundamental signal (10 kHz ±4.5 kHz).
There is a STOP switching feature on the ADP5300 switcher that can completely eliminate these switching ripple artifacts from showing up in the ADC FFT output. The STOP pin on the ADP5300 prevents the SW pin from switching when STOP is held high. This can be used to prevent any switching from occurring during the noise sensitive conversion process of the ADC. In order to achieve this the CNV signal and STOP signal are tied together (see Figure 3) and the CNV signal from the processor is timed to remain high during the conversion time of the ADC. In the case of the AD7980 this is 710 ns max and conversion is initiated on the CNV rising edge. The results are shown in Figure 8. The ripple frequency is more variable in this case, as there are only specific times when the SW node can turn on and regulate. Also note that the SW turn-on time from the STOP signal going low can be hundreds of ns. In Figure 8, the SW pin turns on ~850 ns after the falling edge of STOP. This means we cannot use the STOP feature at 1 MSPS ADC throughput as the VDD supply will fall out of regulation and collapse, as there is insufficient time for the SW pin to go high and regulate. Instead, the STOP function will work for throughputs of 500 kSPS and lower.

As can be seen in Figure 9, the switching ripple spur is completely eliminated from the ADC noise floor with the use of the STOP signal. When an input signal of 10 kHz is applied there is no modulation or artifacts around the fundamental, apart from the normal harmonics. However, there is an efficiency hit for using the STOP feature due to ringing on the SW pin when the SW pin is disabled (STOP high). The efficiency of the ADP5300 with an ADC throughput of 500 kHz drops to ~75%. This is still considerably higher than the efficiency possible with an LDO (<50%) and gives the option of a power/performance trade-off that can be made in the application under the control of the processor/microcontroller if a separate control line is used for the STOP feature.

The cost and PCB area of a switcher solution like the ADP5300 is comparable to that of an LDO. The main addition to the BOM is a chip inductor, a 2.2 μH inductor can be as small as 0603 size, with the input and output caps already being required for an LDO solution. This makes it an attractive alternative to using an LDO in power sensitive applications without significantly impacting precision performance.

High efficiency, ultralow power switching regulators like the ADP5300 result in 45% power savings over LDOs when powering precision ADCs like the AD7980 from a 5 V rail. This has many benefits in IoT applications, extending battery life in wireless sensor nodes or wearable fitness devices, power sensitive isolated industrial systems, and 4 mA to 20 mA loop-powered systems.

**Figure 8.** ADP5300 switching ripple (yellow) with STOP function at 500 kSPS throughput, CNV/STOP signal (blue), and SW pin of ADP5300 (pink).

**Figure 9.** Performance of AD7980 using ADP5300 as VDD supply with STOP feature timed to conversion period.

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**About the Author**

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