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Product Errata

to fix this issue is to ensure that the SDAIN short pulse never occurs. Adding capacitance to SDAIN to prevent the short pulse from rising above 1V is a good solution. This and other solutions are discussed in the next section.

Possible Workarounds

Linear Technology Corporation recommends the following fixes in applications where the problem occurs:

- Observe the SDAIN short pulses before and after the 9th clock of each byte when the master is communicating with the LTC4302-1/LTC4302-2, LTC4305, LTC4306. Add capacitance to the SDAIN line to prevent SDAIN from ever rising above 1V during a short pulse. Adding the same capacitance to SCLIN is also recommended to optimize timing on the I²C bus.

- For new mux designs not requiring pin compatibility with the LTC4305, LTC4306 and not requiring channel selectability by I²C software, users may choose the LTC4312 and LTC4314 2-Channel and 4-Channel Pin Selectable I²C Muxes with Bus Buffers. Channel selection is done out-of-band via ENABLE channel select pins. The LTC4312 and LTC4314 do not contain I²C interface circuitry and therefore do not have any issues with SDAIN short pulses.

- For new single bus buffer designs not requiring pin compatibility with the LTC4302-1/LTC4302-2 and not requiring control by I²C software, users may choose the LTC4300A-1, LTC4303 or LTC4307 I²C bus buffers. These buffers do not contain I²C interface circuitry and therefore do not have any issues with SDAIN short pulses.

- For a given unit, the time window in which the problem occurs is quite narrow – on the order of a few nanoseconds. Due to the narrow time window coupled with random cycle-to-cycle variations, a write operation that fails on the first attempt will often succeed on subsequent attempts. While less than optimal and not guaranteed to work in all cases, adding a software loop to write a register, read back the register contents to confirm the new data, and retry the write if the previous write failed, often fixes the problem.