LTC3880

August 2014

LTC3880 ERRATA

The errata below describe conditions that cause an LTC®3880 device to operate differently than expected or described in the data sheet.

ERRATA SUMMARY

ERRATA #1: RESTORE_USER_ALL

The device ignores resistor programmable parameters when RESTORE_USER_ALL is executed, even if bit 6 of MFR_CONFIG_ALL_LTC3880 is clear.

Conditions:

The following conditions, when present simultaneously, may expose this problem:

1) Resistor configuration pins are used to set any portion of the device behavior instead of EEPROM.
2) A RESTORE_USER_ALL command is issued to the device.

Impact:

Communication at the expected device address can be lost when the above conditions occur. The LTC3880 always responds at global addresses 0x5A and 0x5B, but writing data to these locations is not generally recommended. In a system with multiple LTC PSM devices with the same global address, important parameters such as output voltage or PWM frequency may be incorrect.

Root Cause:

Internal firmware does not use resistor configuration pins to set device configuration when RESTORE_USER_ALL is executed, regardless of the state of bit 6 of MFR_CONFIG_ALL_LTC3880. Only values stored in EEPROM are applied.

Additional RESTORE_USER_ALL Deviations:

RESTORE_USER_ALL does not execute the full device initialization described in the "Power Up and Initialization" segment of the data sheet Operations section. This command will not execute when the die temperature is above 130°C. Faults are not cleared by execution of RESTORE_USER_ALL. When this command is executed, only the related EEPROM contents are copied to RAM PMBus command space after disabling both PWM channels, if either is on. Channels that are then configured to be on will not be enabled after RAM is loaded until that channel's MFR_RESTART_DELAY has expired.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Contact LTC Factory Applications for assistance.

Use MFR_RESET – Where resistor programmable parameters are required, MFR_RESET can be used in lieu of RESTORE_USER_ALL to load all PMBus command values from EEPROM into working RAM while properly applying settings programmed by external resistors.

Program the Device Strictly with EEPROM – The desired value of bus address, output voltage, and PWM frequency and phase can be programmed into EEPROM by issuing the appropriate PMBus commands, setting bit 6 of MFR_CONFIG_ALL_LTC3880, and issuing a STORE_USER_ALL command. When using this programming method, the

ASEL pin should be left open to ensure power-up behavior is self-consistent. Once the device is configured in this fashion, RESTORE_USER_ALL will work properly. EEPROM configuration can also be loaded during the production process. Contact LTC sales for details.

ERRATA #2: FAULT LOG

The fault log cyclical data containing status for the past six ADC events may appear out of order.

Conditions:

The following conditions, when present simultaneously, may expose this problem:

1) The fault log is enabled, bit 7 of MFR_CONFIG_ALL set to a 1.
2) A fault occurred and data is stored in NVM or the user issues a MFR_FAULT_LOG_STORE command.
3) VIN is lost or the part is reset, reloading the fault log information from NVM

Impact:

The fault log cyclical data may be out of order for the past six ADC event logs. Users may have to interpret the fault log data carefully to discern the correct order of the past six events prior to the time the fault occurred.

Root Cause:

A pointer indicating the most recent event location is not initialized correctly.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Contact LTC Factory Applications for assistance.

Use information in the fault log header to debug the system problem – The header is always correct and contains the reason the fault log was generated, a time stamp of how long the part was running prior to the fault, the maximum input voltage, the maximum output voltage and output current for both rails. In addition the header contains the most recent internal die temperature and peak inductor temperatures for both rails. Data in the header is often sufficient to debug a system problem.

Discern the event time location from information in the event log – The status in the cyclical data can potentially be used to provide more information .Good status indicates the event stored is an earlier point in time than bad status.

ERRATA #3: VOUT_TRANSITION_RATE

The VOUT_TRANSITION_RATE slope can be much greater than programmed if the commanded value is set below 0.1V/ms.

Conditions:

The following conditions, when present simultaneously, may expose this problem:

1) The VOUT_TRANSITION_RATE is set below 0.1V/ms.
2) The output voltage is adjusted while the output is on either by margining the part or by changing the VOUT command.

Impact:

The slope of VOUT may be greater than programmed.

Root Cause:

There is a math error in the remainder portion of the VOUT_TRANSITION_RATE slope calculation. When the value in the VOUT_TRANSITION_RATE command is small, the remainder portion of the calculation can be a large percentage of the overall slope calculation. Large errors in the remainder can cause subsequent large errors in the overall calculation.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Contact LTC Factory Applications for assistance.

Verify the slope for a specific VOUT_TRANSITON_RATE value. If large errors are seen, slightly modify the value in the command until acceptable slopes are achieved –

The math error only occurs at specific VOUT_TRANSITION_RATE values. Adjusting the value slightly will produce desired slopes for the application. The default value for the command is 0.25V/ms. At this transition rate, the slope calculation is accurate.

Send new VOUT commands separated in time to achieve the desired slope – Have the system host achieve the desired slope by synthesizing the output ramp through a series of timed VOUT commands.

ERRATA #4: THE ALERTB PIN LOW WHEN SET TO IGNORE THE CONDITION

The ALERTb pin can be asserted low if the GPIOb pin is pulled low as VIN is applied or if the part comes out of reset when I^2C traffic is present.

Conditions:

The following conditions, when present simultaneously, may expose this problem:

1) The GPIOb pin is held low when VIN is applied or the part is reset. The ALERTb pin will be asserted low even if the part is programmed not to assert ALERTb when GPIOb is held low.
2) I^2C communication occurs before the LTC3880 is out of reset and only a portion of the command is seen by the part. This communication can be interpreted as CML faults. If CML faults are detected, the ALERTb pin is asserted low.

Impact:

The ALERTb pin may be asserted when it is configured to not be. This may cause the system firmware to process more information than is required to determine the source of the problem.

Root Cause:

During reset the part defaults to assert the ALERTb pin when the above conditions are met. This occurs before the circuitry is able to override this assertion. Once the ALERTb pin is asserted, it is latched and must be cleared.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Contact LTC Factory Applications for assistance.

Wait at least 150ms after issuing a reset before communicating with the part – This assures the LTC3880 will not miss a portion of the I^2C communication and misinterpret the input data causing a CML fault.

Issue a clear faults command shortly after VIN is applied – This will clear all faults and de-assert the ALERTb pin.

Assert bit 0 of MFR_CONFIG_ALL_LTC3880 – This is the default configuration of the part. The part will issue a clear faults command when the RUN pins are released de-asserting the ALERTb pin. Before the RUN pins are released the system host must ignore ALERTb assertions.

Resolve the board issue holding GPIO low before the part fully initializes– The GPIOb pins are not held low by the LTC3880. If the pins are low at power-up there is likely a board issue. Use the ALERTb signal and the host to resolve the location of the board problem.

ERRATA #5: STATUS_WORD VS STATUS_BYTE

Bits in STATUS_WORD LSB may be asserted when the STATUS_WORD MSB reports all zeros.

Conditions:

The following conditions, when present simultaneously, may expose this problem:

1) When polling STATUS_WORD, if a fault occurs at the right time, the read value can have a bit set in the lower byte with no corresponding bits set in the upper byte.

Impact:

A minor inconsistency can occur when firmware is polling the STATUS_WORD register of the part.

Root Cause:

The two bytes making up STATUS_WORD are transferred separately to the I^2C controller of the LTC3880. If STATUS_WORD is read between transfers, an incoherent read can occur.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Contact LTC Factory Applications for assistance.

Poll STATUS_BYTE instead of STATUS_WORD – STATUS_BYTE indicates the part status sufficiently.

Poll STATUS_WORD twice if a discrepancy is detected – STAUS_WORD will poll correctly immediately after the first incorrect reading.

ERRATA #6: MINOR SHOOT-THROUGH WITH LOW QG FETS

The part may exhibit minor shoot-through and lower than expected efficiency using some of the next generation low QG FETs at high output current levels.

Conditions:

The following conditions, when present simultaneously, may expose this problem:

1) The power stage contains low gate charge FETs such as the 25V Infineon MOSFETs (specifically the BSC050NE2LS and BSC010NE2LSI).

2) The rail output current exceeds 25 Amps per phase.

Impact:

The conversion efficiency may be less than expected causing excess current on VIN.

Root Cause:

Under very large transient load conditions, ground bounce may cause the TG driver to turn back on when it should be off.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Contact LTC Factory Applications for assistance.

Place a 4Ω resistor in series with the TG pin to the gate of the top FET – This resistor is used in conjunction with the normally recommended 2Ω resistor between the boost diode and the boost pin. The 4Ω resistor slows down the TG falling edge sufficiently to reduce ground bounce and prevent the TG pin from turning back on.

Use a 30V FET in place of the 25V top FET – The 30V FET, shown in all the data sheet examples, requires more gate charge to turn off. The extra gate charge increases the turn-off time of the Top FET reducing ground bounce thereby preventing the TG pin from turning back on.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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