MAX6399:
Safety Application Note

Failure-In-Time, Failure Mode Distribution and Pin Failure Mode and Effects Analysis

OCTOBER 2027

Contents

1 | Overview

The scope of this document is to provide a report on MAX6399 to support in functional safety designs. This contains:

- Failure-In-Time (FIT) rates of the component calculated in accordance with the industry reliability standards
- Failure Mode Distribution of the device (FMD)
- Pin Failure Mode and Effects Analysis (Pin FMEA)

General Description

The MAX6399 is a high-voltage protection switch controller designed to safeguard DC-DC converters from undervoltage (UV) and overvoltage (OV) conditions. It actively monitors the output voltage and rapidly disconnects the load in case of overvoltage conditions, while a power-OK signal asserts during an input UV condition.

Key features include adjustable DC-DC output OV and DC-DC input UV thresholds, an internal charge pump circuitry that can generate a gate voltage up to 10V for optimal MOSFET drive, and various protection mechanisms such as internal overtemperature shutdown and latch-off functionality. The device operates across a wide range from 5.75V to 72V and is available in a compact TDFN package specified from -40°C to +125°C.

Table 1-1 Product Description

Part Number	Primary Function	System Function
MAX6399	High-voltage protection switch controller	The gate output pulls low to turn OFF the external switch during an overvoltage (OV) or overtemperature condition, and asserts POK when an undervoltage (UV) condition is detected.

Figure 1-1 shows the product specific block diagram of MAX6399.

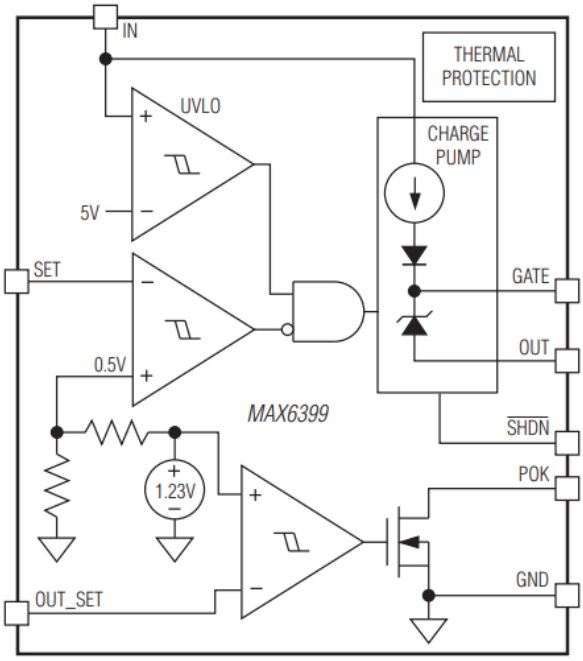

Figure 1-1 MAX6399 Block Diagram

MAX6399 was developed following a quality-managed development process in compliance with ISO 9001 quality management system standards but was not developed in compliance with IEC61508 safety standard. The associated certificates are available on Quality Certificates | Analog Devices.

2 | Functional Safety Failure-In-Time (FIT) Rates

This section offers specific details on the base functional safety failure-in-time (FIT) rates for MAX6399, according to SN29500, IEC 62380 and accelerated testing conditions of HTOL. It also identifies the relevant component category for each standard, allowing customers to compute their own failure rates.

- Table 2-1 provides FIT rates according to SN29500
- Table 2-2 provides FIT rates according to IEC 62380
- Table 2-3 provides FIT rates according to HTOL

The FIT rates of MAX6399 based on SN29500 for a specific industrial mission profile is detailed below:

Table 2-1 Functional Safety Component FIT Rate According to SN29500

SN29500 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Predicted Component FIT Rate	30.38

- Mission Profile: 20 years constant operation at 55°C temperature
- Climate type: World-wide (Table 8)
- Operating Voltage (max): 72V
- Power Dissipation: 9.36mW
- Theta-JA: 41°C/W
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT
- Part is sensitive to drift

Note 1: For applications requiring a different mission profile, the following information can be used to calculate the base FIT rate based on SN29500.

- SN29500 part and section: Part 2/Section 5 and ASICs
- Sub-category: CMOS, BiCMOS
- Integration Density: 50-5k

The FIT rates of MAX6399 based on IEC62380 for a specific industrial mission profile is detailed below:

Table 2-2 Functional Safety Component FIT Rates According to IEC62380

IEC62380 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5.17
Die FIT Rate	0.39
Package FIT Rate	4.78

Note 2: For applications requiring a different mission profile, the following information can be used to calculate the base FIT rate based on IEC62380.

- FIT rate calculation model: Section 7.3.1, refer to Mathematical Model
- IEC62380 part and section for die FIT rate: Table 16, MOS ASIC circuits, Full Custom
- Production year for die FIT rate: 2005
- Integration Density: 50-5k
- IEC62380 part and section for package FIT rate: Table 17b, Peripheral Connection Packages
- Package type: TDFN 8 pins, length: 3mm, width: 3mm, pitch: 0.65mm
- Interface device (EOS relevant): No

The FIT rates of MAX6399 based on accelerated testing conditions of HTOL is detailed below:

Table 2-3 Functional Safety Component FIT Rates According to HTOL Testing

Confidence Level	FIT (Failures Per 10^9 Hours)
70%	3.87
90%	7.40
95%	9.63
99%	14.81

Note 3: The FIT rates for various confidence levels were determined through HTOL reliability studies, utilizing the Arrhenius equation for acceleration assuming a chi-square distribution using the following test parameters:

- Sample size: 4,007
- Number of Failures: 0
- Activation Energy: 0.7eV
- Raw Device Hours: 4,038,432
- Accelerated Temperature: 55°C
- Equivalent Accelerated Device Hours: 310,971,509

3 | Failure Mode Distribution (FMD)

The failure mode distribution includes all relevant failure modes of the product function as defined in the product description.

Table 3-1 shows the failure mode distribution estimation for MAX6399 as derived from the component die area ratio and complexity, and from engineering expertise.

Since some failures had no effect and do not contribute to any failure mode, the total percentage of the Failure Mode Distribution would not add up to 100%. A Correction factor (CF) was applied to the distribution to account for failures with no effect on the system.

System Function

- The gate output pulls low to turn OFF the external switch during an overvoltage (OV) or overtemperature condition, and asserts POK when an undervoltage (UV) condition is detected.

Table 3-1 Failure Mode Distribution (CF = 1.91)

Failure Modes	Failure Mode Distribution
Cannot pull GATE output low	19%
Cannot pull-up GATE output higher than supply	27%
GATE output pulled up early	1%
GATE output pulled up late	1%
GATE output pulled low early	16%
GATE output pulled low late	6%
POK always asserted	16%
POK never asserted	10%
POK asserted early	2%
POK asserted late	2%

4 | Pin Failure Mode and Effects Analysis (Pin FMEA)

This section presents the Pin Failure Mode and Effects Analysis (Pin FMEA) for MAX6399. The failure modes discussed in this section encompass the common pin-by-pin failure scenarios:

- Pin short-circuited to supply (see Table 4-1)
- Pin short-circuited to GND (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to adjacent pins (see Table 4-4)

Figure 4-1 illustrates the pin diagram for MAX6399. Refer to the product datasheet for a detailed description of each pin's function.

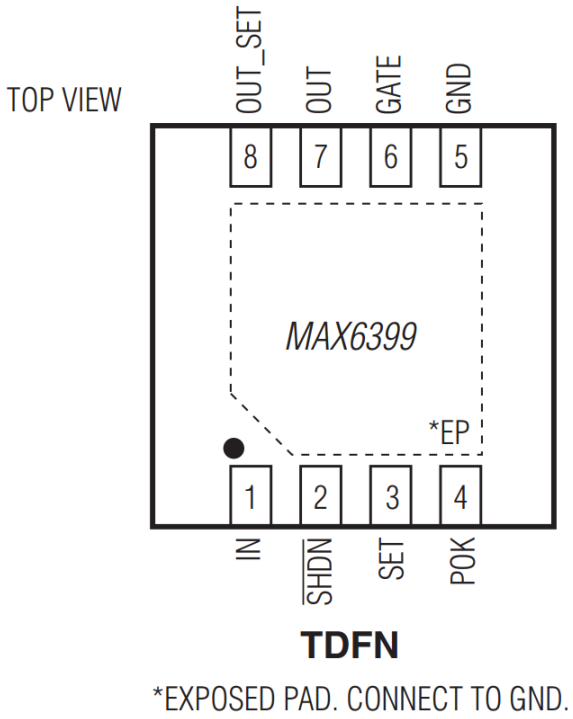

Figure 4-1. MAX6399 Pin Diagram

Below are the usage assumptions and device configuration considered for the Pin FMEA, based on the Typical Application Circuit, unless otherwise noted:

- The supply voltage is VIN = 12V, and POK is pulled up to 3.3V.
- The operating temperature range (TA) is from -40°C to +125°C.

Table 4-1 Pin FMEA for MAX6399 Pins Short-Circuited to Supply

Pin no.	Pin Name	Effect of Failure Mode
1	IN	No effect
2	$\overline{\text{SHDN}}$	No response when $\overline{\text{SHDN}}$ forced low, but system can still detect faults
3	SET	Part always in OV. GATE always low. External switch always OFF
4	POK	POK always high
5	GND	Part not functional
6	GATE	GATE stuck at supply
7	OUT	External switch bypassed. Can control GATE voltage but IN shorted to OUT
8	OUT_SET	No UV detection

Table 4-2 Pin FMEA for MAX6399 Pins Short-Circuited to GND

Pin no.	Pin Name	Effect of Failure Mode
1	IN	Part not functional
2	$\overline{\text{SHDN}}$	GATE always low. External switch always OFF
3	SET	OV condition not detected. GATE will not be pulled down. External switch still ON when it should be OFF
4	POK	POK always low
5	GND	No effect
6	GATE	GATE always low. External switch always OFF
7	OUT	IN shorted to OUT in normal operation. Excessive current through external switch
8	OUT_SET	Part always in UV. POK always low

Table 4-3 Pin FMEA for MAX6399 Pins Open-Circuited

Pin no.	Pin Name	Effect of Failure Mode
1	IN	Part not functional
2	$\overline{\text{SHDN}}$	No response when $\overline{\text{SHDN}}$ forced low
3	SET	OV condition not detected. GATE will not be pulled down. External switch still ON when it should be OFF
4	POK	Unreliable POK
5	GND	Part not functional
6	GATE	No control on external switch. External switch always OFF
7	OUT	No effect
8	OUT_SET	Unreliable POK output

Table 4-4 Pin FMEA for MAX6399 Pins Short-Circuited to Adjacent Pins

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
1	IN	$\overline{\text{SHDN}}$	No response when $\overline{\text{SHDN}}$ forced low, but system can still detect faults
2	$\overline{\text{SHDN}}$	SET	Indeterminate input on $\overline{\text{SHDN}}$ (input above VIL but less than VIH) but system can still detect faults
3	SET	POK	When POK is high, part always in OV. GATE always low. External switch always OFF When POK is low, OV condition not detected. GATE will not be pulled down. External switch still ON when it should be OFF
4	POK	GND	POK always low
5	GND	GATE	GATE always low. External switch always OFF
6	GATE	OUT	GATE stuck at OUT. Switch VGS = 0. External switch always OFF
7	OUT	OUT_SET	No UV detection.
8	OUT_SET	IN	No UV detection. POK always high

5 | Revision History

Revision	Revision Date	Description
A	October 2024	Initial Release

IMPORTANT NOTES AND DISCLAIMER

PLEASE BE AWARE THAT THE PRODUCT IN QUESTION HAS NOT BEEN DEVELOPED IN ACORDANCE WITH INDUSTRIAL SAFETY STANDARDS AND IS NOT RECOMMENDED FOR SUCH APPLICATIONS AS PER THE SPECIFIC DATA SHEET. THIS REPORT IS INTENDED SOLELY TO PROVIDE THE CUSTOMER WITH DETAILED INFORMATION ON FAILURE MODES AND THEIR DISTRIBUTION ACCORDING TO IEC61508, RELATED TO THE POTENTIAL USE OF QUALITY-MANAGED PARTS FOR SPECIFIC HARDWARE EVALUATION CLASS AS DESCRIBED IN THIS STANDARD.

ANALOG DEVICES AIMS TO ASSIST CUSTOMERS IN DESIGNING AND CREATING THEIR OWN END-PRODUCT SOLUTION THAT COMPLY WITH RELEVANT FUNCTIONAL SAFETY STANDARDS AND REQUIREMENTS. THEREFORE, ANALOG DEVICES DOES NOT GUARANTEE SIL COMPLIANCE AT THE SYSTEM LEVEL. ANALOG DEVICES WILL NOT BE RESPONSIBLE FOR ANY CLAIMS OR DAMAGES ARISING FROM THE CUSTOMER'S USE OF AN ANALOG DEVICES PRODUCT IN LIFE SUPPORT, LIFE-CRITICAL, OR SAFETY-CRITICAL SYSTEMS, EQUIPMENT OR APPLICATIONS. CUSTOMERS WILL INDEMNIFY, DEFEND AND HOLD ANALOG DEVICES HARMLESS FROM ANY CLAIMS, DAMAGES, LOSSES, COSTS, EXPENSES, AND LIABILITIES RESULTING FROM THE USE OF ANY ANALOG DEVICES PRODUCT IN SUCH SYSTEMS, EQUIPMENT, OR APPLICATIONS. ANALOG DEVICES DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THIS DOCUMENTATION AND WILL NOT BE LIABLE FOR ITS CONTENT

www.analog.com

AHEAD OF WHAT'S POSSIBLE™