MAX17525:
Safety Application Note

Failure-In-Time, Failure Mode Distribution and Pin Failure Mode and Effects Analysis

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Contents

1 | Overview

The scope of this document is to provide information to support integrating the MAX17525 into functional safety designs. This contains:

- Failure-In-Time (FIT) of the component calculated in accordance with the industry reliability standards
- Failure Mode Distribution of the device (FMD)
- Pin Failure Mode and Effects Analysis (Pin FMEA)

General Description

The MAX17525 adjustable overvoltage, undervoltage, and overcurrent protection device guards systems against overcurrent faults in addition to positive overvoltage and reverse-voltage faults. When used with an optional external pMOSFET, the device also protects downstream circuitry from voltage faults up to +60V, -60V (for -(60V +VOUT) external PFET rating). The device features a low, 31mΩ, on-resistance integrated FET.

During startup, the MAX17525 is designed to charge large capacitances on the output in a continuous mode for applications where large reservoir capacitors are used on the inputs to downstream devices. Two additional options that feature a dual-stage, current-limit mode in which the current is continuously limited to 1.5x and 2x the programmed limit, are available upon request. These options enable faster charging of large load capacitances during startup. The MAX17525 also features reverse-current and overtemperature protection. The device is available in a 20-pin (5mm x 5mm) TQFN package and operates over the -40°C to 125°C temperature range.

Table 1-1 Product Description

Part Number	Primary Function	System Function
MAX17525	High-Accuracy, Adjustable Power Limiter	Protects circuits by detecting fault conditions—such as overvoltage, undervoltage, overtemperature, reverse current, or overcurrent—and, upon detection, disconnects OUT from IN, asserts $\overline{\text{FLAG}}$, and pulls the GP pin high to disable the external PFET.

Figure 1-1 shows the product specific block diagram of MAX17525.

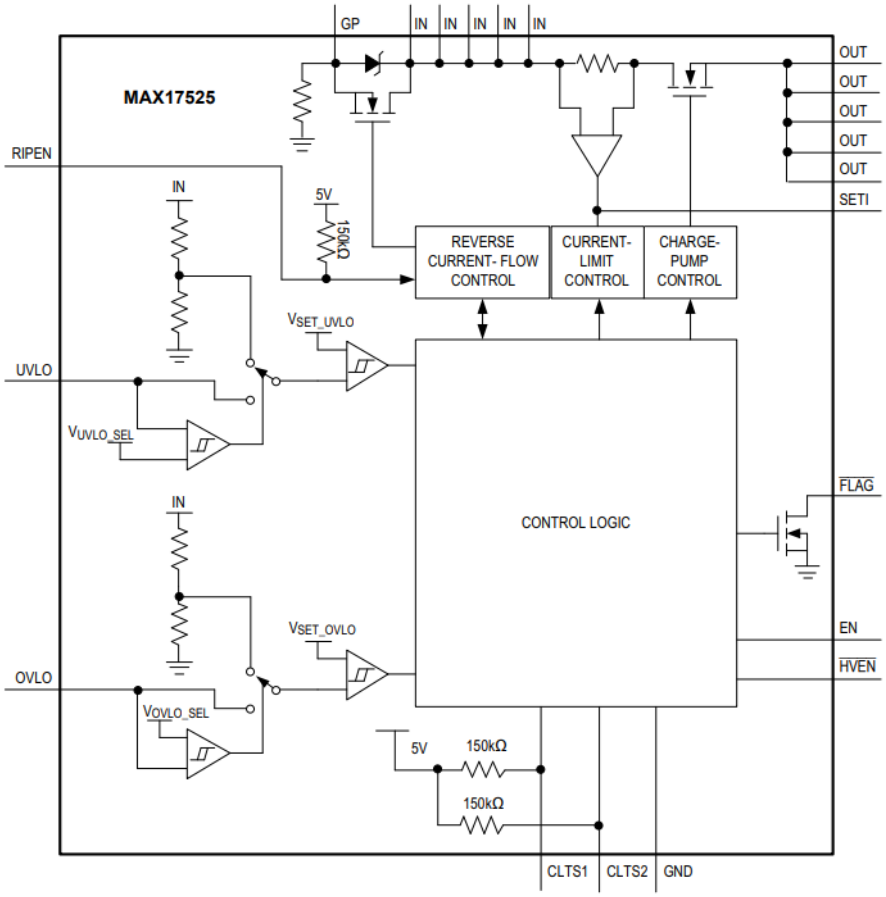

Figure 1-1 MAX17525 Block Diagram

The MAX17525 was developed following a quality-managed development process in compliance with the ISO 9001 quality management system standards but was not developed in compliance with IEC 61508 safety standard. The associated certificates are available on Quality Certificates | Analog Devices.

2 | Functional Safety Failure-In-Time (FIT) Rates

This section offers specific details on the base functional safety failure-in-time (FIT) for MAX17525, according to SN 29500, IEC 62380 and accelerated testing conditions of high-temperature operating life (HTOL). It also identifies the relevant component category for each standard, allowing customers to compute their own failure rates.

- Table 2-1 provides FIT rates according to SN 29500
- Table 2-2 provides FIT rates according to IEC 62380
- Table 2-3 provides FIT rates according to HTOL

The FIT of MAX17525 based on SN 29500 for a specific industrial mission profile is detailed below:

Table 2-1 Functional Safety Component FIT Rate According to SN 29500

SN 29500 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Predicted Component FIT	44.54

- Mission Profile: 20 years constant operation at 55°C temperature
- Operating Voltage (max): 60V (based on product datasheet)
- Power Dissipation: 130mW
- Theta-JA: 29°C/W

Note 1: For applications requiring a different mission profile, the following information can be used to calculate the base FIT based on SN 29500.

- SN 29500 part: Part 2 Table 5 and ASICs
- Sub-category: BiCMOS
- Integration Density: 5k-50k
- Part is sensitive to drift.

The FIT of MAX17525 based on IEC 62380 for a specific industrial mission profile is detailed below:

Table 2-2 Functional Safety Component FIT Rates According to IEC 62380

IEC 62380 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Total Component FIT	6.06
Die FIT	4.98
Package FIT	1.08

Note 2: For applications requiring a different mission profile, the following information can be used to calculate the base FIT based on IEC 62380.

- FIT calculation model: Section 7.3.1, refer to Mathematical Model
- IEC 62380 part and section for die FIT: Table 16, MOS ASIC circuits, Full Custom
- Production year: 2016
- Integration Density: 5k-50k
- Climate type: World-wide (Table 8)
- IEC 62380 part and section for package FIT: Table 17b, Peripheral Connection Packages
- Package type: TQFN 20 pins, length: 5 mm, width: 5mm, pitch: 0.65mm
- Technology Structure: Bipolar BiCMOS (High Voltage)
- Substrate Material: Epoxy Glass (FR4, G-10)
- EOS FIT assumed: 0 FIT

The FIT of MAX17525 based on accelerated testing conditions of HTOL is detailed below:

Table 2-3 Functional Safety Component FIT Rates According to HTOL Testing

Confidence Level	FIT (Failures Per 10^9 Hours)
70%	0.19
90%	0.37
95%	0.48
99%	0.73

Note 3: The FIT values for various confidence levels were determined through HTOL reliability studies, utilizing the Arrhenius equation for acceleration assuming a chi-square distribution using the following test parameters:

- Sample size: 31185
- Number of Failures: 0
- Activation Energy: 0.7eV
- Accelerated Temperature: 55°C
- Equivalent Accelerated Device Hours: 6,280,926,146

3 | Failure Mode Distribution (FMD)

The failure mode distribution includes all relevant failure modes of the product function as defined in the product description.

The application circuit shown in Figure 3-1 is considered in calculating the FMD. Table 3-1 shows the failure mode distribution estimation for MAX17525 as derived from the component die area ratio and complexity, and from engineering expertise.

3-1 Application Circuit

The MAX17525 protects the system from overcurrent, reverse current, overvoltage, undervoltage, and overtemperature conditions. In this application, the circuit monitors a 24V supply and operates in Continuous Current-Limit mode, configured by leaving the CLTS1 and CLTS2 pins floating since they are internally pulled-up. The current-limit threshold is set to 1A, determined by the 37.5kΩ resistor connected to the SETI pin. An external PFET, controlled by the GP pin, blocks current flow during reverse current events. The OVLO and UVLO pins are connected to a resistor divider, setting the overvoltage lockout threshold at 27V and the undervoltage lockout threshold at 21V. The $\overline{\text{FLAG}}$ pin and EN pin are pulled up by the system controller, while a weak pullup is added to the GP pin to ensure a defined state for the external PFET.

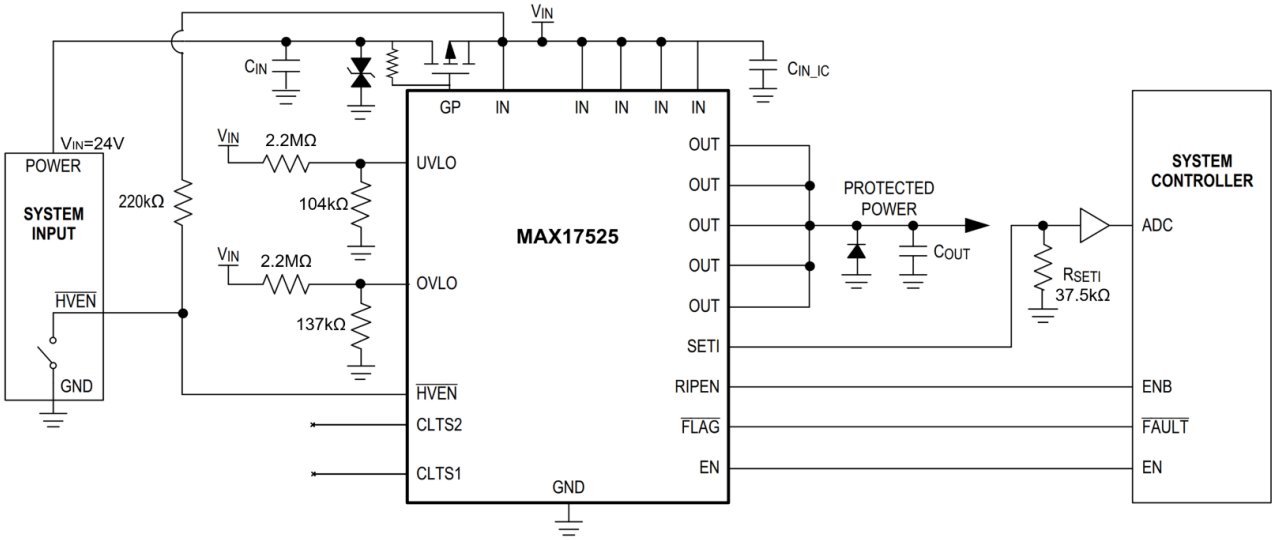

Figure 3-1 Application Use Case Simplified Schematic Diagram

System Function

- Protects circuits by detecting fault conditions—such as overvoltage, undervoltage, overtemperature, reverse current, or overcurrent—and, upon detection, disconnects OUT from IN, asserts $\overline{\text{FLAG}}$, and pulls the GP pin high to disable the external PFET.

Table 3-1 Failure Mode Distribution

Failure Modes	Failure Mode Distribution
Loss of at least one detection or protection capability	41%
Inadvertent trip of at least one detection or protection capability	31%
At least one detection or protection feature trip before it should	1%
At least one detection or protection feature trip after it should	1%
No effect on system function	26%

4 | Pin Failure Mode and Effects Analysis (Pin FMEA)

This section presents the Pin Failure Mode and Effects Analysis (Pin FMEA) for MAX17525. The failure modes discussed in this section encompass the common pin-by-pin failure scenarios:

- Pin short-circuited to supply (see Table 4-1)
- Pin short-circuited to GND (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to adjacent pins (see Table 4-4)

Figure 4-1 illustrates the pin diagram for MAX17525. Refer to the product datasheet for a detailed description of each pin's function.

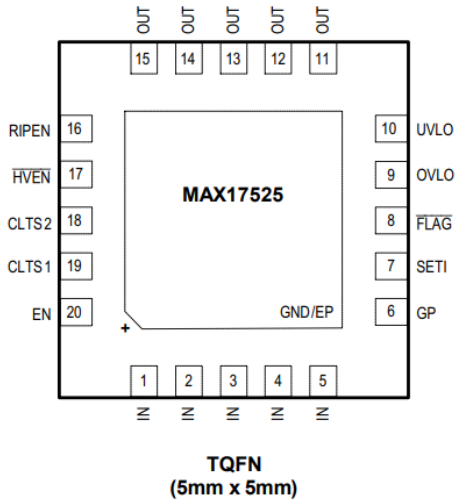

Figure 4-1. MAX17525 Pin Diagram

Below are the usage assumptions and device configuration considered for the Pin FMEA:

- The $\overline{\text{FLAG}}$ pin requires an external pull-up resistor if the system controller does not already have it internally.
- EN pin is pulled high by System Controller GPIO. See discussion in section 3-1.
- The CLTS1, CLTS2, and GP pins are configured as per application circuit. See discussion in section 3-1.
- The UVLO and OVLO threshold voltages are set to 21V and 27V, respectively.
- The supply voltage (VIN) is set to 24V, and the operating temperature range (T_A) is from -40ºC to +125°C.

Table 4-1 Pin FMEA for MAX17525 Pins Short-Circuited to Supply

Pin no.	Pin Name	Effect of Failure Mode
1	IN	No effect.
2	IN	No effect.
3	IN	No effect.
4	IN	No effect.
5	IN	No effect.
6	GP	External PFET is stuck in the off state. Reverse current protection is always active. However, GP pin's maximum rating is exceeded, leading to destructive conditions.
7	SETI	SETI pin's maximum rating is exceeded, leading to destructive conditions.
8	$\overline{\text{FLAG}}$	$\overline{\text{FLAG}}$ pin's maximum rating is exceeded, leading to destructive conditions.
9	OVLO	OVLO pin's maximum rating is exceeded, leading to destructive conditions.
10	UVLO	UVLO pin's maximum rating is exceeded, leading to destructive conditions.
11	OUT	Internal NFET will not be able to disconnect OUT from IN when a failure occurs.
12	OUT	Internal NFET will not be able to disconnect OUT from IN when a failure occurs.
13	OUT	Internal NFET will not be able to disconnect OUT from IN when a failure occurs.
14	OUT	Internal NFET will not be able to disconnect OUT from IN when a failure occurs.
15	OUT	Internal NFET will not be able to disconnect OUT from IN when a failure occurs.
16	RIPEN	RIPEN pin's maximum rating is exceeded, leading to destructive conditions.
17	$\overline{\text{HVEN}}$	$\overline{\text{HVEN}}$ is primarily used to manually clear latched faults. No effect on the system function.
18	CLTS2	CLTS2 pin's maximum rating is exceeded, leading to destructive conditions.
19	CLTS1	CLTS1 pin's maximum rating is exceeded, leading to destructive conditions.
20	EN	EN pin's maximum rating is exceeded, leading to destructive conditions.
-	GND/EP	Part is not functional.

Table 4-2 Pin FMEA for MAX17525 Pins Short-Circuited to GND

Pin no.	Pin Name	Effect of Failure Mode
1	IN	The IN pins are internally shorted to each other. The part does not receive power and does not function.
2	IN	The IN pins are internally shorted to each other. The part does not receive power and does not function.
3	IN	The IN pins are internally shorted to each other. The part does not receive power and does not function.
4	IN	The IN pins are internally shorted to each other. The part does not receive power and does not function.
5	IN	The IN pins are internally shorted to each other. The part does not receive power and does not function.
6	GP	External PFET is always on. GP pin cannot be pulled high even when reverse current is detected.
7	SETI	Shorting SETI to ground asserts $\overline{\text{FLAG}}$ output. External PFET and internal NFET are turned off.
8	$\overline{\text{FLAG}}$	$\overline{\text{FLAG}}$ is always asserted. No effect on other outputs.
9	OVLO	OVLO threshold is set to the internal threshold. OV monitoring is unreliable because the externally set OV threshold (27V) is lower than the internal threshold (36V).
10	UVLO	UVLO threshold is set to the internal threshold. UV monitoring is unreliable because the externally set UV threshold (21V) is higher than the internal threshold (12V).
11	OUT	Overcurrent is detected. $\overline{\text{FLAG}}$ is always asserted and OUT is disconnected from IN.
12	OUT	Overcurrent is detected. $\overline{\text{FLAG}}$ is always asserted and OUT is disconnected from IN.
13	OUT	Overcurrent is detected. $\overline{\text{FLAG}}$ is always asserted and OUT is disconnected from IN.
14	OUT	Overcurrent is detected. $\overline{\text{FLAG}}$ is always asserted and OUT is disconnected from IN.
15	OUT	Overcurrent is detected. $\overline{\text{FLAG}}$ is always asserted and OUT is disconnected from IN.
16	RIPEN	Reverse-current flow protection is disabled.
17	$\overline{\text{HVEN}}$	$\overline{\text{HVEN}}$ is primarily used to manually clear latched faults; it has no effect on the system function.
18	CLTS2	Device switches to latch-off mode from continuous current limit mode. No effect on the system function.
19	CLTS1	Device stays in continuous current limit mode. No effect.
20	EN	EN is primarily used to manually clear latched faults. EN cannot clear latched faults.
-	GND/EP	No effect.

Table 4-3 Pin FMEA for MAX17525 Pins Open-Circuited

Pin no.	Pin Name	Effect of Failure Mode
1	IN	No effect as long as other IN pins are connected to supply.
2	IN	No effect as long as other IN pins are connected to supply.
3	IN	No effect as long as other IN pins are connected to supply.
4	IN	No effect as long as other IN pins are connected to supply.
5	IN	No effect as long as other IN pins are connected to supply.
6	GP	External PFET is always off due to weak pull-up in application circuit.
7	SETI	The current limit is set to 0A, which results in overcurrent detection. GP pin is pulled high and internal NFET is turned off, and $\overline{\text{FLAG}}$ asserts.
8	$\overline{\text{FLAG}}$	$\overline{\text{FLAG}}$ is always de-asserted. No effect on other outputs.
9	OVLO	OV detection feature is not functional. The system cannot detect overvoltage, but other functions remain active.
10	UVLO	UV detection feature is not functional. The system cannot detect undervoltage, but other functions remain active.
11	OUT	No effect on system function. Downstream load can still receive protected power if other OUT pins are connected.
12	OUT	No effect on system function. Downstream load can still receive protected power if other OUT pins are connected.
13	OUT	No effect on system function. Downstream load can still receive protected power if other OUT pins are connected.
14	OUT	No effect on system function. Downstream load can still receive protected power if other OUT pins are connected.
15	OUT	No effect on system function. Downstream load can still receive protected power if other OUT pins are connected.
16	RIPEN	Reverse-current flow protection is always active due to being internally pulled up. No effect on the system function.
17	$\overline{\text{HVEN}}$	$\overline{\text{HVEN}}$ is primarily used to manually clear latched faults; it has no effect on the system function.
18	CLTS2	Device is always in continuous current limit mode due to internal pullup. No effect.
19	CLTS1	Device is always in continuous current limit mode due to internal pullup. No effect.
20	EN	EN is primarily used to manually clear latched faults. EN cannot clear latched faults.
-	GND/EP	Part is not functional.

Table 4-4 Pin FMEA for MAX17525 Pins Short-Circuited to Adjacent Pins

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
1	IN	IN	No effect as these pins are internally shorted.
2	IN	IN	No effect as these pins are internally shorted.
3	IN	IN	No effect as these pins are internally shorted.
4	IN	IN	No effect as these pins are internally shorted.
5	IN	GP	External PFET is stuck in the off state. Reverse current protection is always active.
6	GP	SETI	GP output is greater than 6V, which exceeds SETI pin's absolute maximum rating, leading to destructive conditions.
7	SETI	$\overline{\text{FLAG}}$	Voltage across SETI is 3.9V which causes $\overline{\text{FLAG}}$ to assert. This will then cause an overcurrent fault that will ground both $\overline{\text{FLAG}}$ and SETI, thus turning off the external PFET and NFET, and keeping $\overline{\text{FLAG}}$ asserted.
8	$\overline{\text{FLAG}}$	OVLO	$\overline{\text{FLAG}}$ will assert due to an overvoltage detection which also causes the internal threshold to take over thus de-asserting the $\overline{\text{FLAG}}$ output. $\overline{\text{FLAG}}$ output oscillates.
9	OVLO	UVLO	Both external resistor dividers are in parallel, causing both an overvoltage and undervoltage fault. $\overline{\text{FLAG}}$ will assert, and OUT pins are disconnected from IN.
10	UVLO	OUT	UVLO pin's maximum rating of 20V is exceeded, leading to destructive conditions.
11	OUT	OUT	No effect as these pins are internally shorted.
12	OUT	OUT	No effect as these pins are internally shorted.
13	OUT	OUT	No effect as these pins are internally shorted.
14	OUT	OUT	No effect as these pins are internally shorted.
15	OUT	RIPEN	RIPEN pin's maximum rating is exceeded, leading to destructive conditions.
16	RIPEN	$\overline{\text{HVEN}}$	RIPEN pin's maximum rating is exceeded, leading to destructive conditions.
17	$\overline{\text{HVEN}}$	CLTS2	CLTS2 pin's maximum rating is exceeded, leading to destructive conditions.
18	CLTS2	CLTS1	No effect. Both pins are internally pulled up.
19	CLTS1	EN	No effect.
20	EN	IN	EN pin's maximum rating is exceeded, leading to destructive conditions.

5 | Revision History

Revision	Revision Date	Description
A	06Dec25	Initial Release

IMPORTANT NOTES AND DISCLAIMER

PLEASE BE AWARE THAT THE PRODUCT IN QUESTION HAS NOT BEEN DEVELOPED IN ACORDANCE WITH INDUSTRIAL SAFETY STANDARDS AND IS NOT RECOMMENDED FOR SUCH APPLICATIONS AS PER THE SPECIFIC DATA SHEET. THIS REPORT IS INTENDED SOLELY TO PROVIDE THE CUSTOMER WITH DETAILED INFORMATION ON FAILURE MODES AND THEIR DISTRIBUTION ACCORDING TO IEC61508, RELATED TO THE POTENTIAL USE OF QUALITY-MANAGED PARTS FOR SPECIFIC HARDWARE EVALUATION CLASS AS DESCRIBED IN THIS STANDARD.

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