MAX16137:
Safety Application Note

Failure-In-Time, Failure Mode Distribution and Pin Failure Mode and Effects Analysis

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Contents

1 | Overview

The scope of this document is to provide information to support integrating the MAX16137 into functional safety designs. This contains:

- Failure-In-Time (FIT) of the component calculated in accordance with the industry reliability standards
- Failure Mode Distribution of the device (FMD)
- Pin Failure Mode and Effects Analysis (Pin FMEA)

General Description

The MAX16137 is a low-voltage, ±1% accurate supervisory circuit that monitors a single system supply voltage for undervoltage and overvoltage faults within a factory set threshold window. When the monitored supply voltage drops below the undervoltage threshold or goes above the overvoltage threshold, the reset output asserts low. The reset output deasserts after the reset timeout period when the supply voltage returns to within the undervoltage and overvoltage threshold window. The reset output is active low available in either the push-pull or open-drain options. The MAX16137 offers factory-trimmed nominal input voltage options from 0.5V to 5V in approximately 20mV increments. A variety of factory-trimmed undervoltage/overvoltage thresholds from ±4% to ±11% are available to accommodate different supply voltages and tolerances.

The MAX16137 features a unique Built-In-Self-Test (BIST) diagnostic capability that monitors the health of the internal reset circuit during power-up. If the Built-In-Self-Test fails, the MAX16137 asserts $\overline{\text{BIST}}$ low. During normal operation, the MAX16137 performs an on-demand BIST when the $\overline{\text{CLR/BIST}}$ is pulled low for more than 150µs. The MAX16137 is available in a small, 2mm x 2mm, 8-pin TDFN side-wettable package and operates over the automotive temperature range of -40°C to +125°C.

Table 1-1 Product Description

Part Number	Primary Function	System Function
MAX16137	Window supervisor	Monitors a single system supply voltage for undervoltage (UV) and overvoltage (OV) conditions

Figure 1-1 shows the product specific block diagram of MAX16137.

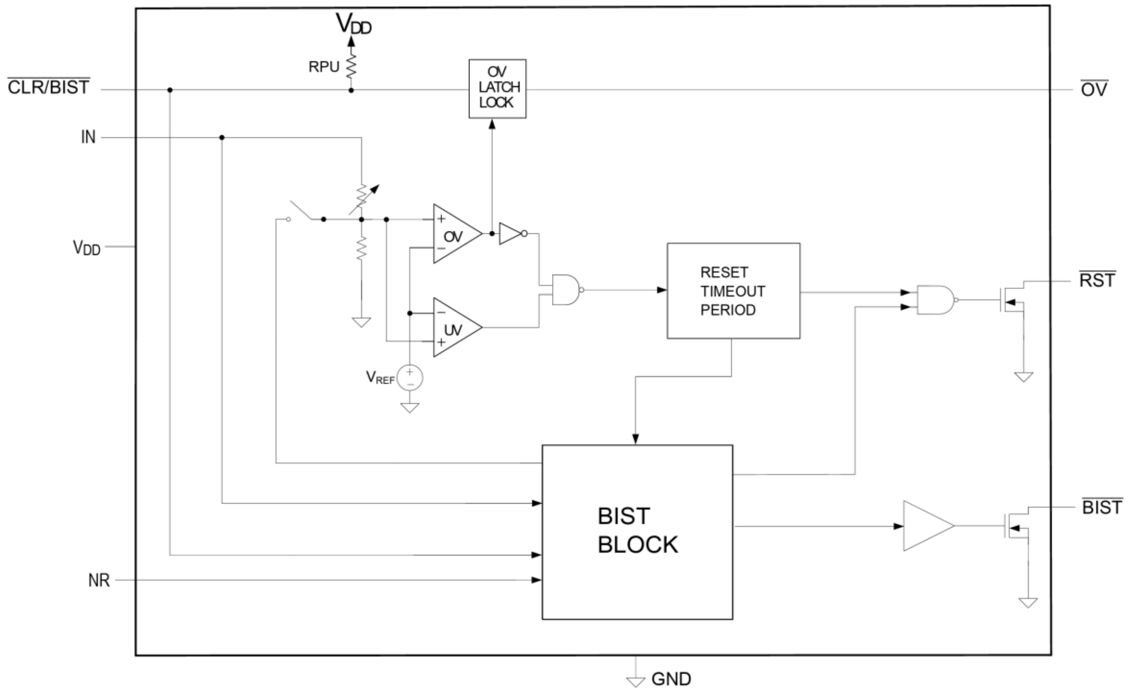

Figure 1-1 MAX16137 Block Diagram

The MAX16137 was developed following a quality-managed development process in compliance with the ISO 9001 quality management system standard but was not developed in compliance with the IEC 61508 safety standard. The associated certificates are available on Quality Certificates | Analog Devices.

2 | Functional Safety Failure-In-Time (FIT)

This section offers specific details on the base functional safety failure-in-time (FIT) for MAX16137, according to SN 29500, IEC 62380 and accelerated testing conditions of high-temperature operating life (HTOL). It also identifies the relevant component category for each standard, allowing customers to compute their own failure rates.

- Table 2-1 provides FIT according to SN 29500
- Table 2-2 provides FIT according to IEC 62380
- Table 2-3 provides FIT according to HTOL

The FIT of MAX16137 based on SN 29500 for a specific industrial mission profile is detailed below:

Table 2-1 Functional Safety Component FIT According to SN 29500

SN 29500 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Predicted Component FIT	50.04

- Mission Profile: 20 years constant operation at 55°C temperature
- Operating Voltage (max): 5.5V
- Power Dissipation: 126.5uW
- Package Thermal Resistance, Junction-to-Ambient (Θ_{JA}): 162°C/W

Note 1: For applications requiring a different mission profile, the following information can be used to calculate the base FIT based on SN 29500.
- SN 29500 part: Part 2 Table 5 under ASICs
- Sub-category: CMOS, BiCMOS
- Integration Density: 5k-50k
- Part is sensitive to drift

The FIT of MAX16137 based on IEC 62380 for a specific industrial mission profile is detailed below:

Table 2-2 Functional Safety Component FIT According to IEC 62380

IEC 62380 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Total Component FIT	4.40
Die FIT	4.20
Package FIT	0.20

Note 2: For applications requiring a different mission profile, the following information can be used to calculate the base FIT based on IEC 62380.
- FIT calculation model: Section 7.3.1, refer to Mathematical Model
- IEC 62380 part and section for die FIT: Table 16, MOS ASIC circuits, Full Custom
- Production year for die FIT: 2021
- Integration Density: 5k-50k
- Climate type: World-wide (Table 8)
- IEC 62380 part and section for package FIT: Table 17b, Peripheral Connection Packages
- Package type: TDFN 8 pins, length: 2mm, width: 2mm, pitch: 0.5mm
- Technology Structure: MOS BiCMOS (Low Voltage)
- Substrate Material: FR4
- EOS FIT assumed: 0 FIT

The FIT of MAX16137 based on accelerated testing conditions of HTOL is detailed below:

Table 2-3 Functional Safety Component FIT According to HTOL Testing

Confidence Level	FIT (Failures Per 10^9 Hours)
70%	0.19
90%	0.37
95%	0.48
99%	0.73

Note 3: The FIT for various confidence levels were determined through HTOL reliability studies, utilizing the Arrhenius equation for acceleration assuming a chi-square distribution using the following test parameters:

- Sample size: 31185
- Number of Failures: 0
- Activation Energy: 0.7eV
- Accelerated Temperature: 55°C
- Equivalent Accelerated Device Hours: 6280926146

3 | Failure Mode Distribution (FMD)

The failure mode distribution includes all relevant failure modes of the product function as defined in the product description.

Table 3-1 shows the failure mode distribution estimation for MAX16137 as derived from the component die area ratio and complexity, and from engineering expertise.

System Function

- Monitors a single system supply voltage for undervoltage (UV) and overvoltage (OV) conditions. Asserts $\overline{\text{OV}}$ when an overvoltage is detected and asserts $\overline{\text{RST}}$ when either OV or UV condition occurs.

Table 3-1 Failure Mode Distribution

Failure Modes	Failure Mode Distribution
At least one output pin always asserts	28%
At least one output pin never asserts[1]	33%
At least one output pin will assert early[2]	3%
At least one output pin will assert late[3]	10%
Loss of BIST function[4]	6%
No effect on system function[5]	20%

Note 4:

[1] $\overline{\text{RST}}$ no longer responds to UV faults while both $\overline{\text{RST}}$ and $\overline{\text{OV}}$ no longer respond to OV faults.

[2] Early assertion due to a shift in the voltage threshold (i.e. UV threshold of 3.14V triggers at 3.45V and/or OV threshold at 3.48V triggers at 3.13V)

[3] Late assertion due to a shift in the voltage threshold (i.e. UV threshold of 3.14V triggers at 2.83V and/or OV threshold at 3.48V triggers at 3.82V)

[4] Loss of BIST includes:

- Impaired on-demand BIST initiation capability
- Faults cannot be detected once BIST is initiated

[5] The following were of no effect on the primary system function:

- $\overline{\text{BIST}}$ can still assert when a fault is detected even when the device is stuck in on-demand BIST mode
- $\overline{\text{OV}}$ clears immediately but continues to respond to OV faults
- Negligible timing discrepancies upon output pin de-assertion
- Power-on threshold drift and thermal shutdown drift failure

4 | Pin Failure Mode and Effects Analysis (Pin FMEA)

This section presents the Pin Failure Mode and Effects Analysis (Pin FMEA) for MAX16137. The failure modes discussed in this section encompass the common pin-by-pin failure scenarios:

- Pin short-circuited to supply (see Table 4-1)
- Pin short-circuited to GND (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to adjacent pins (see Table 4-4)

Figure 4-1 illustrates the pin diagram for MAX16137. Refer to the product datasheet for a detailed description of each pin's function.

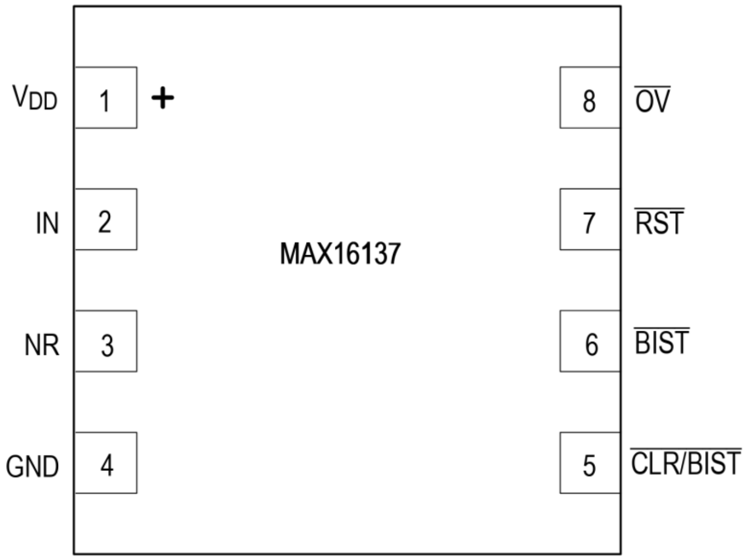

Figure 4-1. MAX16137 Pin Diagram

Below are the usage assumptions and device configuration considered for the Pin FMEA, based on the Typical Application Circuit, unless otherwise noted:

- The operating voltage range for VDD is from 1.71V to 5.5V, and the operating temperature range is from -40°C to +125°C.
- The $\overline{OV}$, $\overline{RST}$, and $\overline{CLR/BIST}$ pins are connected to a 10kΩ pull-up resistor.
- Typical values are measured at VDD = 5V, and ambient operating temperature (T_A)= +25°C.

Table 4-1 Pin FMEA for MAX16137 Pins Short-Circuited to Supply

Pin no.	Pin Name	Effect of Failure Mode
1	VDD	This is the default configuration. No effect.
2	IN	OV is always detected. $\overline{\text{RST}}$ and $\overline{\text{OV}}$ are always low.
3	NR	Supply is grounded and part has no power. Part is not functional.
4	GND	Part is not functional. All output pins will never assert.
5	$\overline{\text{CLR/BIST}}$	$\overline{\text{CLR/BIST}}$ is also internally pulled high. On-demand BIST cannot be initiated externally if pulled high.
6	$\overline{\text{BIST}}$	$\overline{\text{BIST}}$ is always high.
7	$\overline{\text{RST}}$	$\overline{\text{RST}}$ is always high.
8	$\overline{\text{OV}}$	$\overline{\text{OV}}$ is always high.

Table 4-2 Pin FMEA for MAX16137 Pins Short-Circuited to GND

Pin no.	Pin Name	Effect of Failure Mode
1	VDD	Part is not functional. All output pins will never assert.
2	IN	UV is always detected. $\overline{\text{RST}}$ is always low.
3	NR	This is the assumption in the application circuit. No effect.
4	GND	This is the default configuration. No effect.
5	$\overline{\text{CLR/BIST}}$	On-demand BIST will be initiated and $\overline{\text{RST}}$ will intermittently assert. $\overline{\text{OV}}$ can still respond to OV faults but will not latch.
6	$\overline{\text{BIST}}$	$\overline{\text{BIST}}$ is always low.
7	$\overline{\text{RST}}$	$\overline{\text{RST}}$ is always low.
8	$\overline{\text{OV}}$	$\overline{\text{OV}}$ is always low.

Table 4-3 Pin FMEA for MAX16137 Pins Open-Circuited

Pin no.	Pin Name	Effect of Failure Mode
1	VDD	Part has no power. Part is not functional.
2	IN	UV is always detected. $\overline{\text{RST}}$ is always low.
3	NR	No effect during normal operation.
4	GND	Part is not functional. All output pins will never assert.
5	$\overline{\text{CLR/BIST}}$	$\overline{\text{CLR/BIST}}$ is internally pulled high. On-demand BIST cannot be initiated so BIST function is lost.
6	$\overline{\text{BIST}}$	$\overline{\text{BIST}}$ is always high.
7	$\overline{\text{RST}}$	$\overline{\text{RST}}$ is always high.
8	$\overline{\text{OV}}$	$\overline{\text{OV}}$ is always high.

Table 4-4 Pin FMEA for MAX16137 Pins Short-Circuited to Adjacent Pins

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
1	VDD	IN	OV is always detected. $\overline{\text{RST}}$ and $\overline{\text{OV}}$ are always low.
2	IN	NR	UV is always detected. $\overline{\text{RST}}$ is always low.
3	NR	GND	This is the assumption in the application circuit. No effect.
4	GND	$\overline{\text{CLR/BIST}}$	On-demand BIST will be initiated and $\overline{\text{RST}}$ will intermittently assert. $\overline{\text{OV}}$ can still respond to OV faults but will not latch.
5	$\overline{\text{CLR/BIST}}$	$\overline{\text{BIST}}$	$\overline{\text{CLR/BIST}}$ and $\overline{\text{BIST}}$ output are both pulled high by default. $\overline{\text{BIST}}$ output will follow $\overline{\text{CLR/BIST}}$ input. No effect on system function.
6	$\overline{\text{BIST}}$	$\overline{\text{RST}}$	Outputs shorted together. $\overline{\text{RST}}$ and $\overline{\text{BIST}}$ OR-ed together.
7	$\overline{\text{RST}}$	$\overline{\text{OV}}$	Outputs shorted together. $\overline{\text{OV}}$ and $\overline{\text{RST}}$ OR-ed together.
8	$\overline{\text{OV}}$	VDD	$\overline{\text{OV}}$ is always high.

5 | Revision History

Revision	Revision Date	Description
A	25Aug26	Initial Release

IMPORTANT NOTES AND DISCLAIMER

PLEASE BE AWARE THAT THE PRODUCT IN QUESTION HAS NOT BEEN DEVELOPED IN ACCORDANCE WITH INDUSTRIAL SAFETY STANDARDS AND IS NOT RECOMMENDED FOR SUCH APPLICATIONS AS PER THE SPECIFIC DATA SHEET. THIS REPORT IS INTENDED SOLELY TO PROVIDE THE CUSTOMER WITH DETAILED INFORMATION ON FAILURE RATES, FAILURE MODE DISTRIBUTION, AND PIN FAILURE MODE EFFECTS ANALYSIS ACCORDING TO IEC 61508, RELATED TO THE POTENTIAL USE OF FUNCTIONAL SAFETY (FS) – ENABLED PARTS IN SAFETY-CRITICAL SYSTEMS.

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